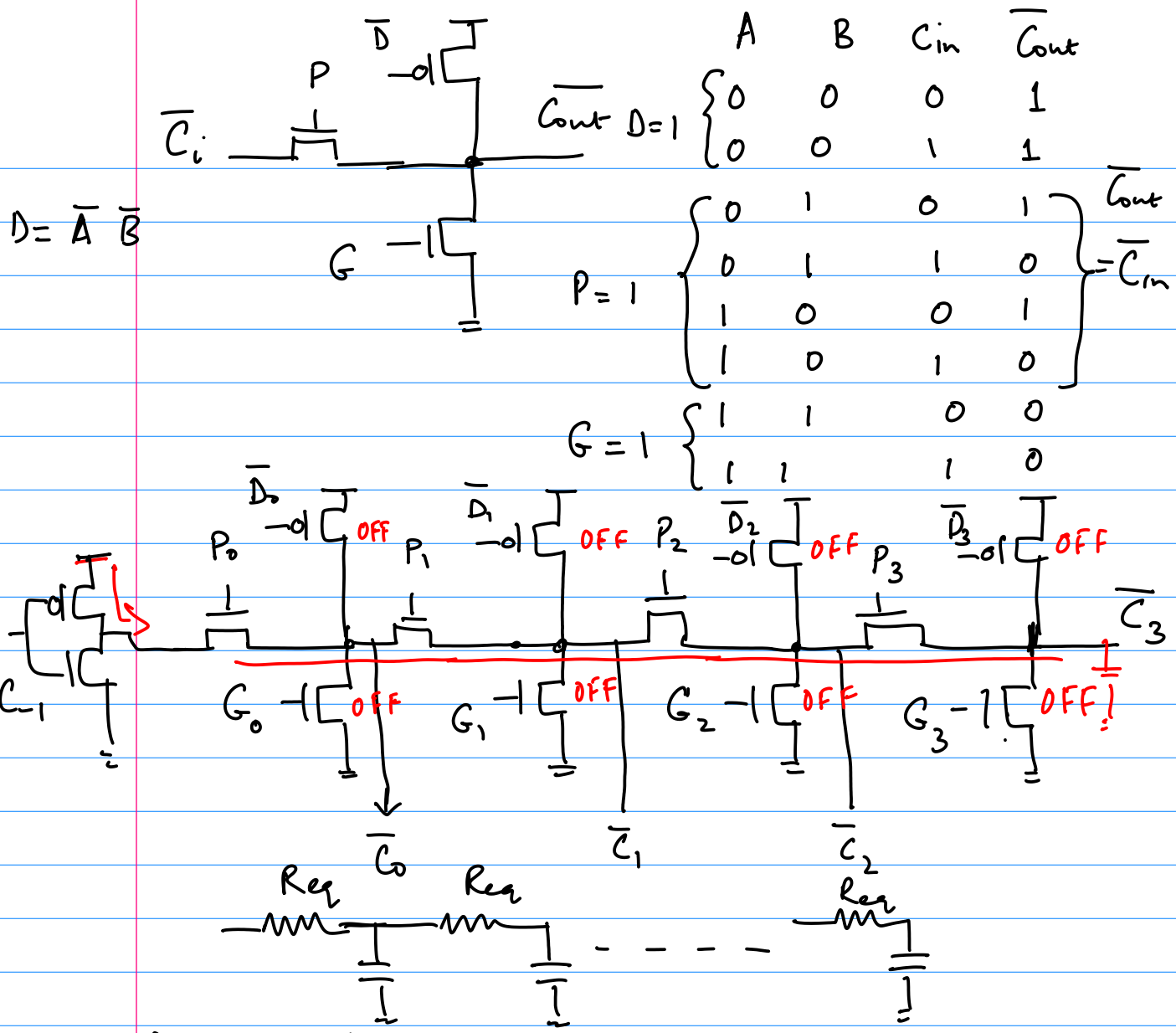
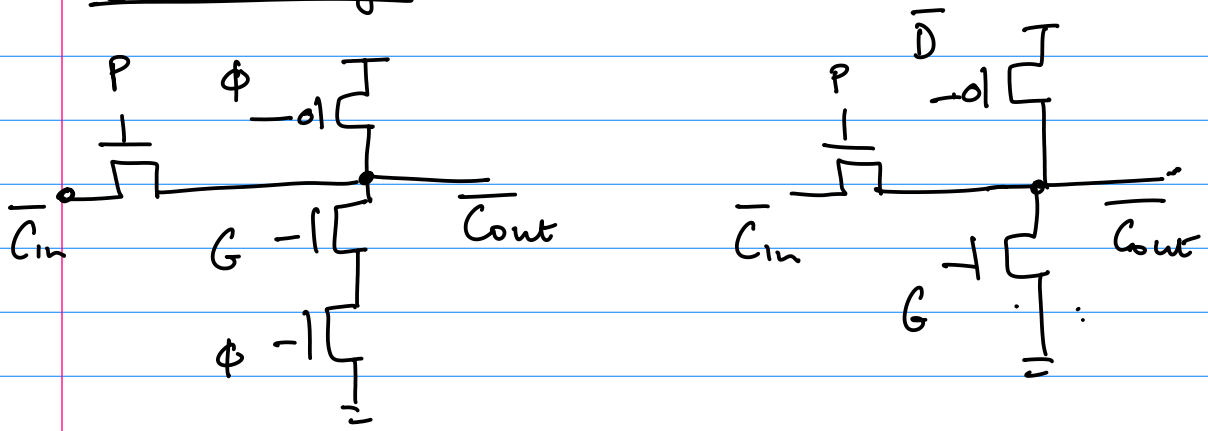
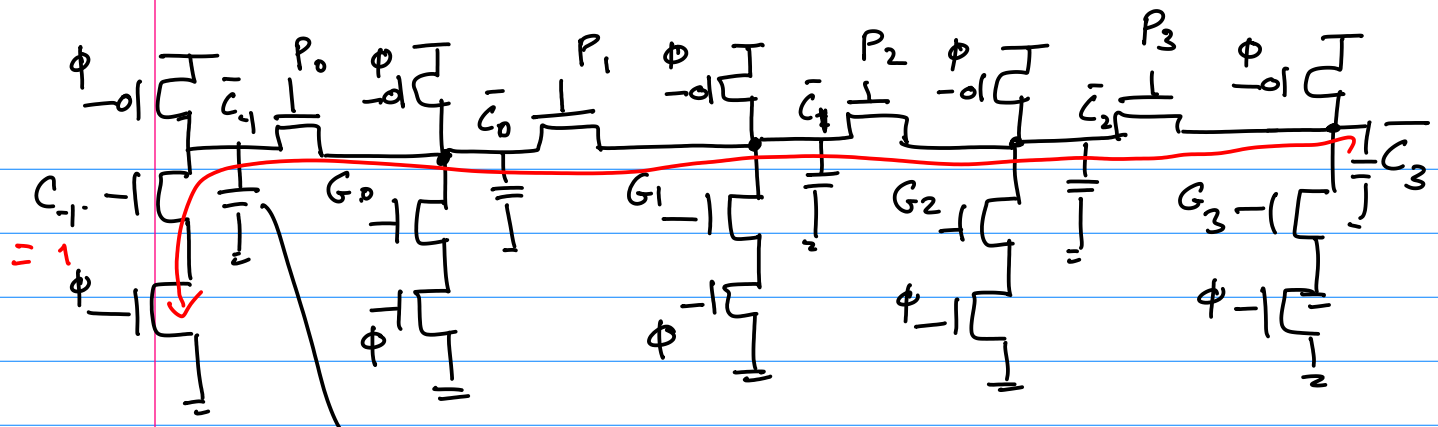


Dynamic logic.

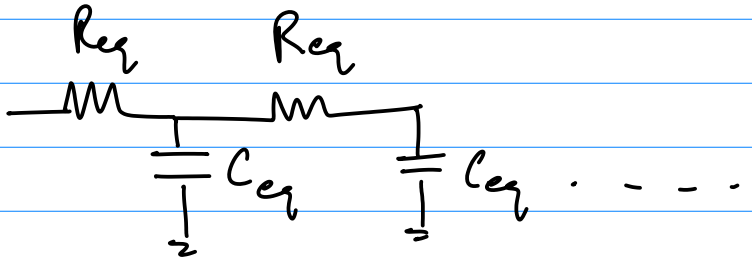


Manchester carry chain

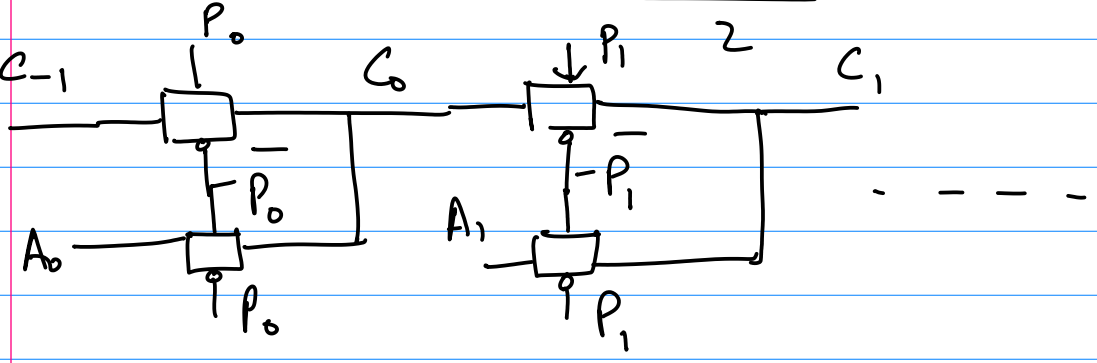


$\phi = 0$ all capacitors will charge

$\phi = 1$; conditionally discharge based on P_i, G_i, C_{i-1}



$\sim R_{eq} C_{eq} \frac{N(N+1)}{2} \longrightarrow N^2$



If we put a buffer every 3-5 stages (depends on the technology) then delay $\propto N$. rather than N^2

Ripple carry

Delay $= (N-1)\, t_{carry} + t_{sum} + t_{setup}$.

constant, need not

worry about it

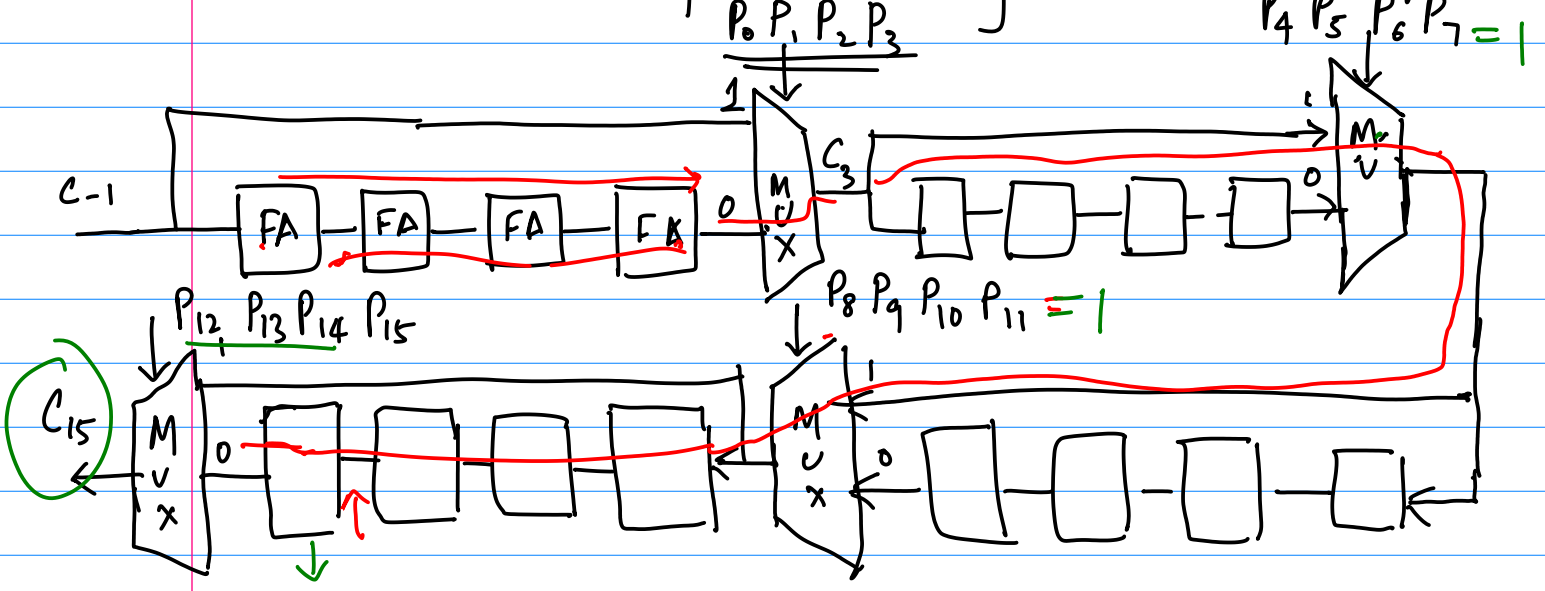
optimise.

So far: cell level optimisation
mirror symmetric, X^scan gate,
dynamic --

Abandon ripple carry (delay ↑^ses linearly with N)

Carry bypass adder.

Worst case is when all the propogate signals are 1 and generate signals = 0.
But this can be detected in advance,
Since propogate signals depend only on the inputs. When all are 1,
route the input carry to the output.



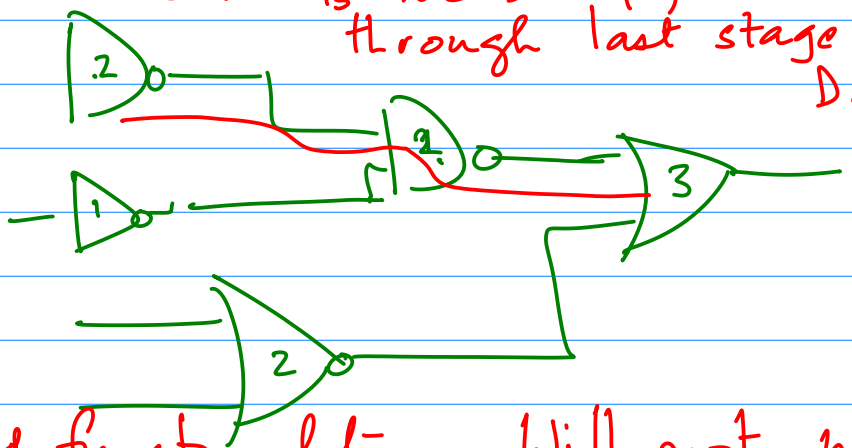
A, B: 0,0 or 1,1
Cout is independent of Cin

In both case $P = 0$.

$P_0 = 0$
$P_{15} = 0$.

Carry generated in 1st stage and ripples through 1st stage; goes through 3 MUXes. C_{15} available earlier; but S_{15} needs C_{14}; has to ripple through last stage.

Delay = 7



Static timing analysis.
- decouple timing and functionality — Will not work for Carry bypass.

Carry bypass adder.

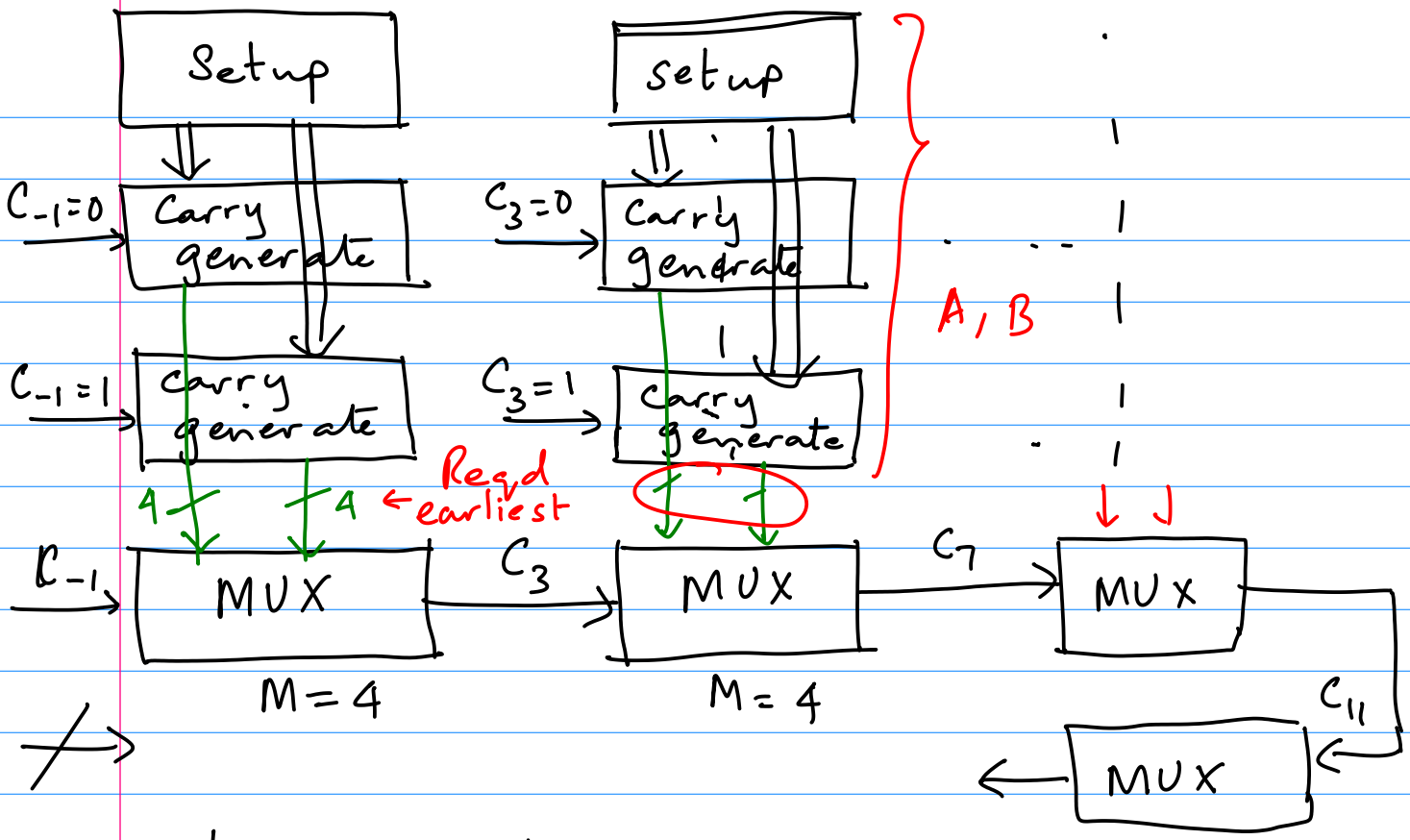
$$\text{Delay} = t_{setup} + \left(\frac{N}{M} - 1\right) t_{mux} + 2M t_{carry}.$$

G, P (const; independent of the no. of bits)

M: block size.
(4 in the example)

N: No. of bits (16)

$$t_{ripple\,carry} = t_{setup} + t_{sum} + (N-1) t_{carry}.$$



$$t_{carrysel} = t_{setup} + \left(\frac{N}{M}\right) t_{mux} + t_{sum}.$$

Variable block size carry select

The first MUX has to decide early., second MUX can get inputs later (cannot decide before arrival of c_3).

First block is size M — $M t_{carry}$

2nd block is size M+1 — $(M+1) t_{carry}$

'P' blocks. ... $M+(P-1)$ → $(M+(P-1)) \cdot t_{carry}$

Each MUX has a variable number of 2:1 MUXes; delay does not increase with the number.

Delay.

$$M + (M+1) + \cdots + M + (P-1) = N;$$

total no. of bits

$$MP + \frac{P(P-1)}{2} = N$$

for large P; LHS $\sim \frac{P^2}{2}$,

$$P \sim \sqrt{2N}$$

Since there are P blocks, for large N, delay $\sim \sqrt{2N}\, t_{mux}$; ↑ses as square root rather than linearly with no. of bits

Same thing can be done for carry bypass.