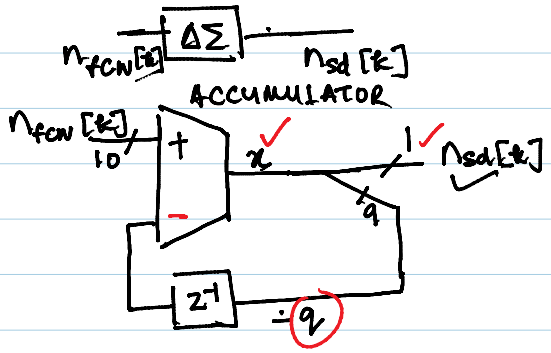
Lecture 43

Tuesday, April 11, 2017
2:55 PM

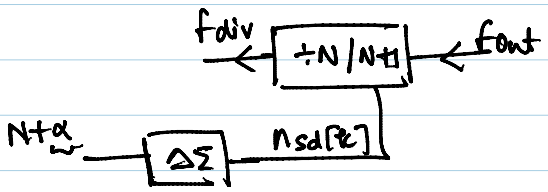


$$x[k] = n_{sd}[k] - q[k]$$

$$n_{fcw}[k] - q[k-1] = x[k]$$

$$n_{sd}[k] = n_{fcw}[k] + q[k] - q[k-1]$$

$$N_{sd}(z) = N_{fcw}(z) + Q(z)(1-z^{-1})$$



$$f_{out} = (N+\alpha) f_{ref}$$

$n_{fcw}[k]$: 10 bit i/p. $\Rightarrow$ $f_{out} = N f_{ref} + \frac{f_{ref}}{2^{10}} \times P$

$0 < P < 2^{10}$ $\qquad \frac{P}{2^{10}} = \alpha$

$P = 4$; $\quad 0 < \alpha \leq 2^{10}-1$

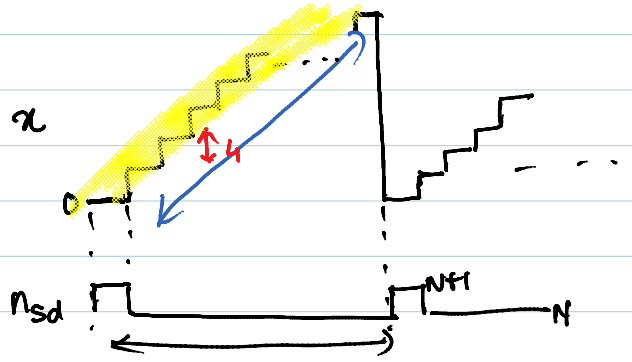
$n_{fcw}[k] = 4$ $\qquad f_{out} = \left(N + \frac{4}{2^{10}}\right) f_{ref}$.

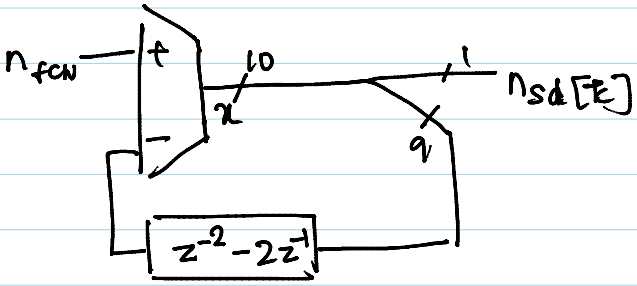
$$n_{sd}[k] = n_{fcw}[k] + (q[k] - q[k-1])$$

$n_{sd}[0] = 0$, $q[0] = 0$, $x[k] = 0$

$x[1] = n_{fcw}[1] + q[0] = 4$

$x[2] = n_{fcw}[2] + q[1] = 8$





n_{fcw} — ΔΣ — n_{sd}

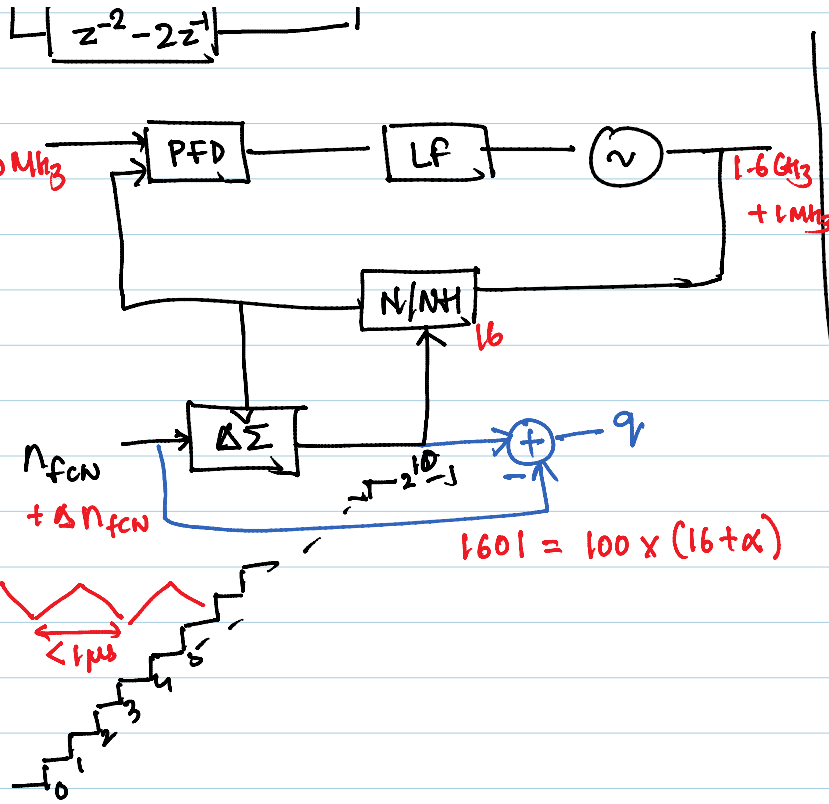
$$N_{sd}(z) = N_{fcw}(z) + (1-z^{-1})Q$$

$$f_{out} = N f_{ref} + \frac{f_{ref}}{2^{10}}$$

$n_{fcw} = 1$

$$NTF(z) = (1-z^{-1})^2$$
$$= 1 + z^{-2} - 2z^{-1}$$

Frac-N PLL



Frac-N PLL

1.) $\Delta F_{MIN} = \frac{freq}{2^N} \leq 100\ kHz$

2) Mine Spur freq. $\geq \frac{freq}{2^N}$

Eg: 900 MHz → 925 MHz

ΔF = 200 kHz

900.200MHz

900.201

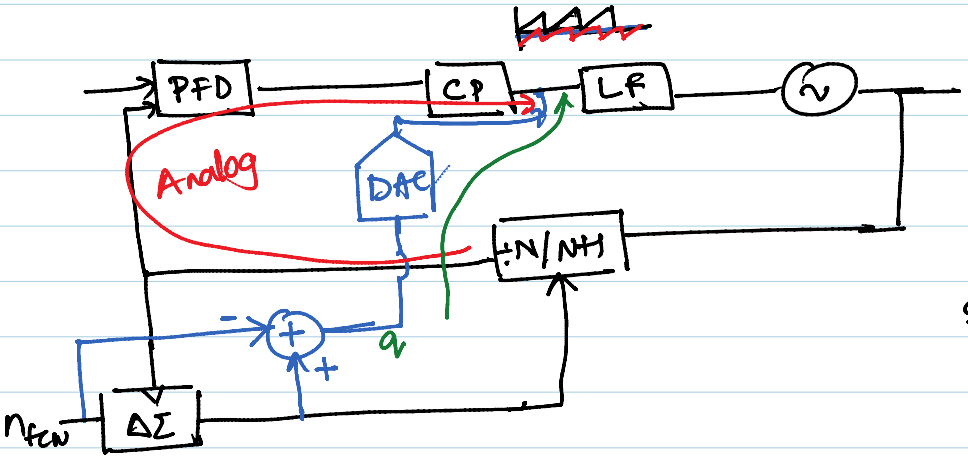
199

freq = 100 MHz

$\frac{freq}{2^{10}} \approx \frac{100\ MHz}{1000} = 100\ kHz$

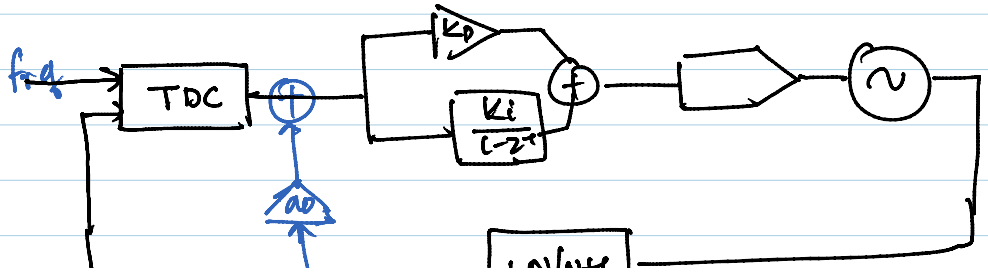
$f_{out} = 1.6\ GHz + n \times 1MHz$

$n_{fcw} = 0, 10, 20, 30 \_$

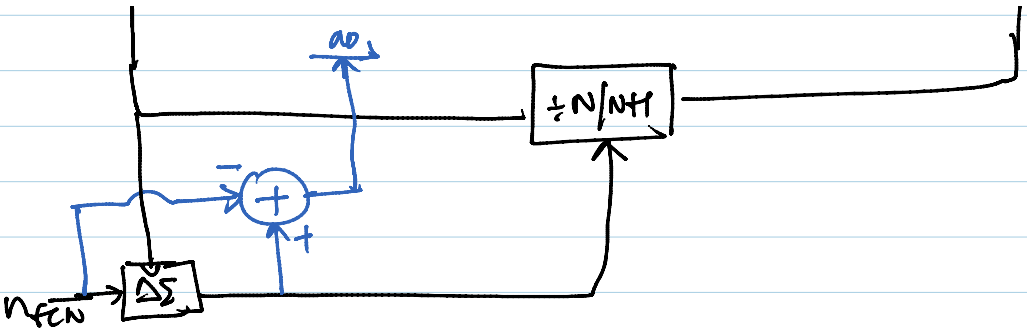


1) Mismatch between two paths for noise cancellation

2) Non-linearity / resolution of DAC limit cancellation of quantization noise



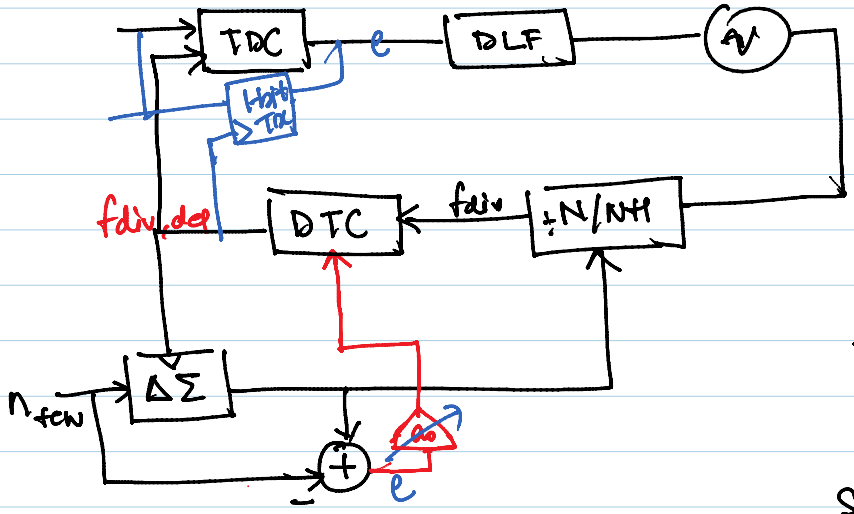
1) TDC resolution is limited by inverter delay.



delay -

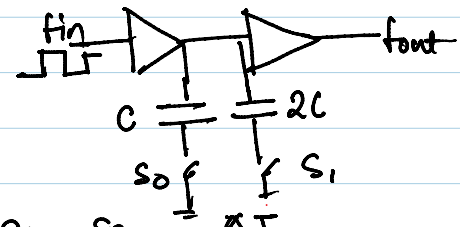
2) TDC non-linearity

3) Quantization noise

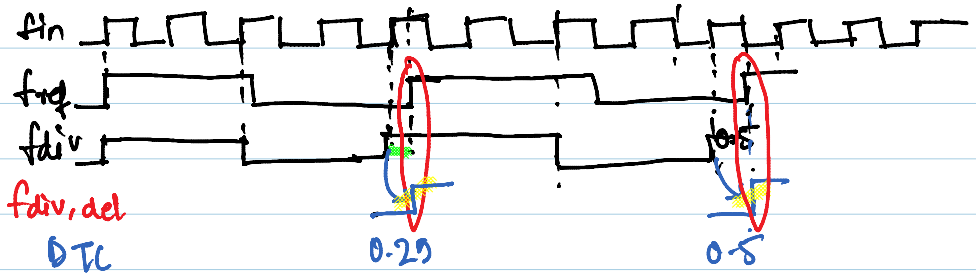


TDC: Time to digital converter

DTC: Digital to time converter



S_1	S_0	ΔT
0	0	~~t offset~~
0	1	$+t_d$
1	0	$+2t_d$
1	1	$+3t_d$

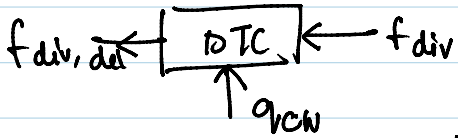


q	n_{sd}
0	0
0.25	0
0.50	0
0.75	0
0	1

f_{out} = 2.5 GHz T = 400 ps

TDC: Δt_d = 5ps

DTC: Δt_d = 0.5ps



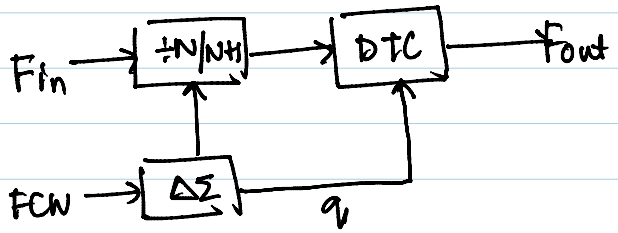
Range of DTC : 400 ps

1) PVT variation for DTC

2) DTC gain must be calibrated

3) DTC non-linearity

q_{FCW} (10-bit) ; $t_d = 0.4\,ps$



Fractional-N Divider