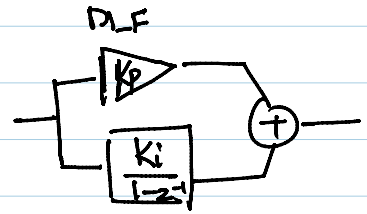
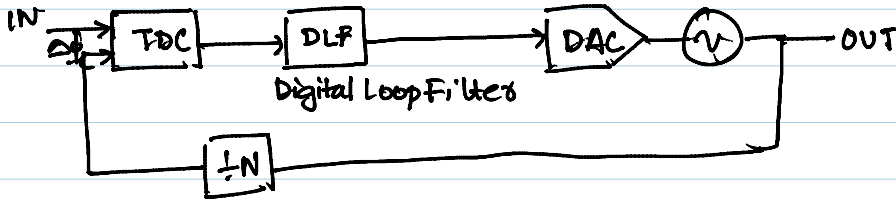
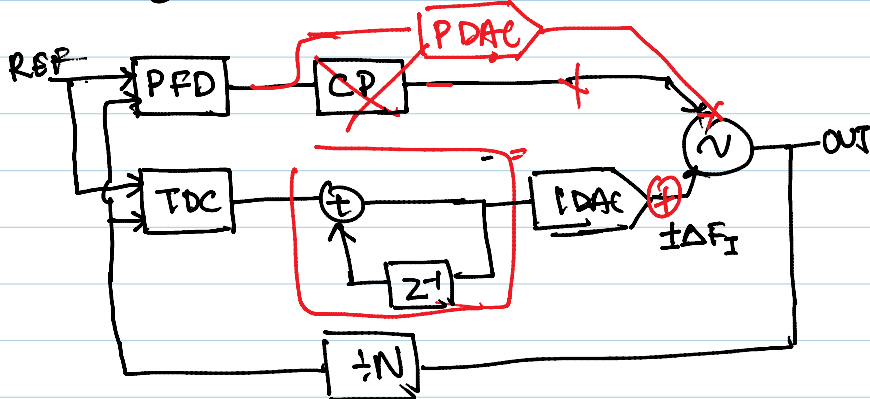


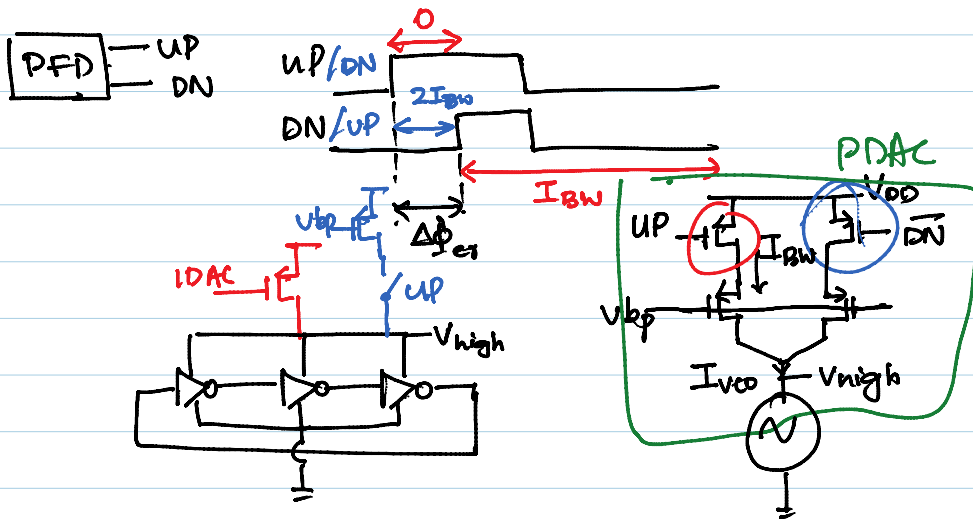
DPLL



Quantization noise of TDC → increases o/p jitter

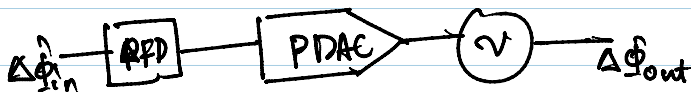


- No quantization noise in proportional path
- Digital accumulator has much lesser area as compared to C_1

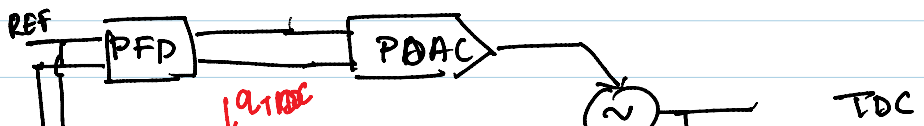


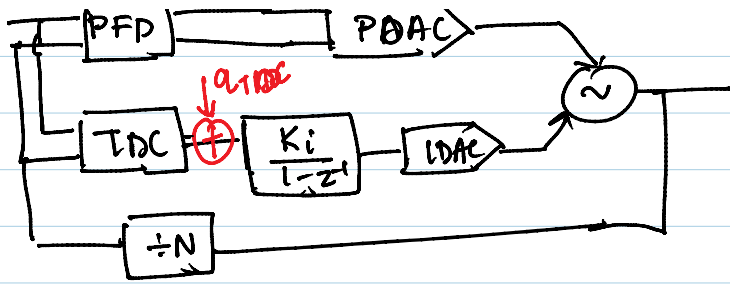
$$I_{vc0} : \begin{matrix} \Delta\phi_{err} \\ 0 \leftarrow I_{BW} \rightarrow -\Delta\phi_{err} \\ \pm I_{BW} \end{matrix}$$

Proportional path gain, $K_p = \frac{1}{2\pi} \times I_{BW} \times \frac{K_{ceo}}{s}$



$$\frac{\Delta\phi_{out}}{\Delta\phi_{in}} = \frac{1}{2\pi} I_{BW} \frac{K_{ceo}}{s}$$





TDC

- Req. range of TDC $\pm 2\pi$
for infinite freq. acq.

Freq: 100 MHz, $T_{sig} = 10\text{ns}$

Range: 20 ns.

$a_{TDC} = 500\text{ ps.} \Rightarrow \frac{20}{0.5} = 40$

1-bit TDC

