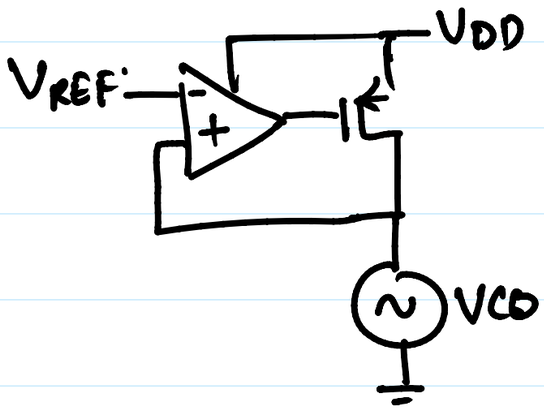
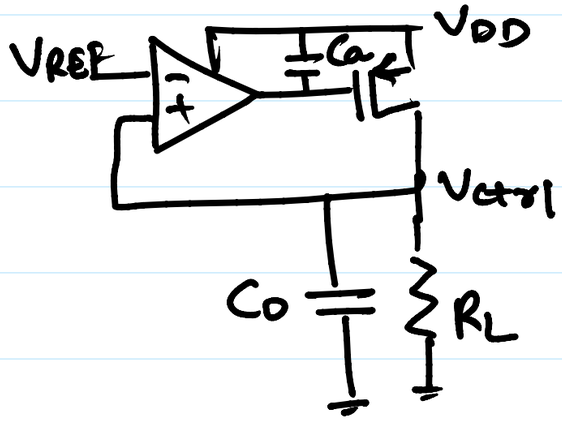
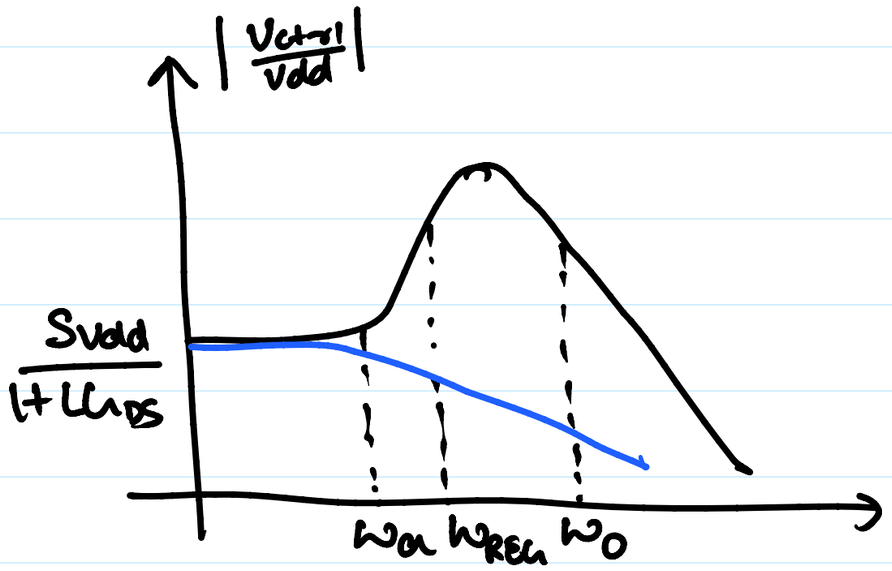
Lecture 29

Monday, March 20, 2017 10:04 AM

PSRR in PLLs.



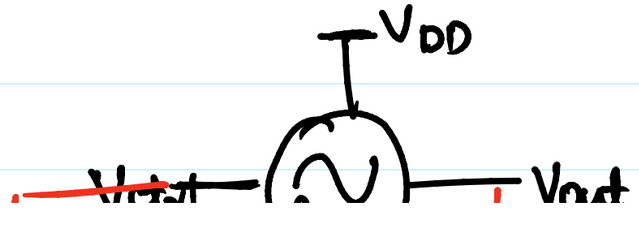




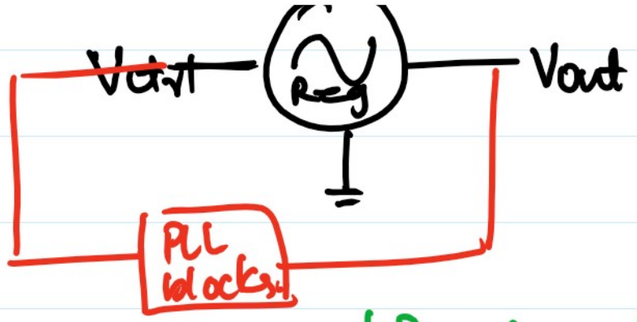
$$\frac{V_{ctrl}(s)}{V_{dd}(s)} = \frac{S_{vdd}}{\left(1+\frac{s}{\omega_0}\right)\left(1+LG(s)\right)}$$

$$LG(s) = \frac{A_a A_o}{\left(1+\frac{s}{\omega_a}\right)\left(1+\frac{s}{\omega_0}\right)}$$

$$\omega_a = \frac{1}{r_{oa} C_a} \quad , \quad \omega_0 = \frac{1}{(r_{dsp} \| R_L) C_o}$$

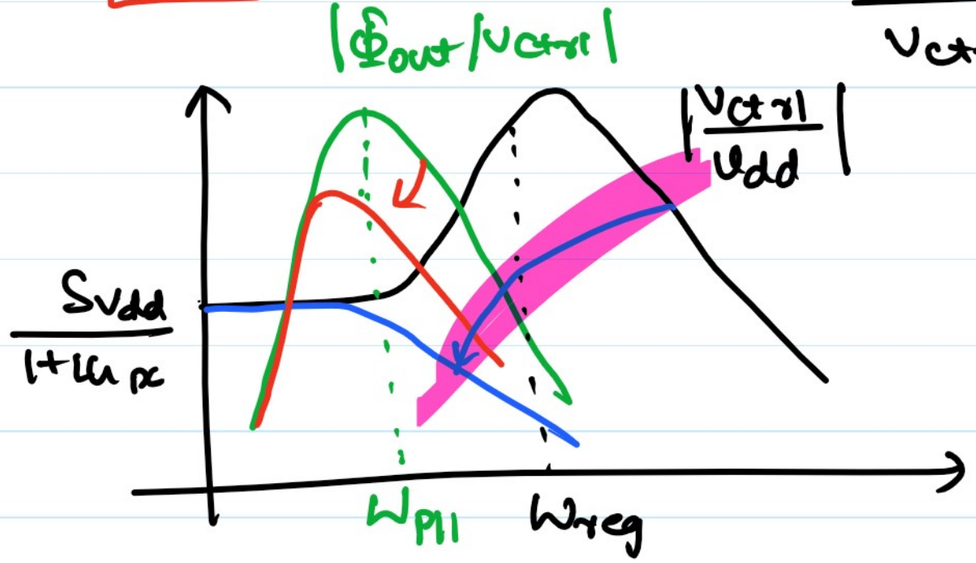


$$\frac{V_{ctrl}(s)}{} = \frac{S_{VDD}}{}$$



$$\frac{V_{ctrl}(s)}{V_{DD}(s)} = \frac{\Delta V_{DD}}{(1+s/\omega_0)(1+LG_{reg})}$$

$$\frac{\Phi_{out}(s)}{V_{ctrl}(s)} = \frac{K_{VCO}}{s} \frac{1}{1+LG_{RPLL}}$$



$$\frac{\Phi_{out}(s)}{V_{DD}(s)} = \frac{V_{ctrl}(s)}{V_{dd}(s)} \times \frac{\Phi_{out}(s)}{V_{ctrl}(s)}$$

$$LG_{RPll}(s) = \underbrace{\frac{I_{cp}}{s^2(C_1+C_2)} \frac{1}{2\pi} K_{VCO} \frac{(1+s/\omega_z)}{(1+s/\omega_{p3})}}_{\text{w/o reg}} \times \underbrace{\left(\frac{1}{1+s/\omega_{reg}}\right)}_{\text{w/ reg}}$$

For better PSRR

a) $\omega_{Pll} < \omega_{reg}$ $\Rightarrow$ large power in reg

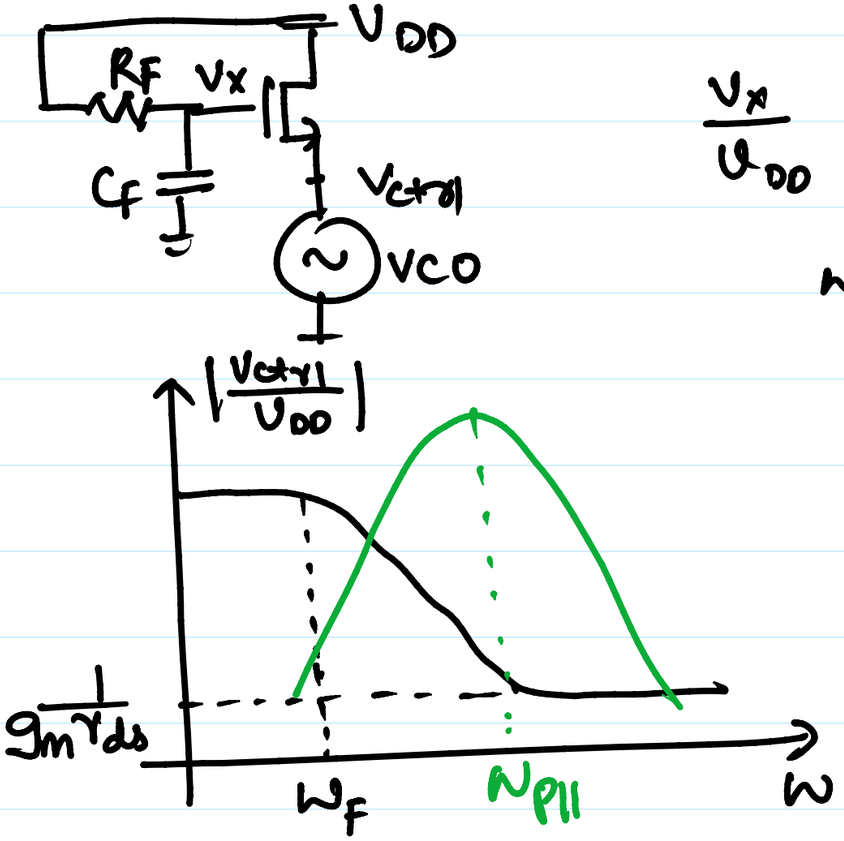
b) $\omega_0 < \omega_a$ for regulator $\Rightarrow$ large capacitor, lower PLL bandwidth

c) Lower PLL bandwidth $\Rightarrow$ Increase in VCO noise

c) Lower PLL bandwidth ⇒ Increase in VCO noise.

Techniques to improve PSRR

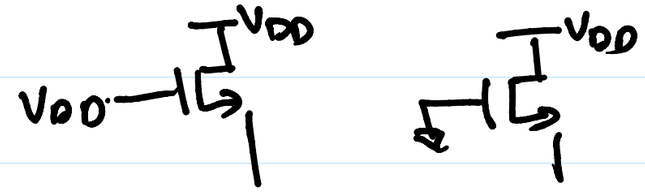
1) NMOS as current source.

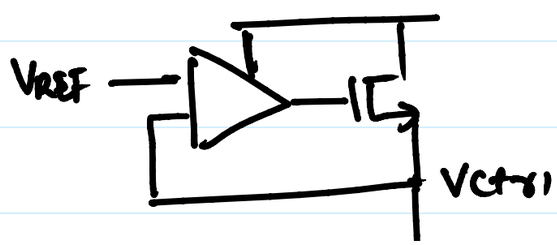


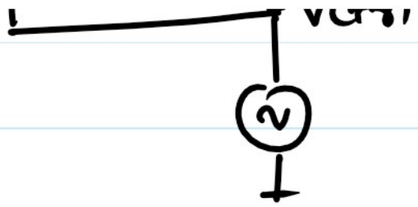
$$\frac{V_x}{V_{DD}} = \frac{1}{1+sC_F R_F}$$

$$\omega_F = \frac{1}{C_F R_F}$$

For better PSRR ; $\omega_F \ll \omega_{PLL}$

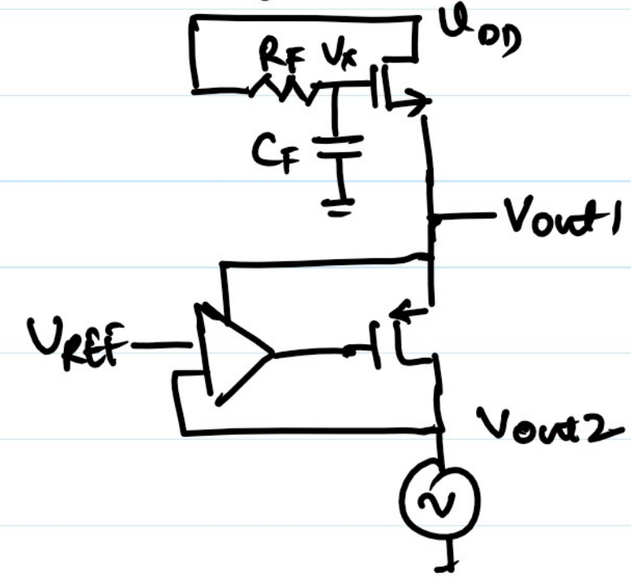


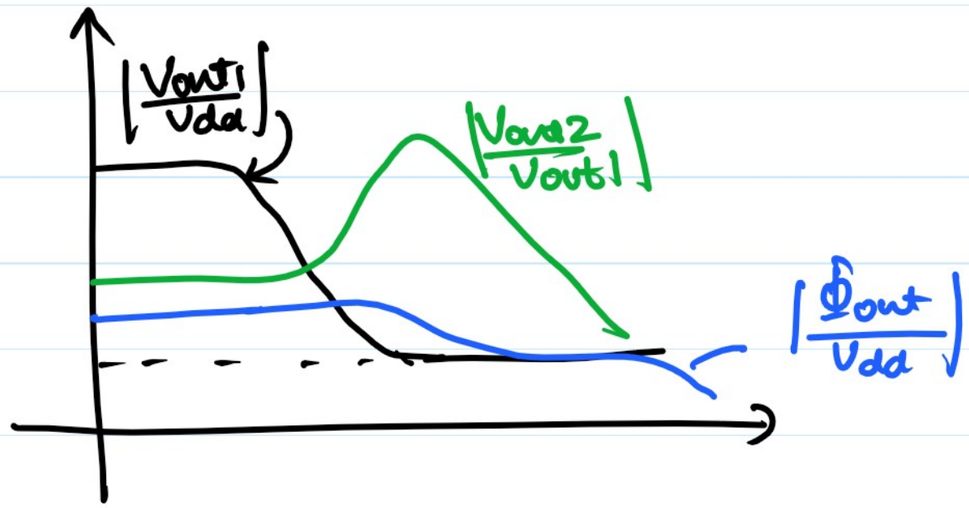




Cascaded Regulators

b)



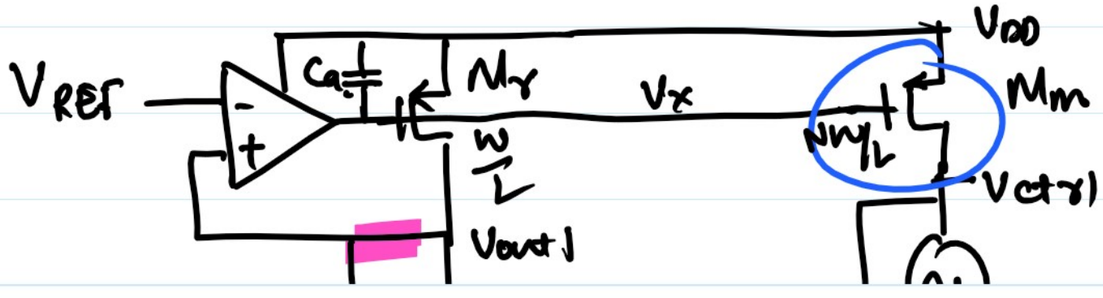


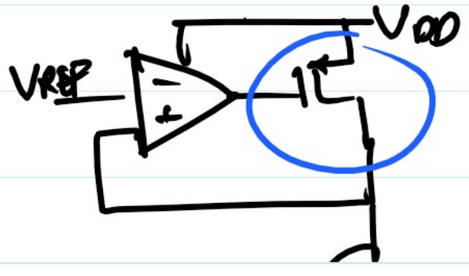
Cons: Larger headroom for regulator

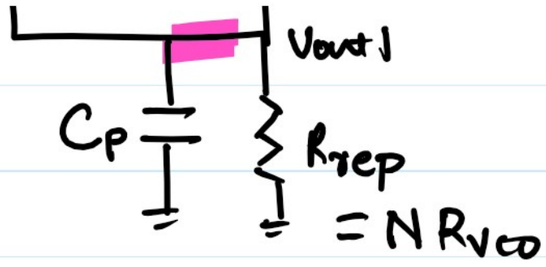
In a given CMOS technology

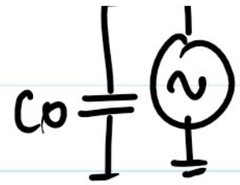
Regular Vt, low Vt, high Vt, Native

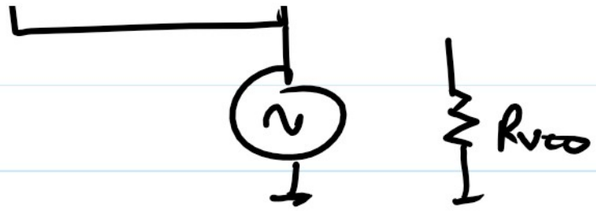
c) Replica-biased LDO

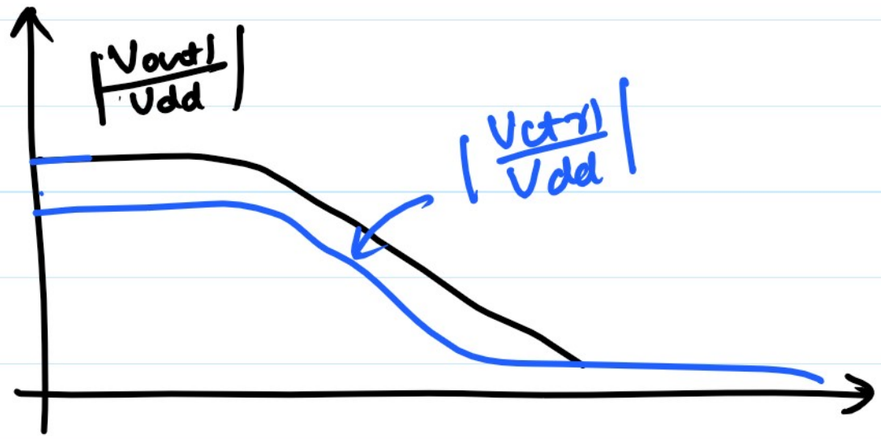






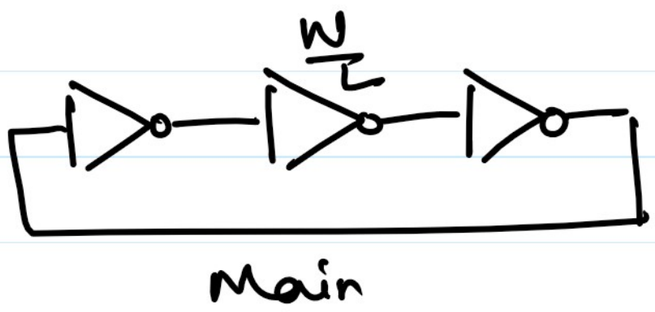




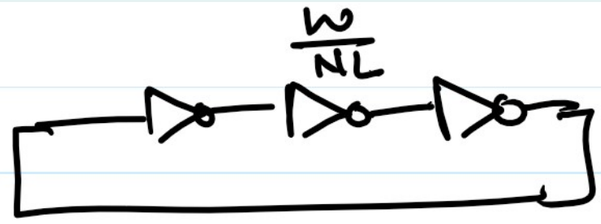


Remarks

- Mismatch between M_r and M_m degrade PSRR



Main



Rep.