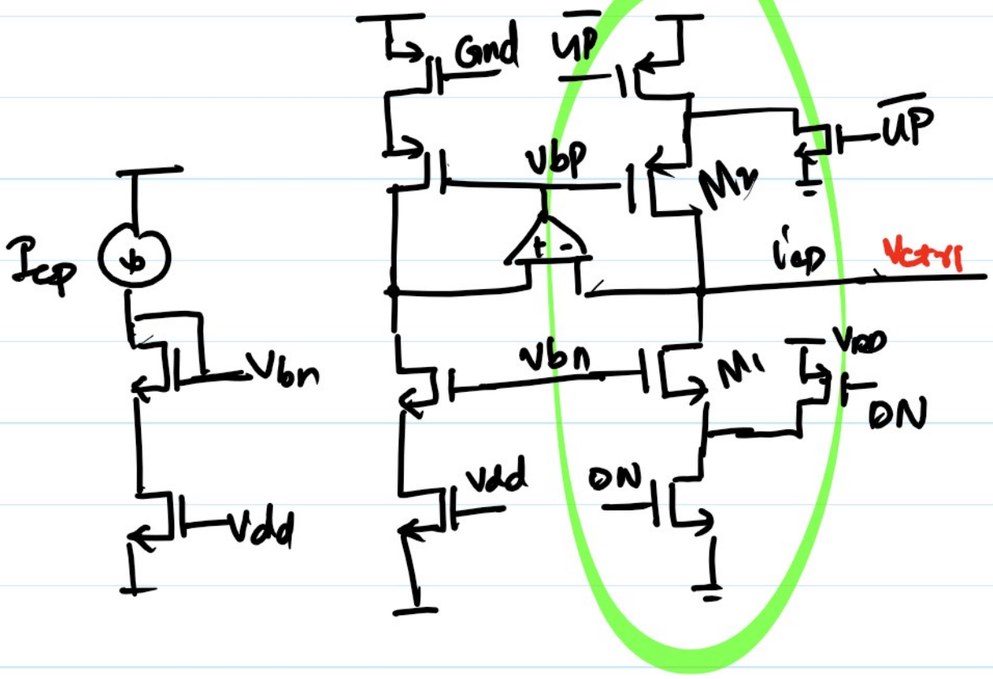
Lecture 21

Monday, February 20, 2017 9:56 AM

Charge-pump.

Source-switched CP

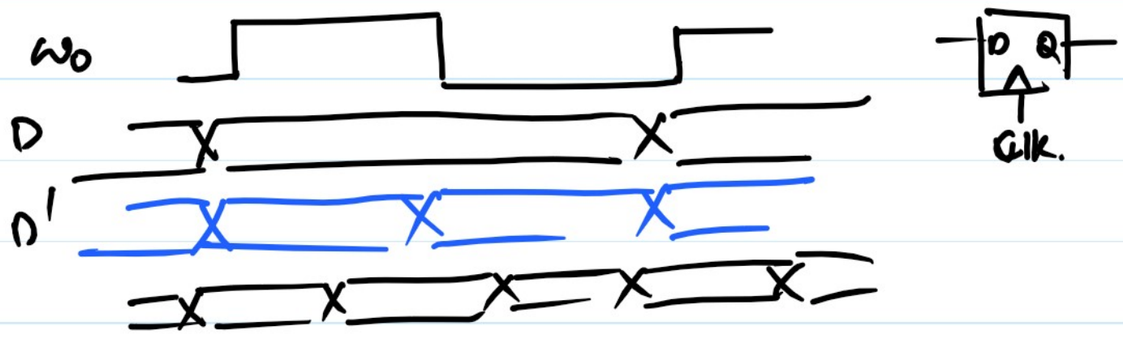


* PMOS/NMOS current source switch between cutoff to saturation region.
* T_{ON} mismatch between I_{up} & I_{dn}.

Delay locked loop.

$V_{in} = A\sin(\omega t)$

ω_0, 1-phase



— Multi-phase Clk required in sub-rate clock & data recovery

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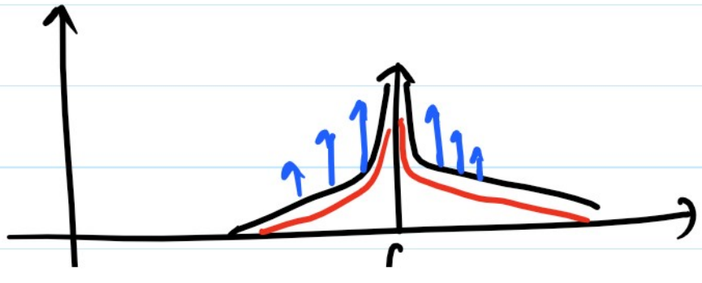
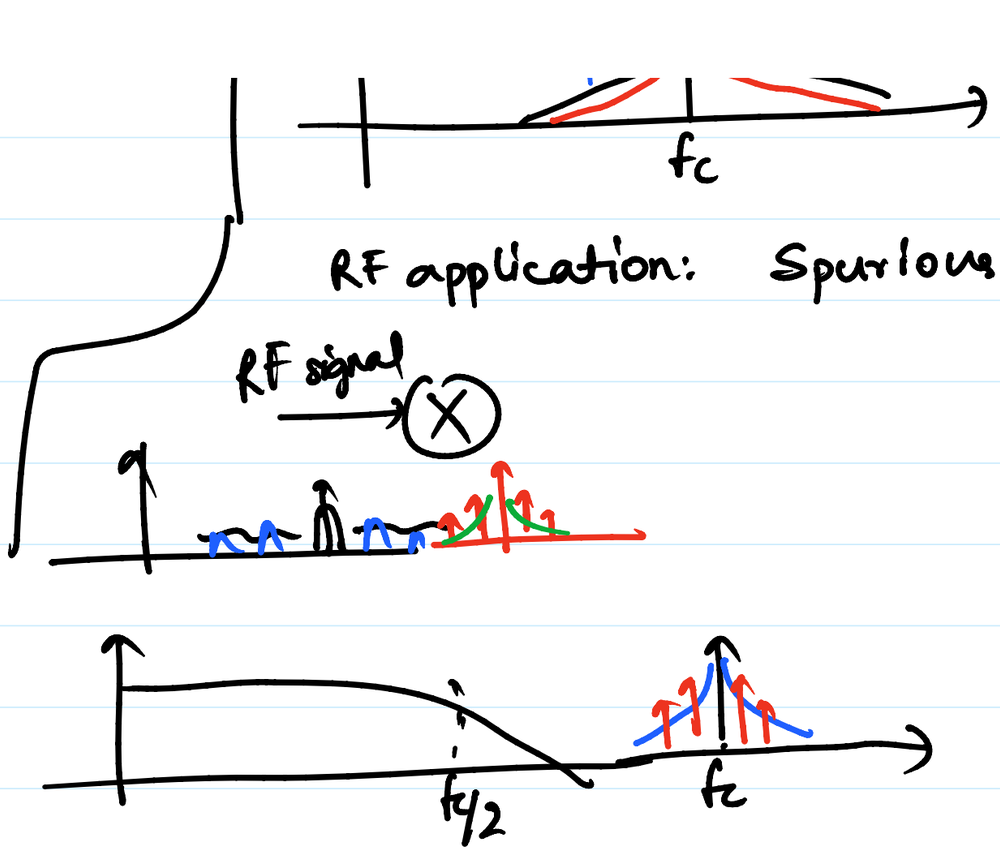
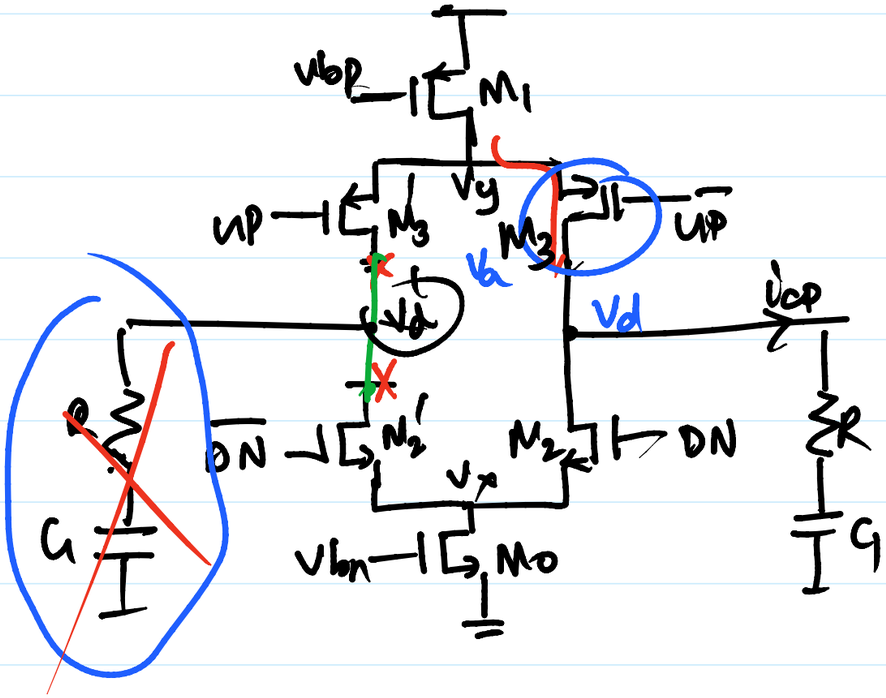
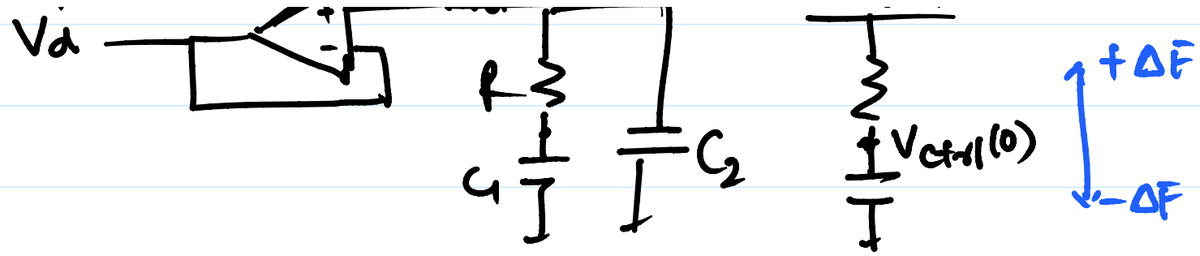
$t_{d,inv}$ = 1 clock period

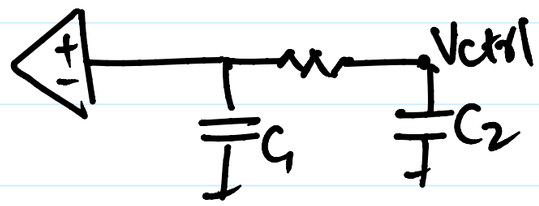


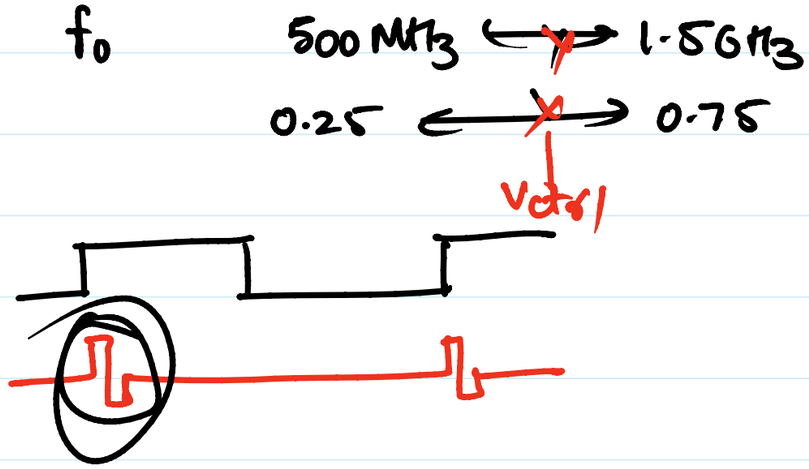




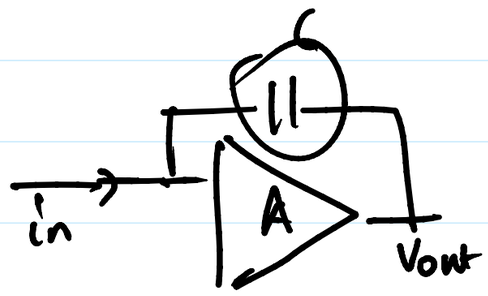
- ✗ Current source is always ON.
- ✗ Static-power consumption.
- ✓ Faster in switching.
- ✓ Transients on Vx/Vy are limited
- ✓ UP/DN signals can be limited swing
- ✗ clock feed-through is a problem

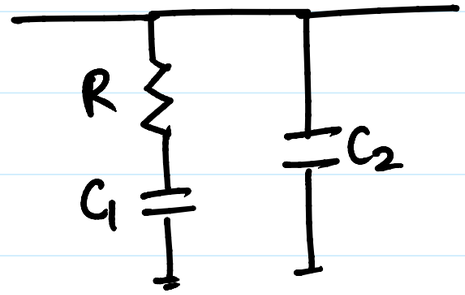


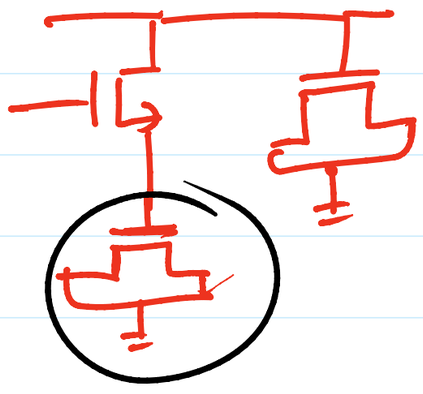




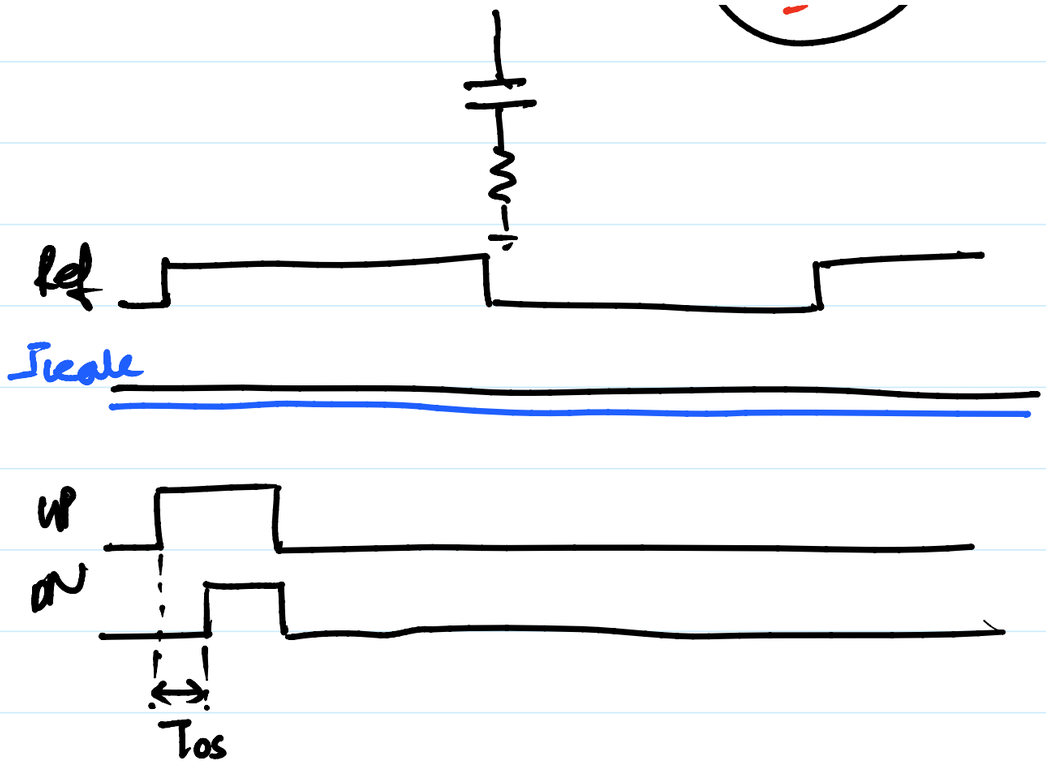
Loop filter







* Large phase margin → large C_1
  loop F
* Resistor choice is based on noise
* Leak current in active devices
* Active MOS capacitance is dependent on control voltage



$$I_{up} = I_{dn} = I_{cp}$$

$$I_{leak} \ll I_{cp}$$

$$I_{cp} \times \frac{T_{os}}{T_{ref}} = I_{leak}$$

$$T_{os} = \frac{I_{leak}}{I_{cp}} \cdot T_{ref}$$