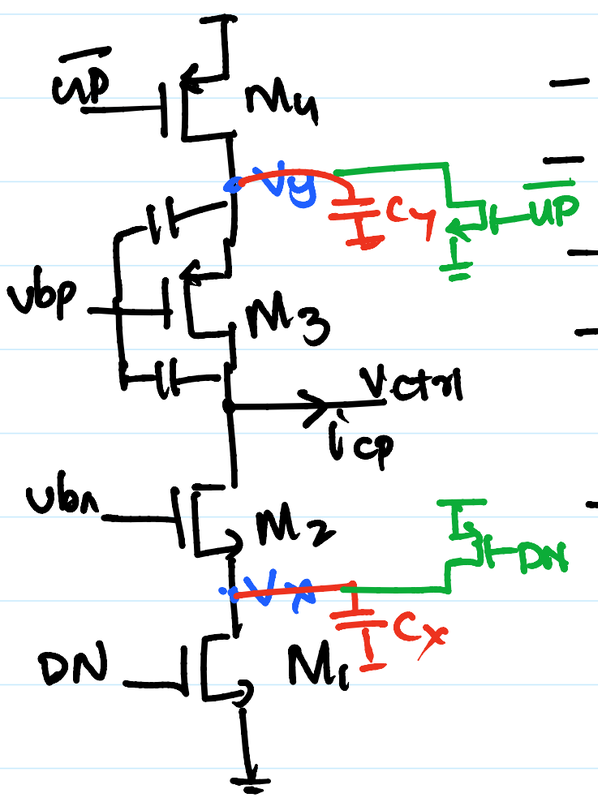
Lecture 20

Thursday, February 16, 2017 11:22 AM

Lecture-20.

Charge-pump Design

1. Drain-switched CP
2. Gate-switched CP
3. Source-switched CP



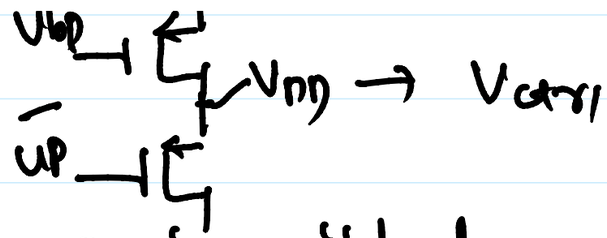
- M_2, M_3 are current sources
- M_1, M_4 are switches
- Clock feedthrough ↓
- In active phase — $V_x \rightarrow$ Gnd, $V_y \rightarrow V_{dd}$
- In reset phase — $V_y \rightarrow V_{bp} + |V_{tn}| \rightarrow V_{dd}$, $V_x \rightarrow V_{bn} - V_{tn} \rightarrow$ Gnd

M_3 : $|V_{DS}| \longrightarrow V_{bp} + |V_{tn}| - V_{ctrl}$

M_2 : $V_{DS} \longrightarrow V_{ctrl} - (V_{bn} - V_{tn})$

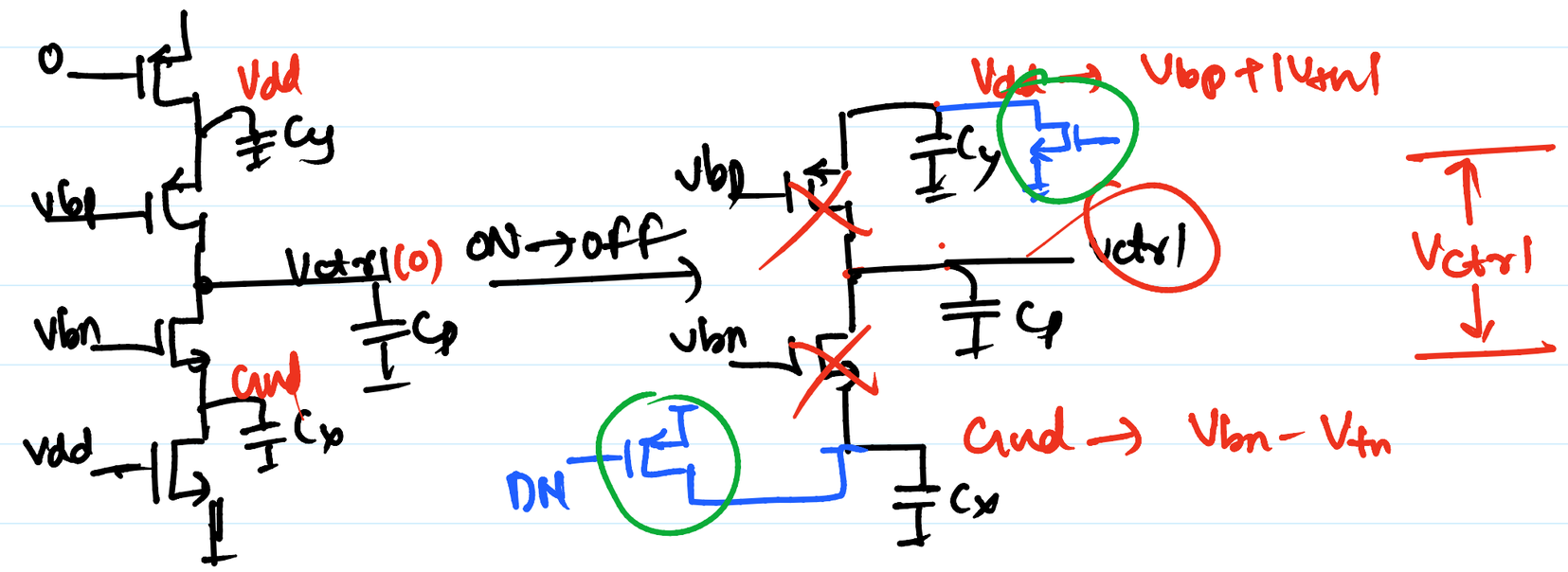
Vbp

$V_{bp} \rightarrow V_{ctrl}$

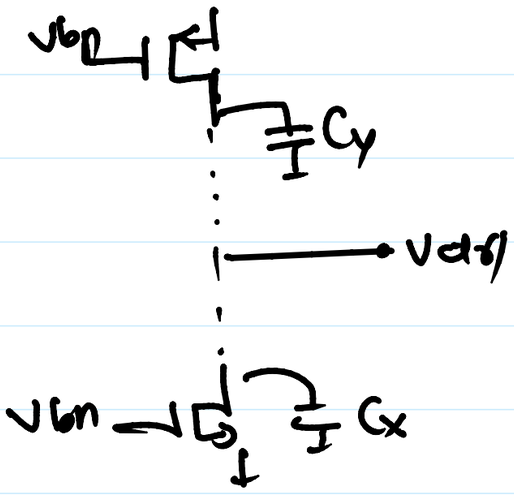


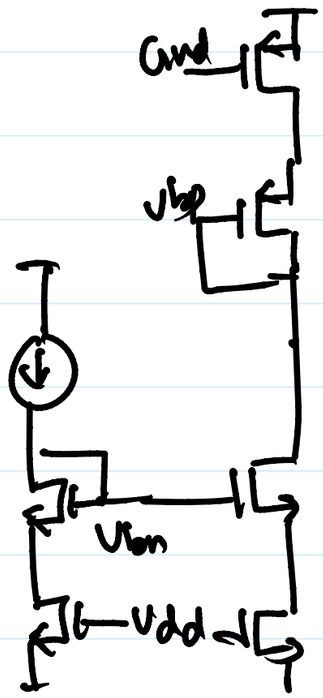
- Charge sharing between V_x & V_y ⇒ ΔV_{ctrl}

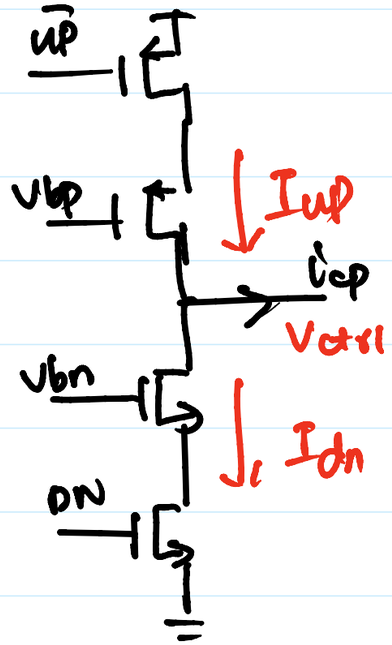
$V_{DS} = 0$ in off-state



Drain-switched ⟶

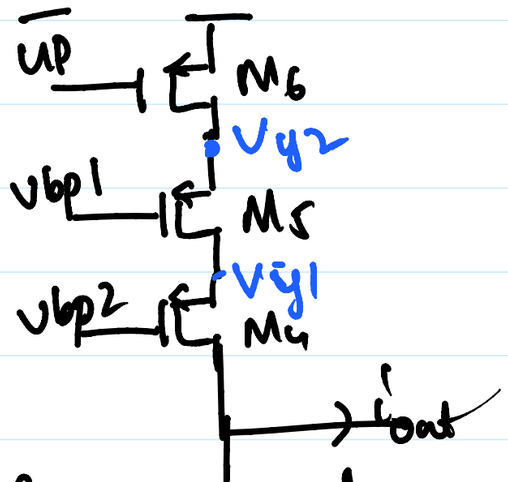






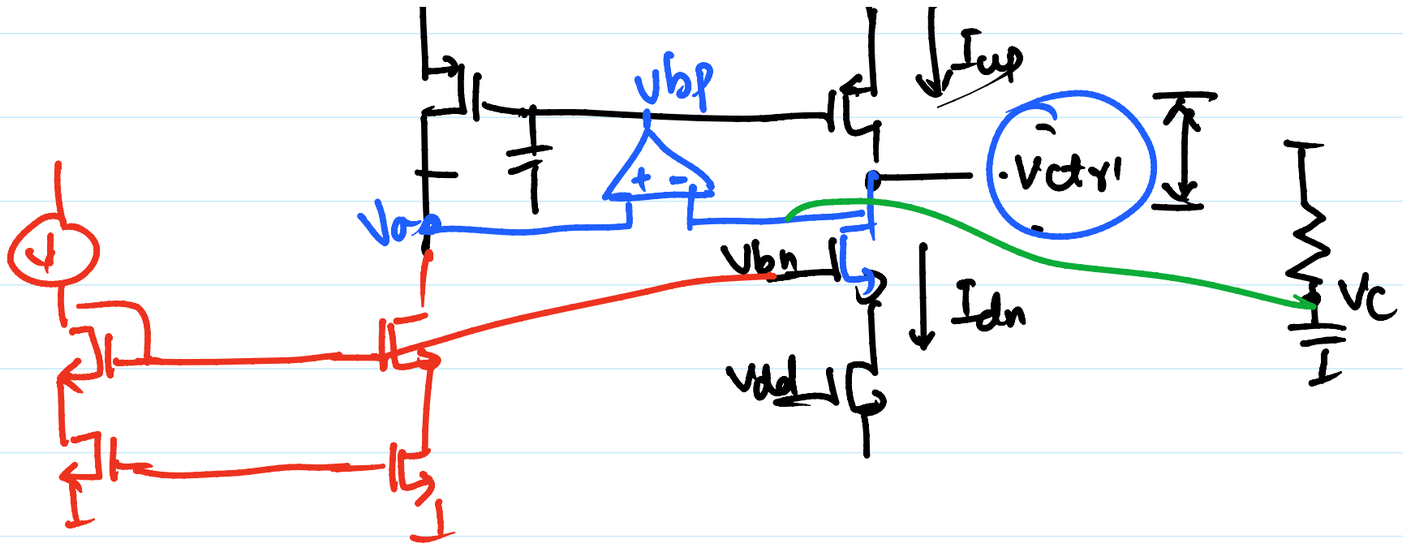
- $I_{up} \neq I_{dn}$: Channel length mod.

→ Cascode current source



Cas. current source.

* Larger Rout for current source.
* V_{ctrl} range is reduced.
→ Speed of operation is reduced


Vbp
Iup
Vctrl
Vop
Vbn
Idn
Vdd
Vc