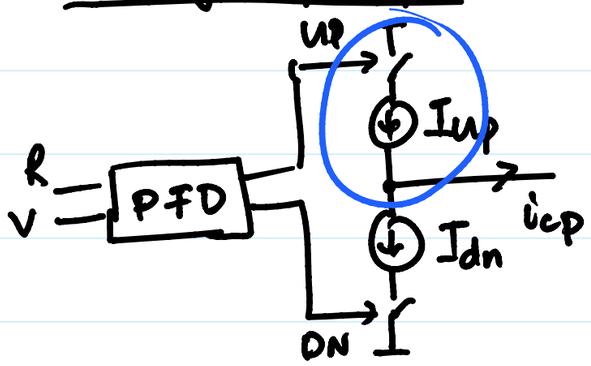
Lecture 19

Wednesday, February 15, 2017 8:02 AM

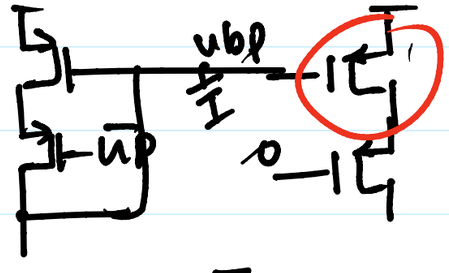
Building blocks of CP-PLL

Charge pump

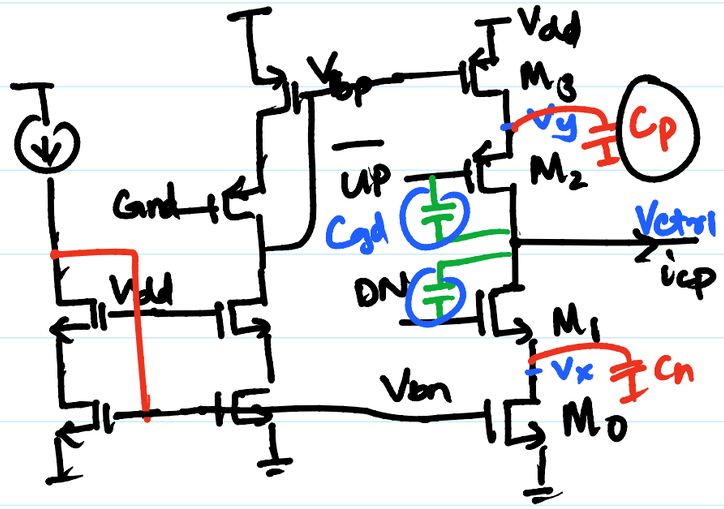


$I_{up} = I_{dn} = I_{cp}$

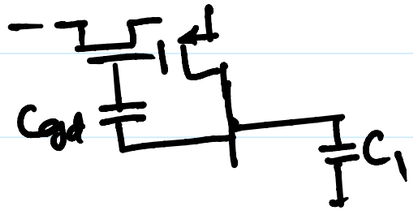
- Current source (PMOS/NMOS, $R_{out} = \infty$)
- Switch ($R_{ON} = 0$, $R_{OFF} = \infty$)



Drain-switched charge pump



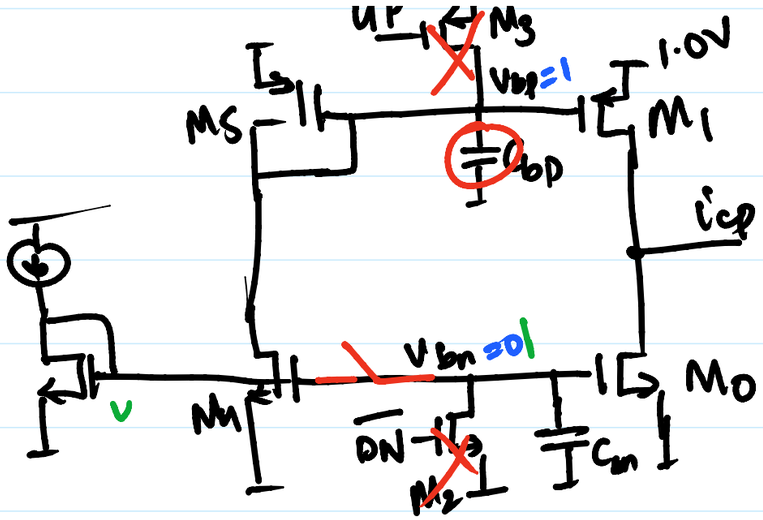
- M_0, M_3 current sources
- M_1, M_2 are switches
- $\overline{UP} = 1$, $DN = 0$, $V_x = 0$, $V_y = 1$
  M_0, M_3 in linear region
- Large transient current during switch-ON.
  $\Rightarrow$ ΔI pushed in Loop filter every ref. period



Clock feed-through.

Gate-switched charge pump

- M_0, M_3 are current sources.



- M_0, M_1 are current sources
- In off-state, $V_{gs,n} = 0$, $V_{gs,p} = 0$
- ✓ OFF → ON state, M_0, M_1 are in saturation
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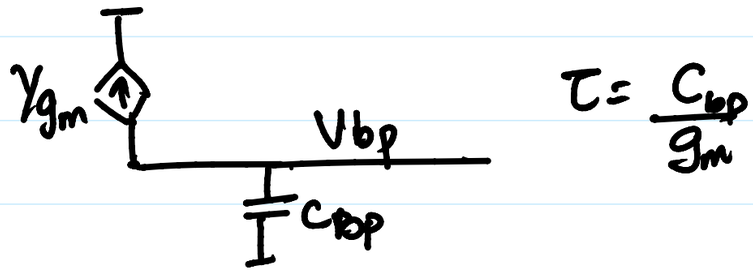
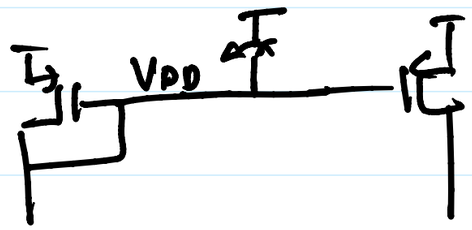


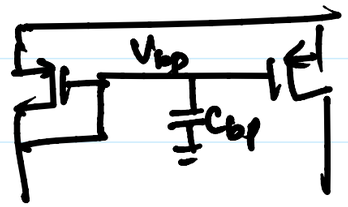
$$\tau = \frac{C_{bp}}{g_m}$$

Faster settling → large g_m
(more power)
Large gate capacitance
→ slower settling

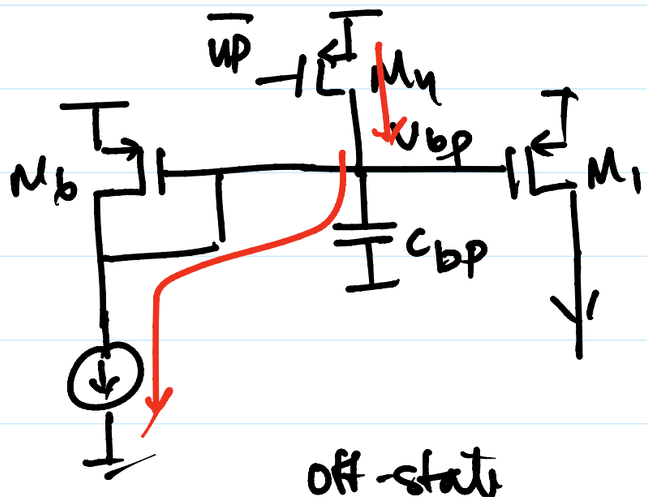
OFF-state



ON-state

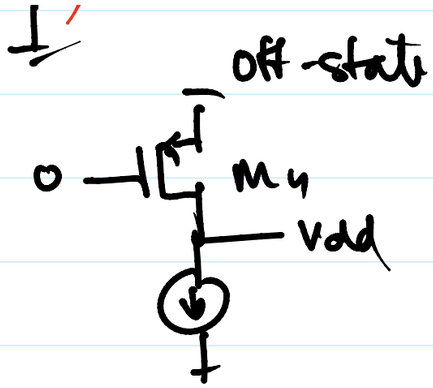


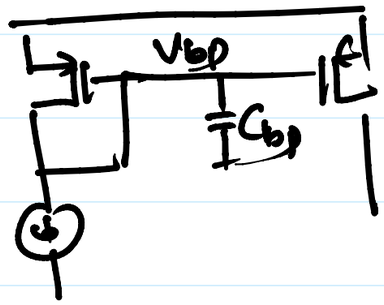
- lesser clock feed-through
- DN = 0, UP = 1 ⇒ $V_{bn} = 0$

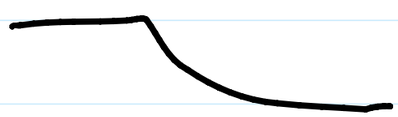


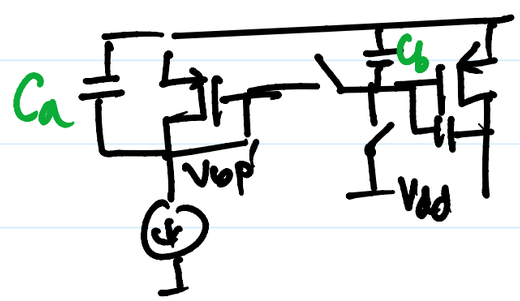
UP = 1, M6, M1 cut-off.

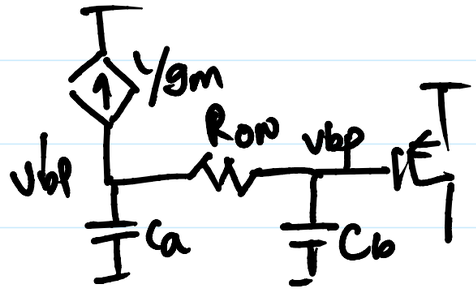
off-state









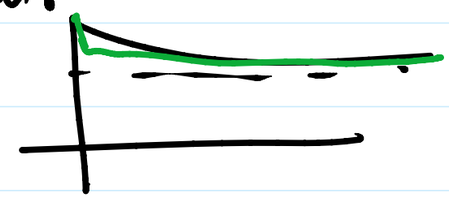


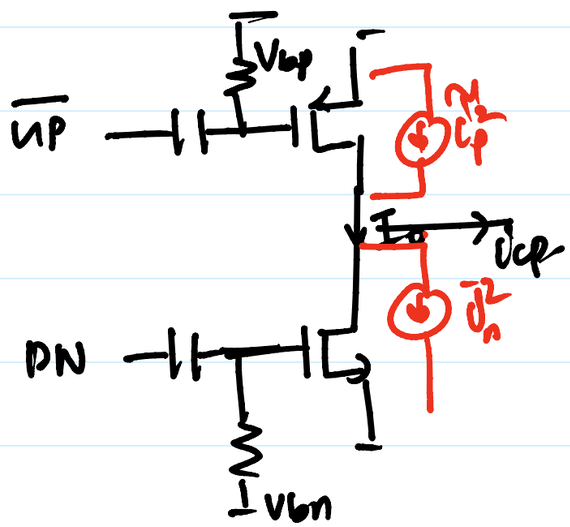
- $I_{up} = I_{dn} = I_{cp}$
- $I_{up} = I_{dn} = 0.9 I_{cp}$ ...

$f=0^-$; $V_{bp} = V_{DD}$, $V'_{bp} = V_{bp}(\infty)$

$\Rightarrow$ Loop-gain $\rightarrow$ τ_{lk} $\rightarrow$ Ref-spur

$I_{up} = 0.99 I_{cp}$
$I_{dn} = 0.98 I_{cp}$
$\Delta I = 0.01 I_{cp}$





$$i_{cp} = \left(g_{mp} V_{up} - g_{mn} V_{dn}\right)$$

$$\overline{i_{cp,n}^2} = \left(\overline{i_p^2} + \overline{i_n^2}\right) \times \left(\frac{T_{rst}}{T}\right)$$

$\frac{0.2n}{10ns} = \frac{1}{50}$

- $I_{cp} = 100\mu A$ (static power)
- UP / DN CMOS logic

- $\overline{UP}$ / DN CMOS logic.
- Linearity of CP