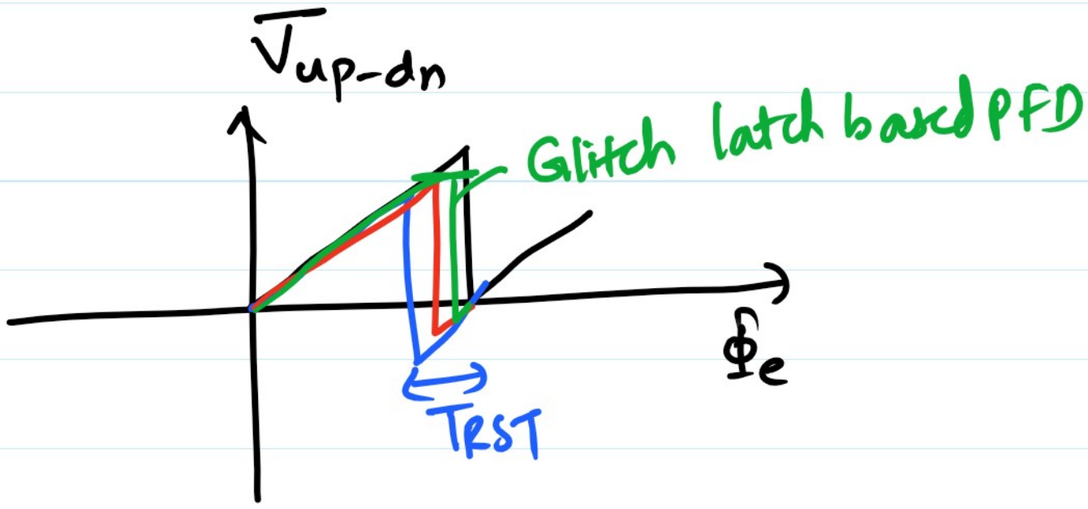
Lecture 16

Thursday, February 9, 2017 3:03 PM

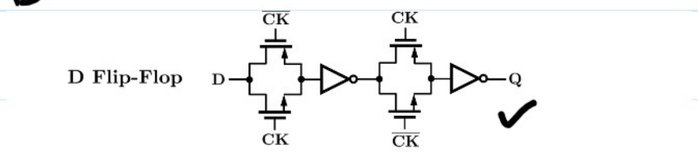
Building blocks of PLL.

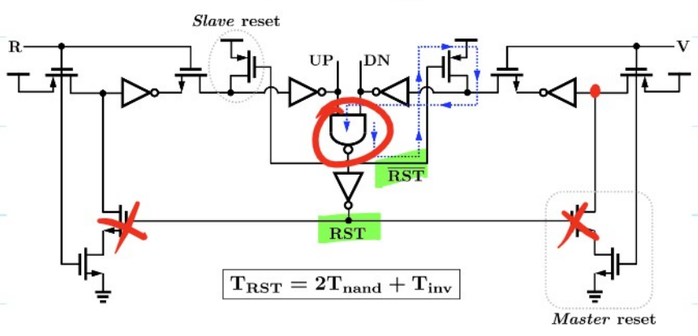
PFD: 1.) NAND based PFD

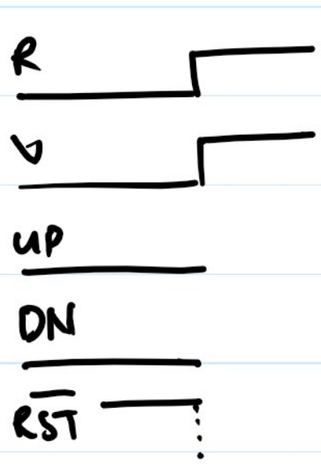
$$T_{RST} = T_{nand4} + 2T_{nand2} + t_d$$



2) Pass-transistor PFD



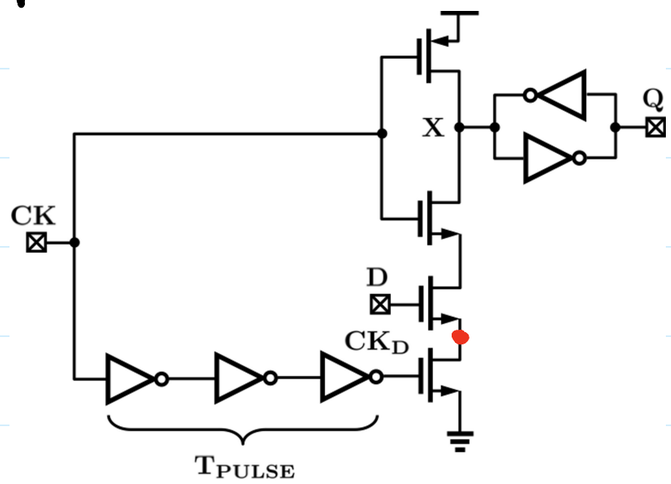


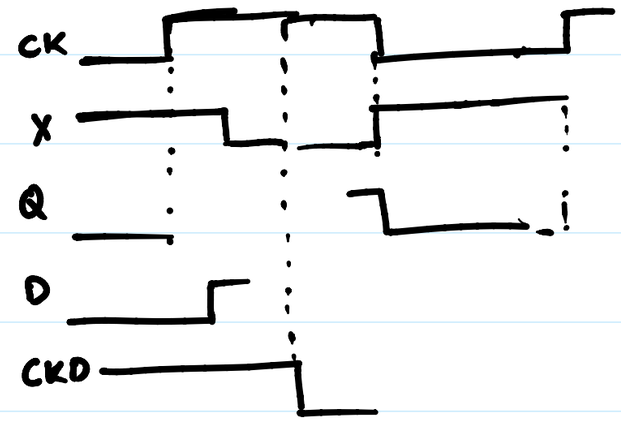


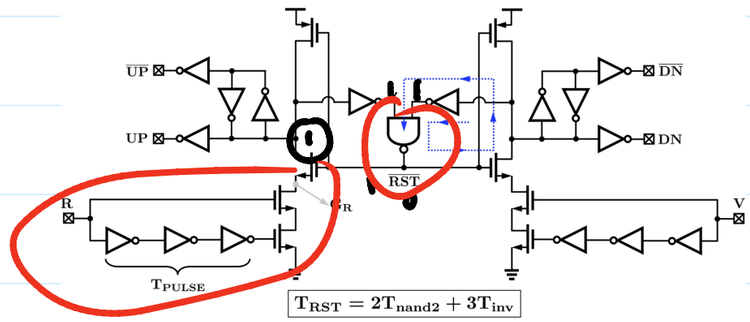
3) Glitch-latch based PFD

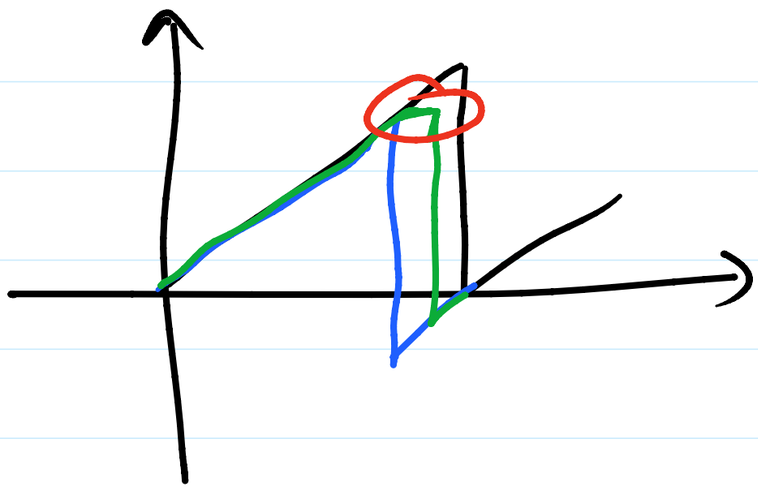
Glitch-latch flip-flop

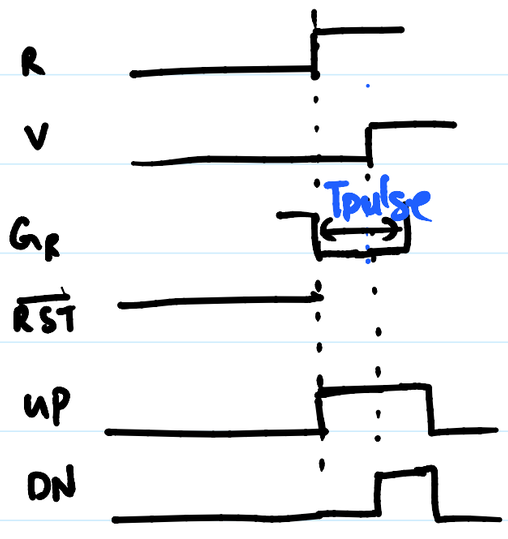
Standard Flip-Flop

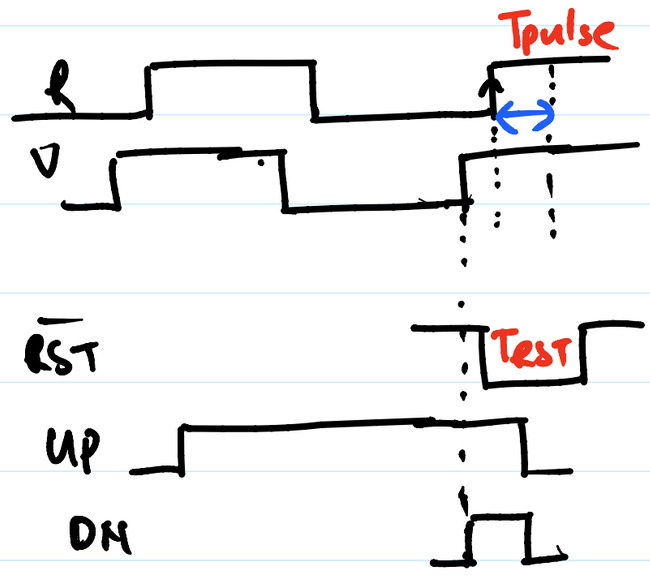




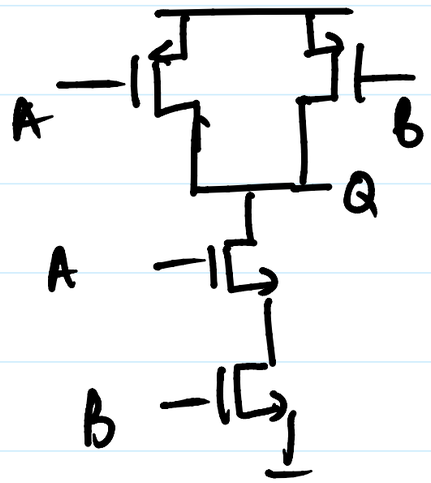




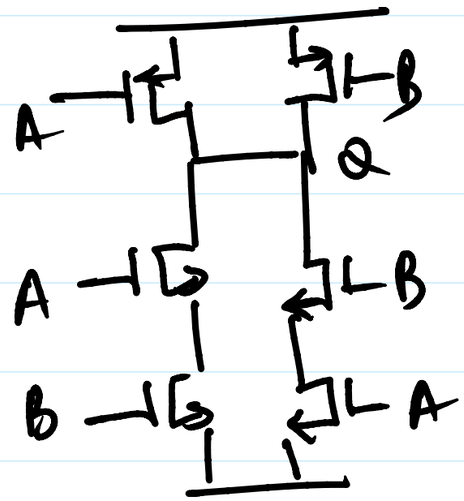




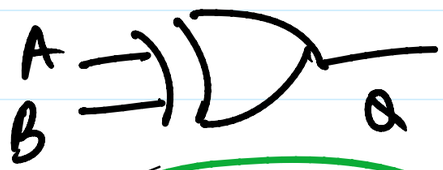
NAND Gate

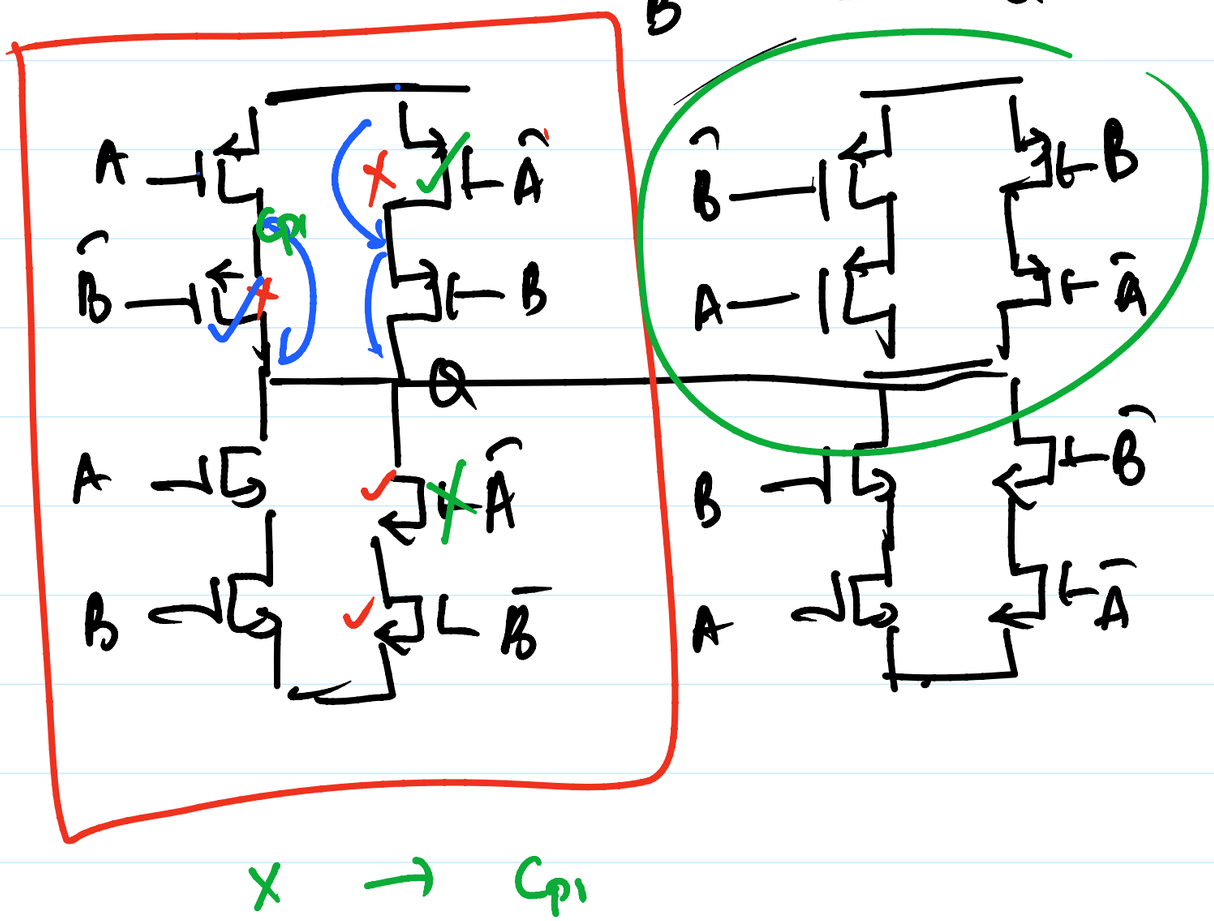


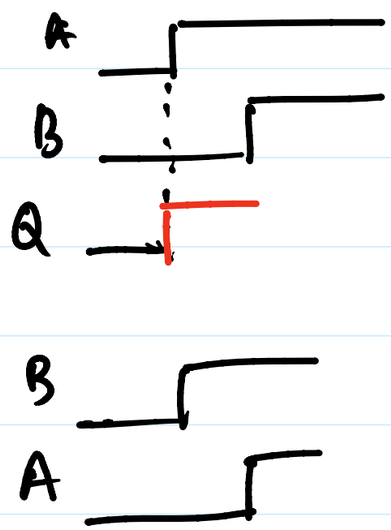
$td_{A \to Q} \neq td_{B \to Q}$



XOR gate







X → C_{p1}

$X_{1/2} + X_{1/2} \rightarrow C_{p_1} \& C_{p_1}$