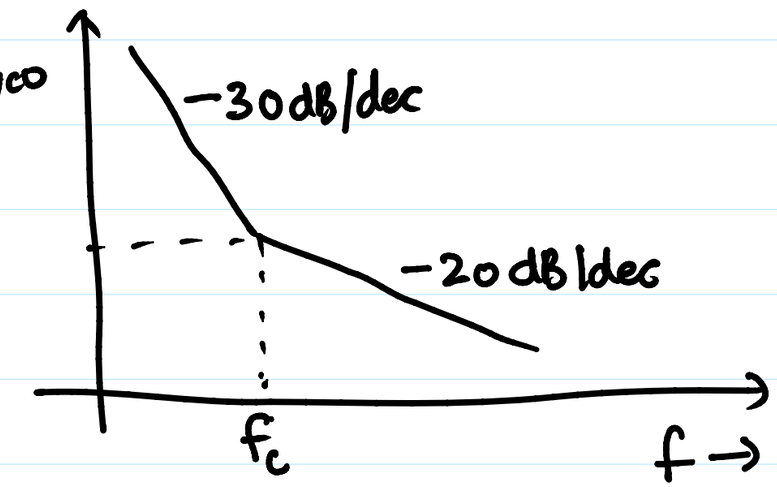
Lecture 15

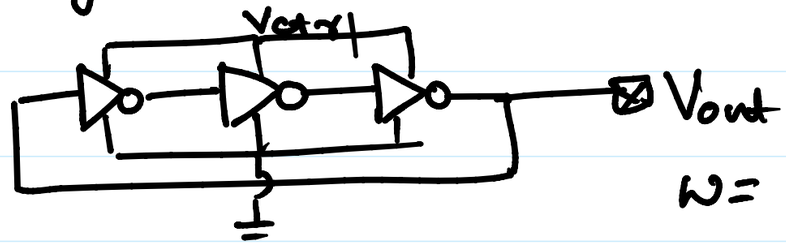
Thursday, February 9, 2017 10:38 AM

Noise Sources in CP-PLL

1. Charge pump
2. Resistor
3. Oscillator



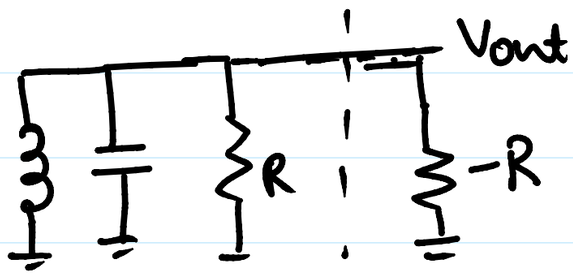
a) Ring oscillator



$$\omega = \frac{2\pi}{6 t_d}$$

t_d: delay of each inverter

b) LC - oscillators



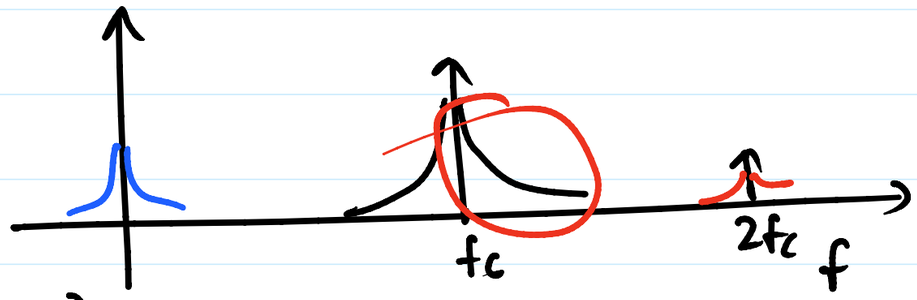
$$\omega = \frac{1}{\sqrt{LC}}$$

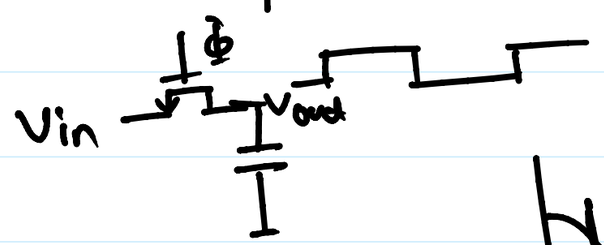
Phase Noise Simulation of Oscillator

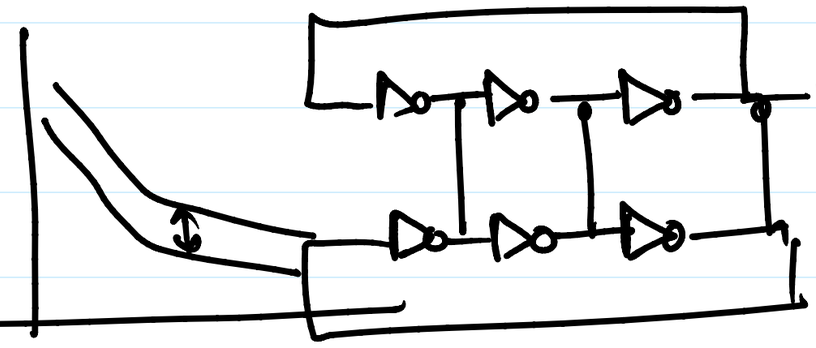
1) PSS (Periodic Steady State) Analysis

∴ f_0 o/p frequency of oscillator

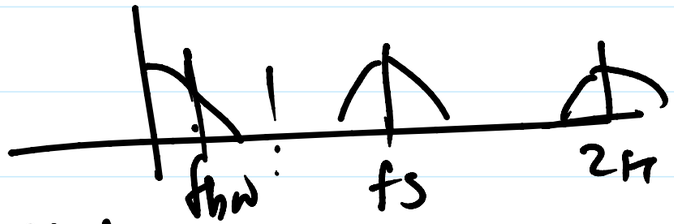
2) PNOISE







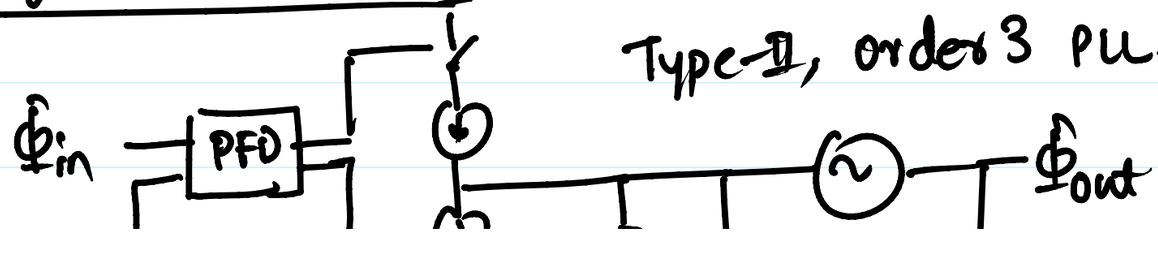
1mW
−90dBc/Hz @ 1MHz offset

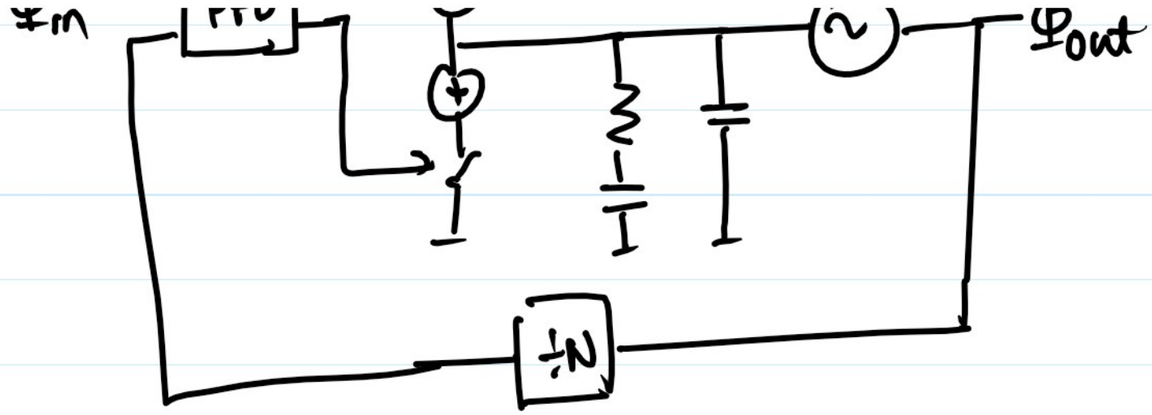


−93 dBc/Hz @ 1MHz
(2mW)

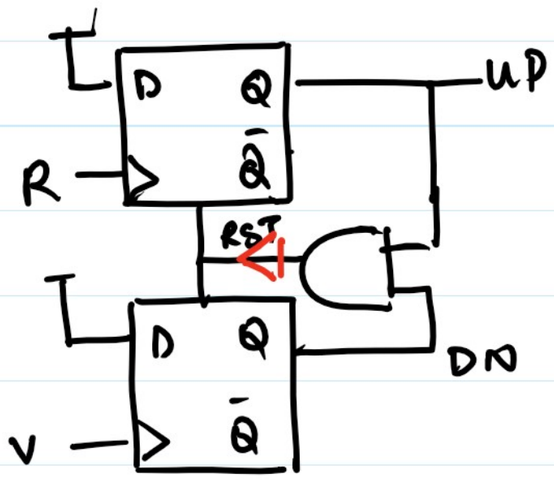
Building blocks of CP-PLL

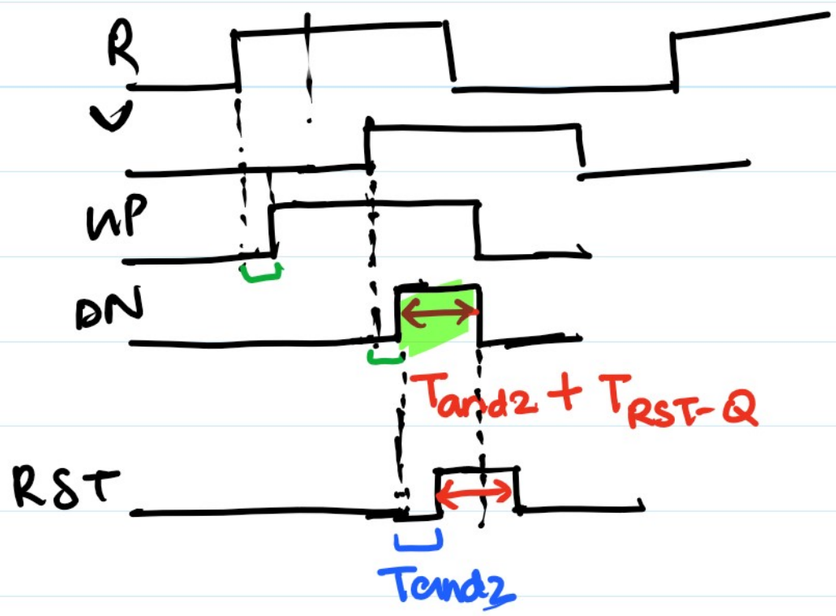
Type-II, order 3 PLL





1.) Phase frequency Detector (PFD)

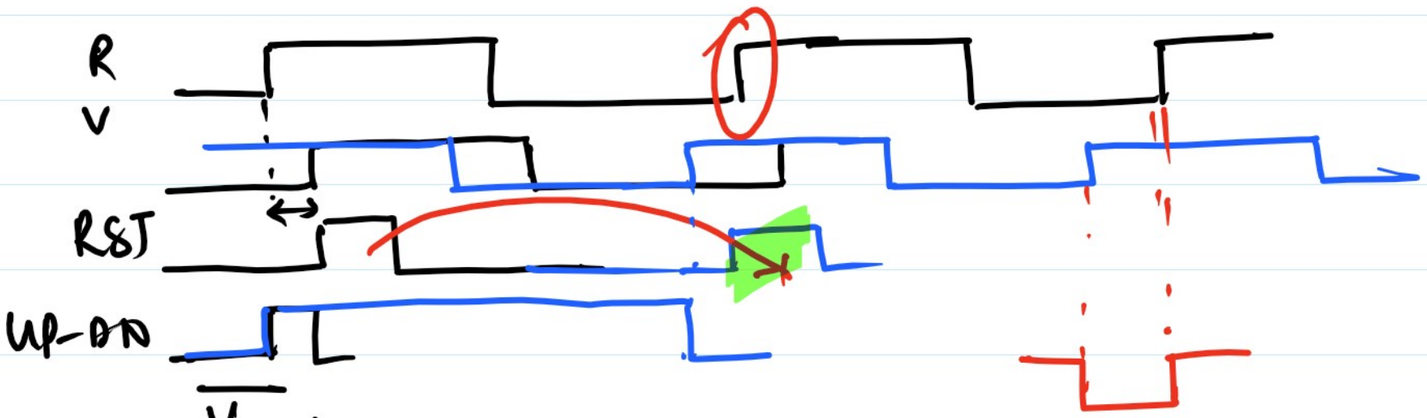


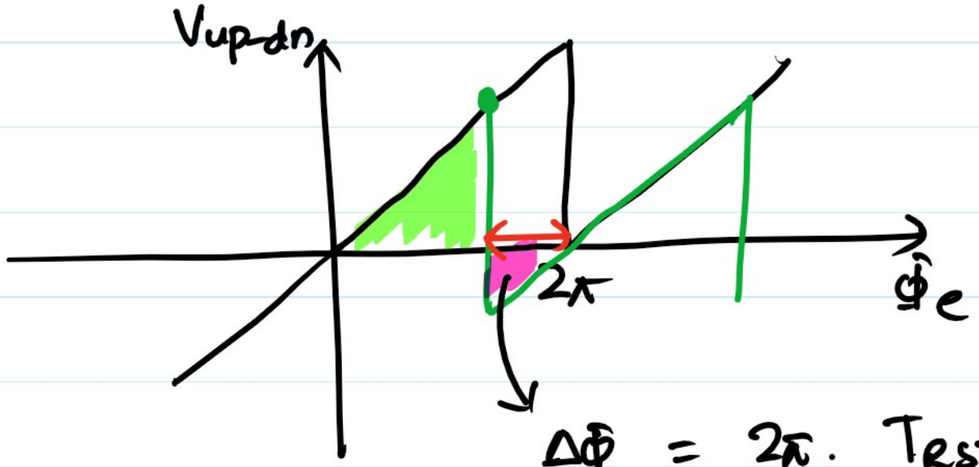


if $T_{ON} >$ $\pm T_{RST-Q}$

$$T_{ON} = T_{and2} + T_{RST-Q} + T_d = T_{OV}$$

$$T_{RST} = T_{and2} + T_{RST-Q} + T_d$$





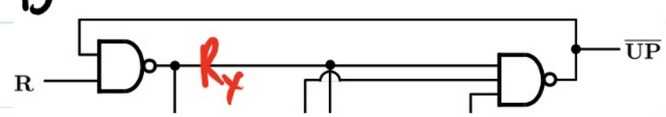
$$\Delta\Phi = 2\pi \cdot \frac{T_{RST}}{T_R} \quad ; \; T_R - \text{ref. period}$$

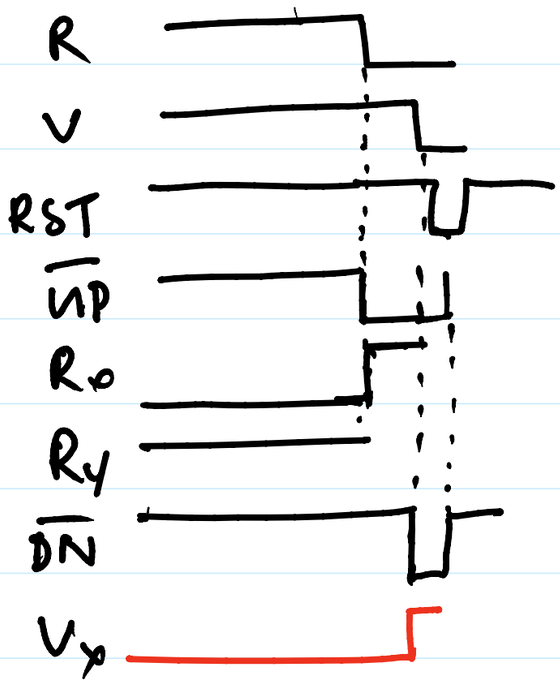
$$\Delta\phi < \pi$$

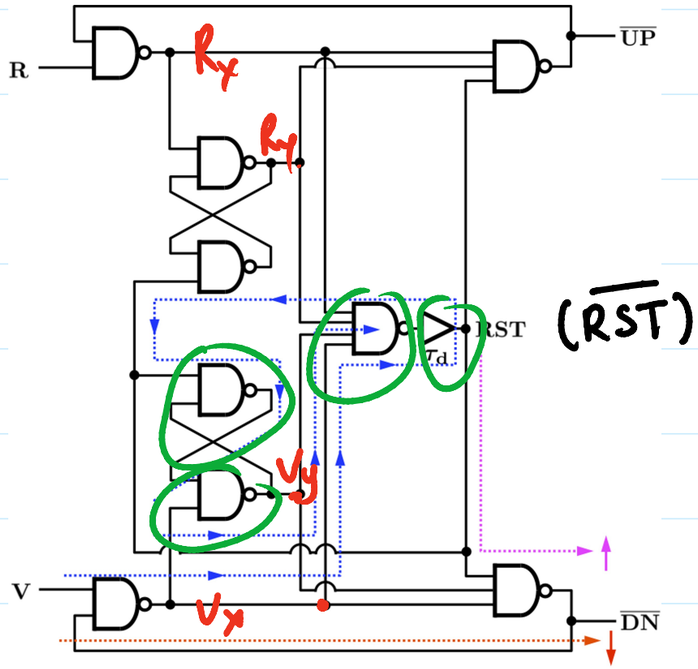
$$2\pi \cdot \frac{T_{RST}}{T_R} < \pi$$

$$f_{ref} = \frac{1}{T_R} < \frac{1}{2T_{RST}} \Rightarrow \text{limits operating freq. of PFD}$$

a) NANP based PFD







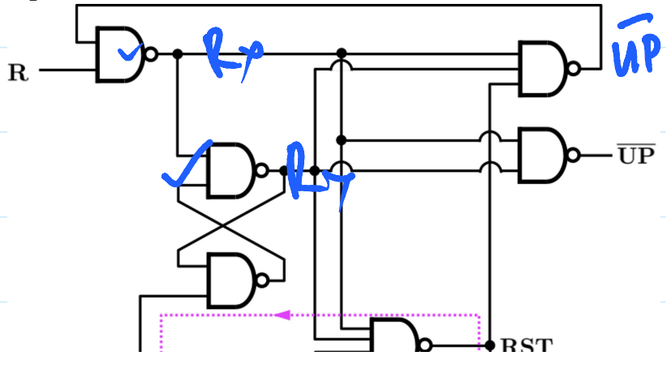
$(\overline{RST})$

$T_{OV} = T_{nand4} + \tau_d$

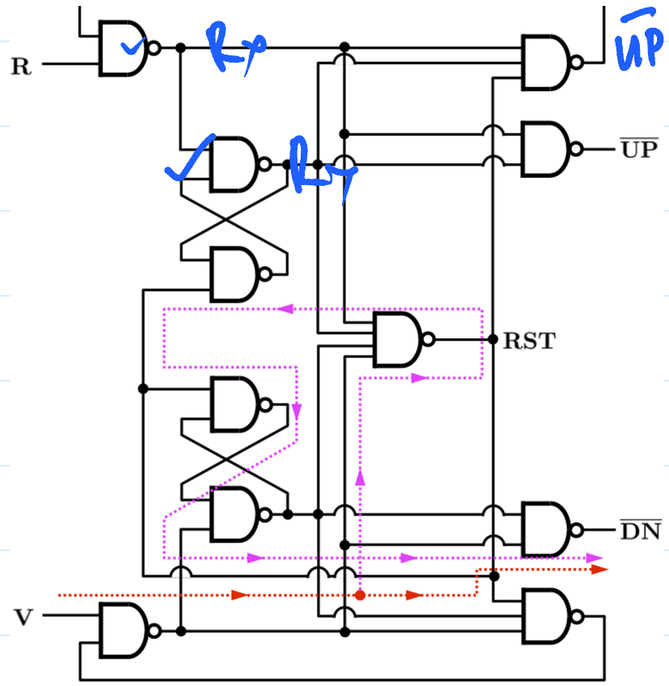
$T_{RST} = T_{nand4} + 2T_{nand2} + \tau_d$ (time for Reset signal to be low)

Ideally, $T_{OV} = T_{ON}$ (on time for CP- switches)

$T_{RST} = 0$



$T_{OV} = 2T_{nand2} + T_{nand4} + \tau_d$



$$T_{OV} = 2T_{nand_2} + T_{nand_4} + T_d$$