EE6324: Phase-Locked Loops D-Slot, Room: ESB 129

Instructor:	Saurabh Saxena, saurabh.saxena@ee.iitm.ac.in
Office:	ESB 245A, Ph: 4457
Office hours:	By appointment
Textbook:	No text book needed.
Prerequisites:	EE5320

Course Description: Emphasis is on developing intuition behind frequency synthesizer design, learning mathematical basis behind operation, and realizing PLLs at architecture and transistor level. Topics include integer/fractional-N phase-locked loops (PLLs), delay-locked loop (DLL), multiplying-DLL, injection-locked PLLs, and sub-sampled PLLs. Building blocks include phase/frequency detectors, charge-pump, LC/ring-oscillators, multi-modulus frequency dividers, active/passive loop-filter, etc.

Course Outline:

Week 1	Introduction; Basic concepts
Week 2	PLL type/order; Tracking; Acquistion
Week 3	Phase/Frequency Detectors; Charge-pump PLLs
Week 4	Loop components: Oscillators; Dividers
Week 5	Loop components: PFD; Charge-pump; Active loop-filter
Week 6	Noise analysis in PLLs
Week 7	Supply-regulated PLLs
Week 8	Self-biased & BW-tracking PLLs
Week 9	Delay-locked loop (DLL); Multiplying-DLL
Week 10	Digital PLLs
Week 11	Digital PLLs contd.
Week 12	Fractional-N PLLs
Week 13	Fractional-N PLLs contd.
Week 14	ILO-based PLL; Sub-sampled PLL
Week 15	Project Presentations

Important dates:

Quiz-I	21^{st} Feb.
Quiz-II	28^{th} Mar.
Project presentations	17-20^{th}Apr.
Project report	8^{th} May (9am)

Grading Policy:

Homework	20%
Quiz-I	20%
Quiz-II	20%
Project	40%

Reference books:

- F. Gardner, *Phaselock Techniques*, John Wiley & Sons, 2005.
- W. Egan, *Phase-Lock Basics*, John Wiley & Sons, 2008.
- R. Best, *Phase-Locked Loops : Design, Simulation, and Applications*, McGraw Hill, 2003.