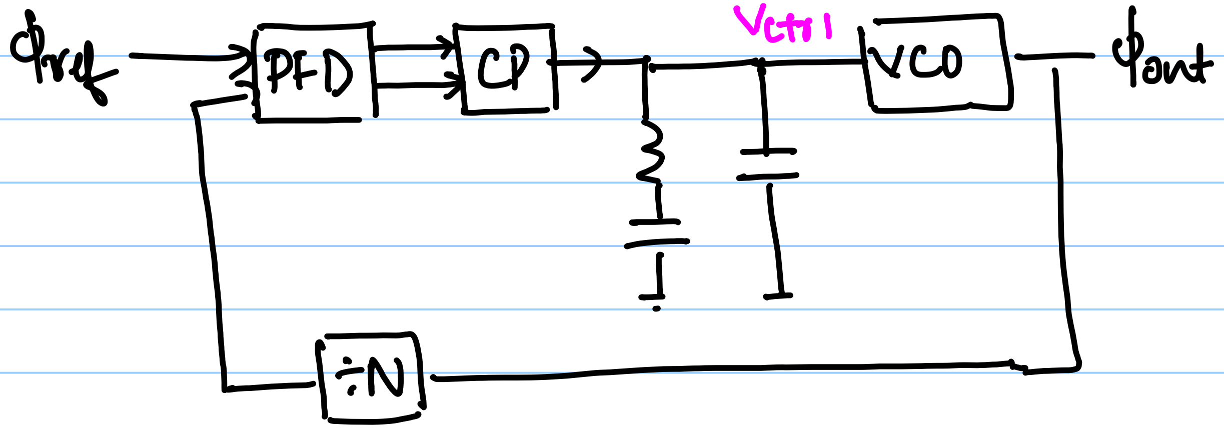
Note Title 23-10-2020

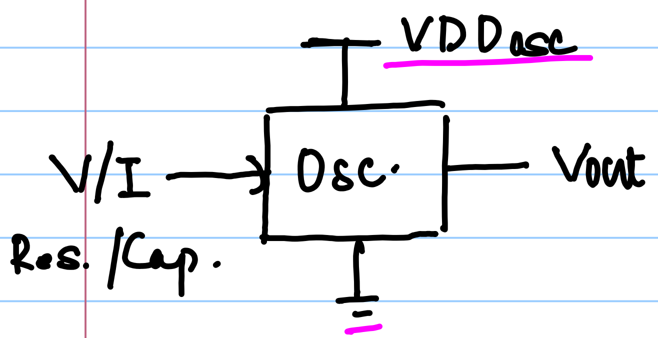
Lecture #24

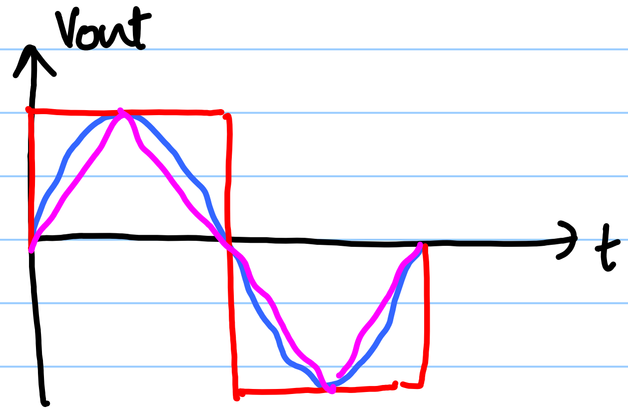
- PLL @ block-level
- Behavioral Simulations : Noise, loop-gain.



- Clock @ f_{out} using f_{ref}.
- Minimum jitter σ_{clock} ✓
- Minimum power cons. ✓
- Ref. spur

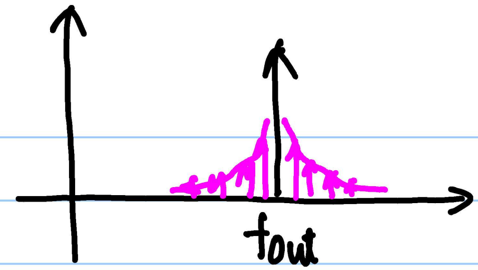
Voltage Controlled (Oscillator) :
Current Controlled





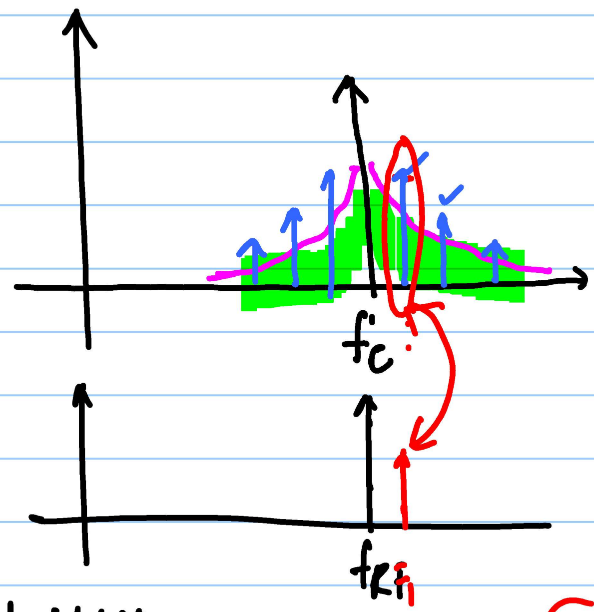
Crystal Oscillators.

$|\square| \to V_{out}\ (f_{out})$



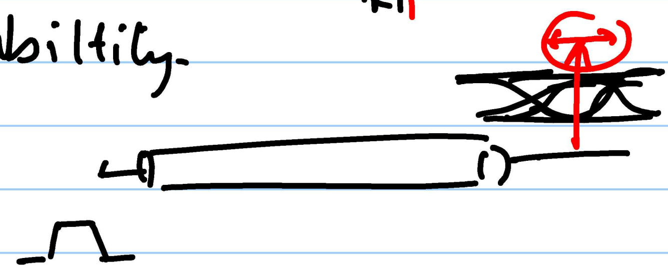
- low frequency.
- excellent freq. stability. $\left(\frac{\Delta F}{f_{osc}} \times 10^6\ (\text{ppm}) = 10 - 100\ \text{ppm}\right.$
- excellent phase noise
- can't be integrated on chip.

Tuned Oscillators (L&C)



- Clapp / Colpitts / Hartley oscillators
- Consume large area.
- Good phase noise, moderate frequency stability.

Ring Oscillator

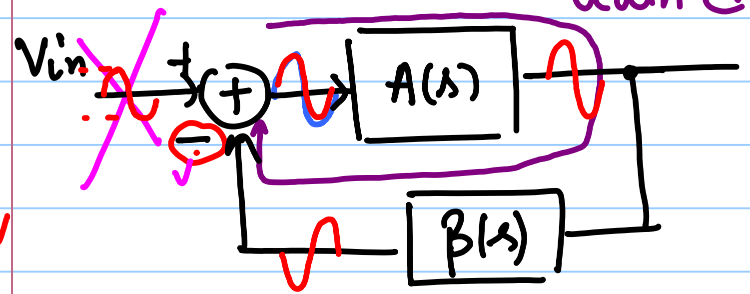


- Moderate phase noise
- Small area.

- RF.
- ADC/DAC
- Power Mang.
- Memory
- Processor

Gain @ $\omega_0 = 1$ and phase @ $\omega_0 = 180^\circ$ $\Rightarrow$ $|A(s)\beta(s)|_{\omega=\omega_0} = 1$

$\angle A(\omega_0)\beta(\omega_0) = 180^\circ$

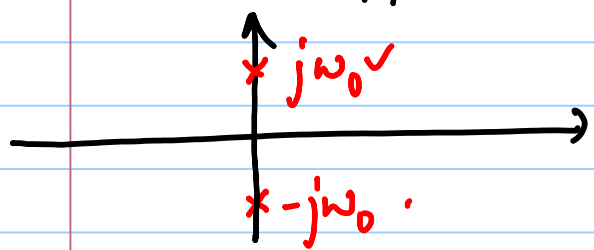


$$\frac{V_{out}}{V_{in}} = \frac{A(s)}{1 \pm A(s)\beta(s)} = H(s)$$

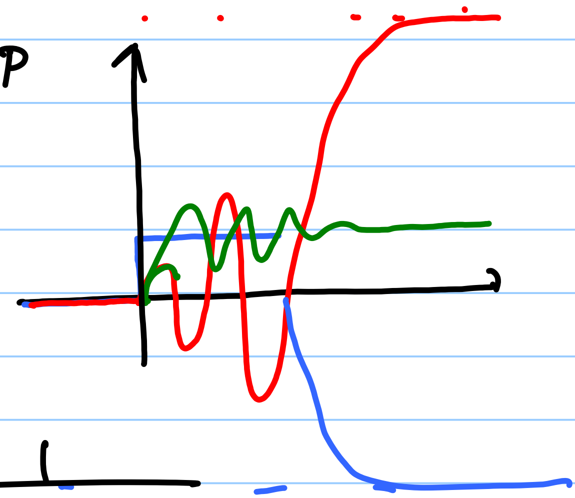
Above system is not stable if poles are in R.H.P

Above system is stable if poles in L.H.P

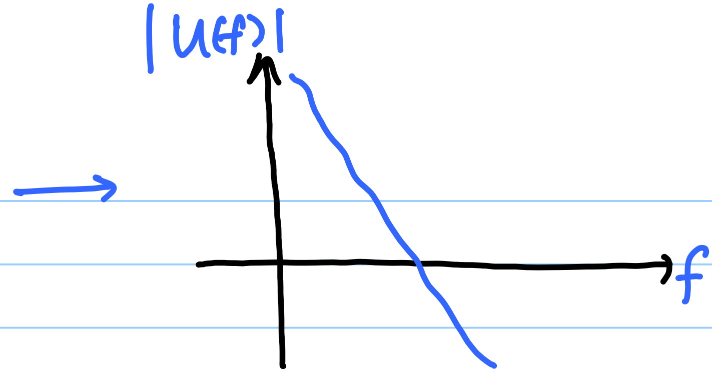
What happens if poles are on $j\omega$ axis.

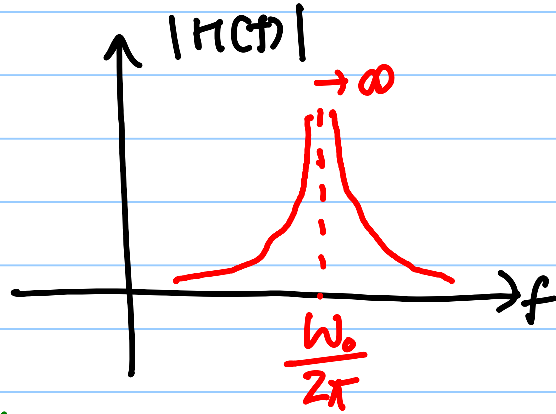


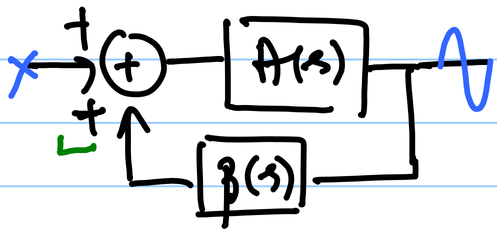
$$H(s) = \frac{1}{(s+j\omega_0)(s-j\omega_0)} = \frac{1}{s^2+\omega_0^2}$$



$$H(s) = \frac{1}{s^2 + \omega_0^2}$$







$$L_G(s) = A(s)\,\beta(s)$$

$$\begin{cases} |L_G(\omega)|_{\omega=\omega_0} = 1 \checkmark \\ \measuredangle L_G(\omega=\omega_0) = 2k\pi \checkmark \end{cases}$$

- Sustained oscillations. ✓
- Closed loop poles on $j\omega$ axis.