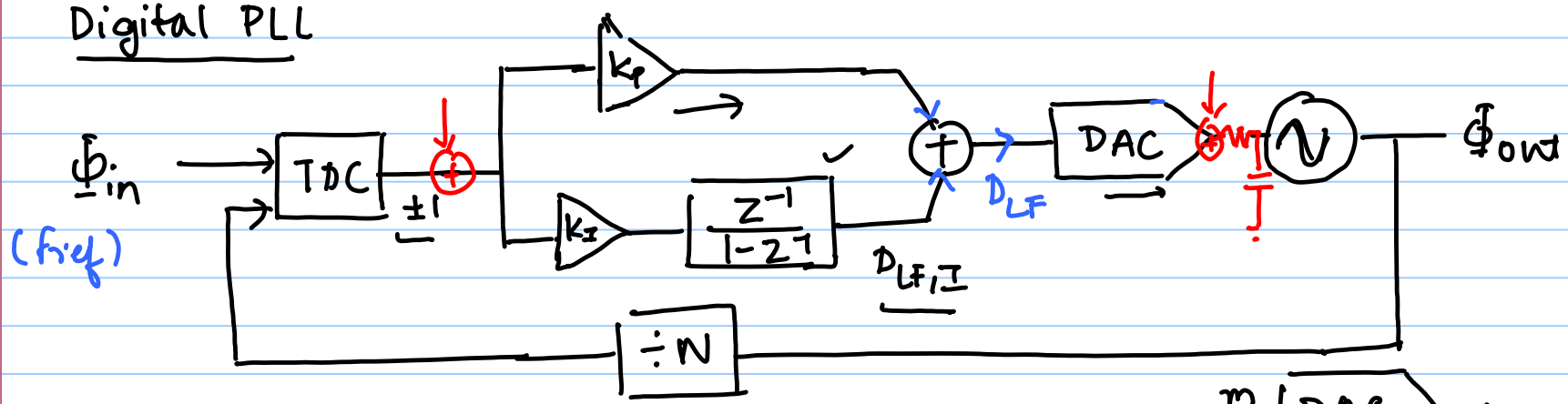
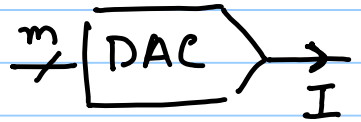
Lecture #43

Note Title 31-10-2018

Digital PLL





In steady state: $D_{LF,I}$ is fixed

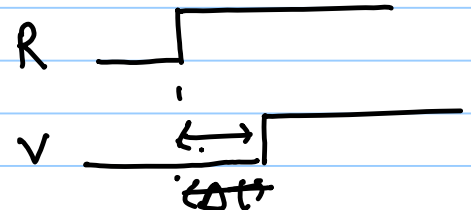
$D_{LF,P}$ vary @ fref

$$V_{out} = \sin\left(\omega_0 t + K_{VCO} \int i_{out}\, dt\right)$$

$$I_{out} = P \cdot (I_{LSB})$$

$$\pm X \times I_{LSB} = i_{out}$$

$$i_{out} = \pm TDC_{LSB} \times I_{LSB} \times K_P$$



Analog PLL : Δt

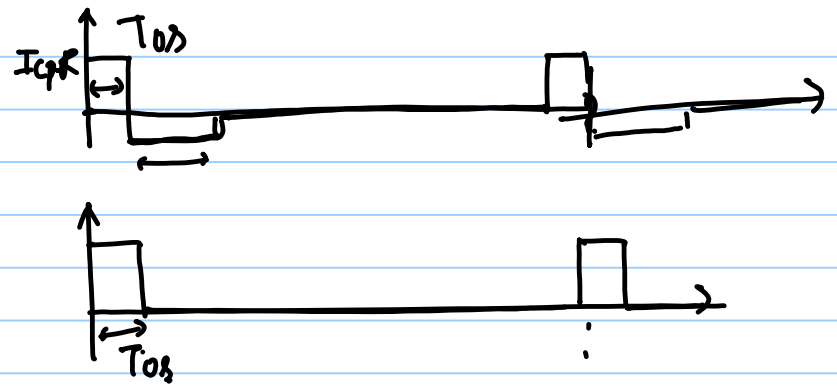
Digital PLL : $P \cdot TDC_{LSB}$

✓ I_{LSB} ↓

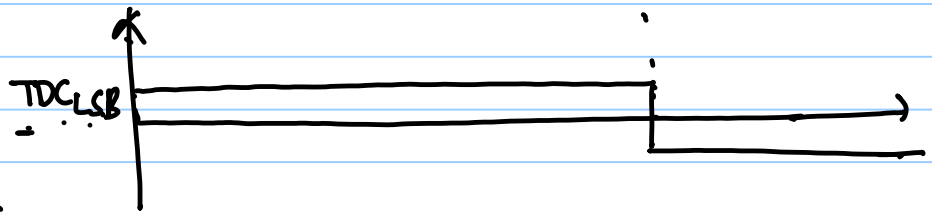
large cap. (Area problem)

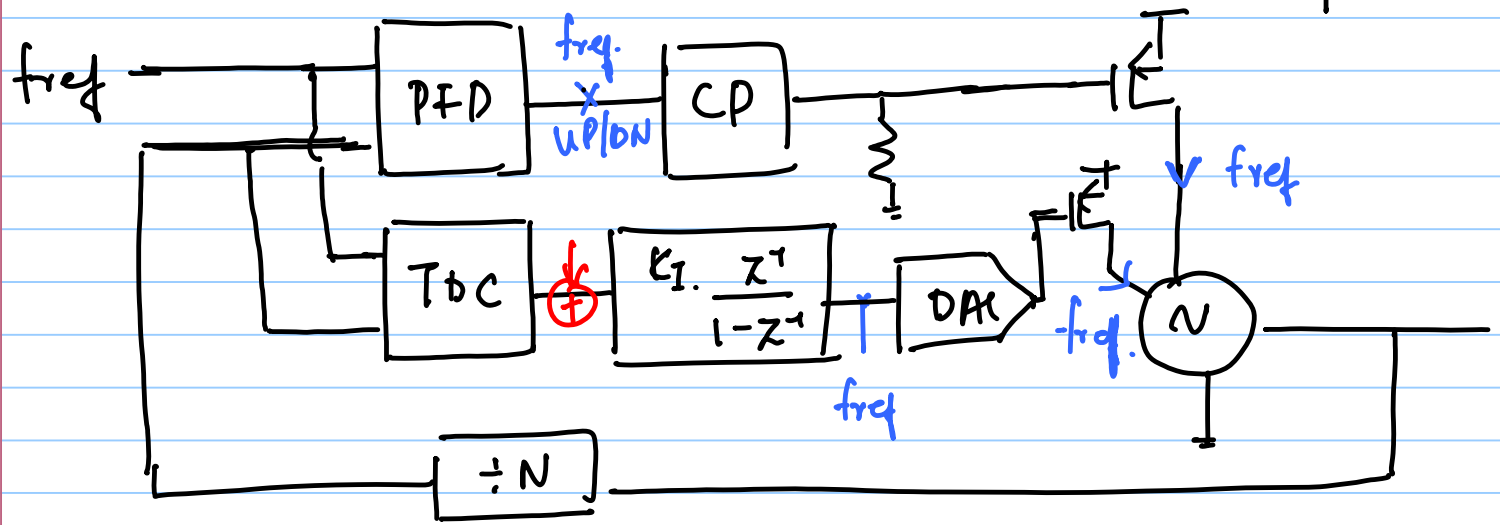
DAC $\xrightarrow{I_{LSB}\downarrow}$ # of cells, → Large DAC area

Analog PLL



Digital PLL



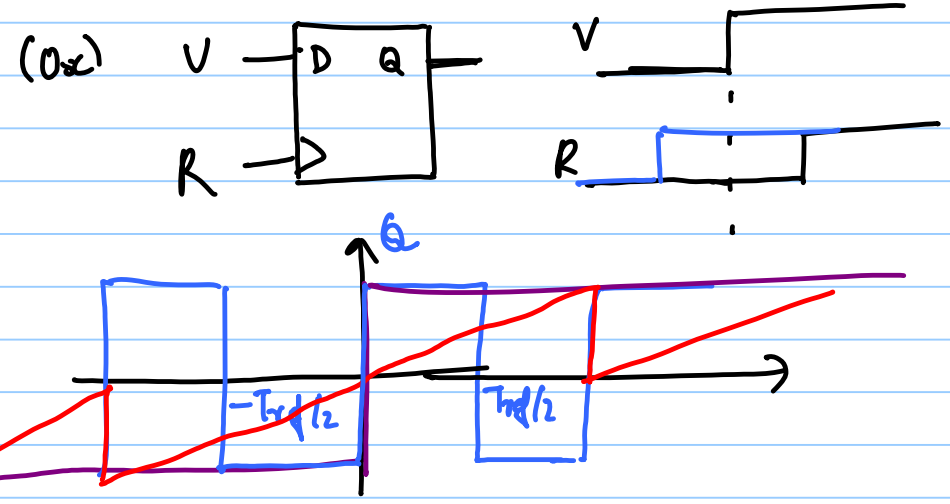


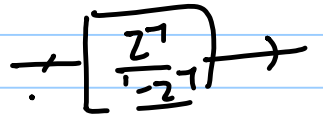
TDC:

fine resolution — # of delay cells (n-bits) $\frac{T_{ref}}{2^n}$

coarse resolution — quantization.

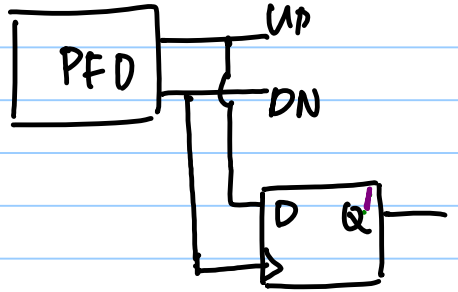
1-bit TDC

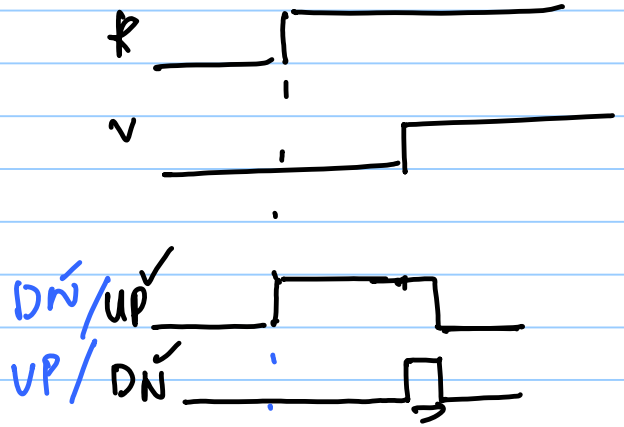




1 1000x Tref = 1000

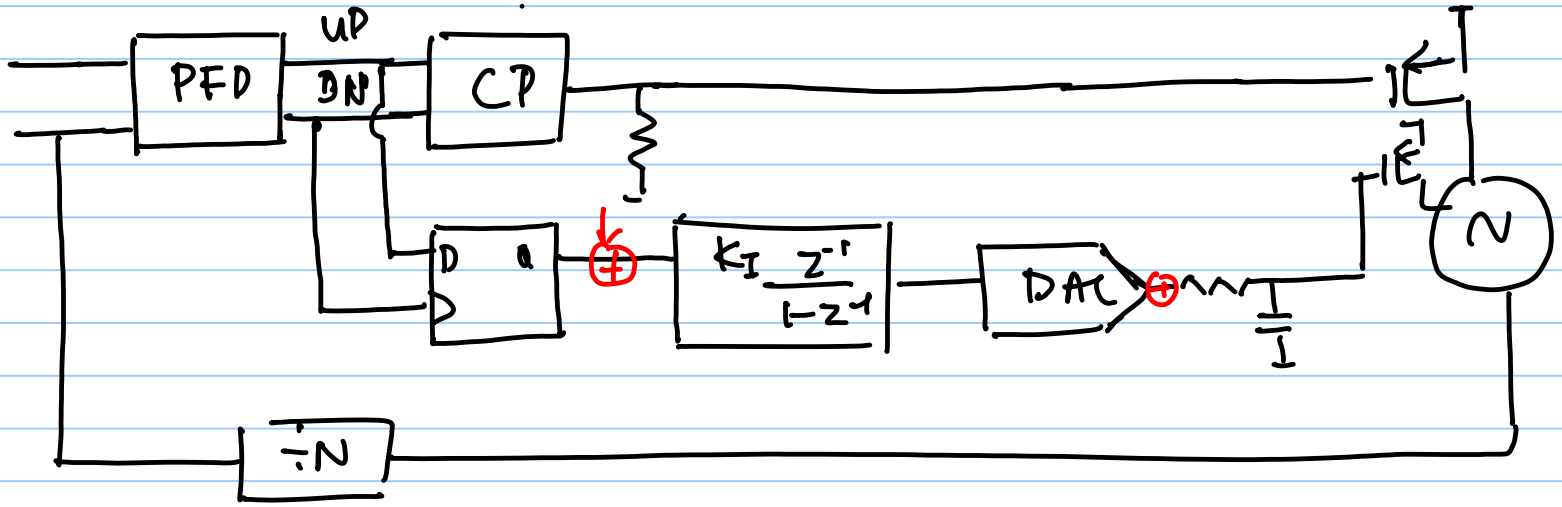
10 100x Tref = 1000

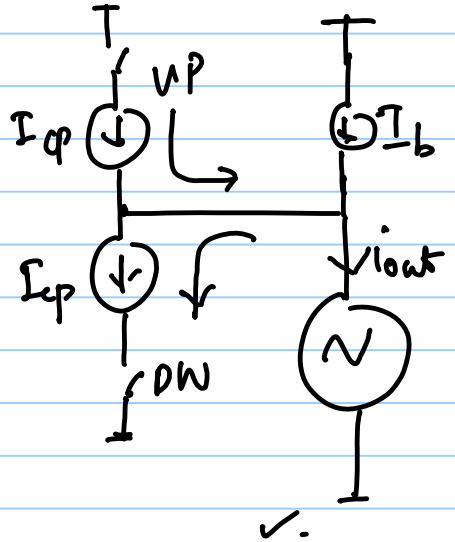


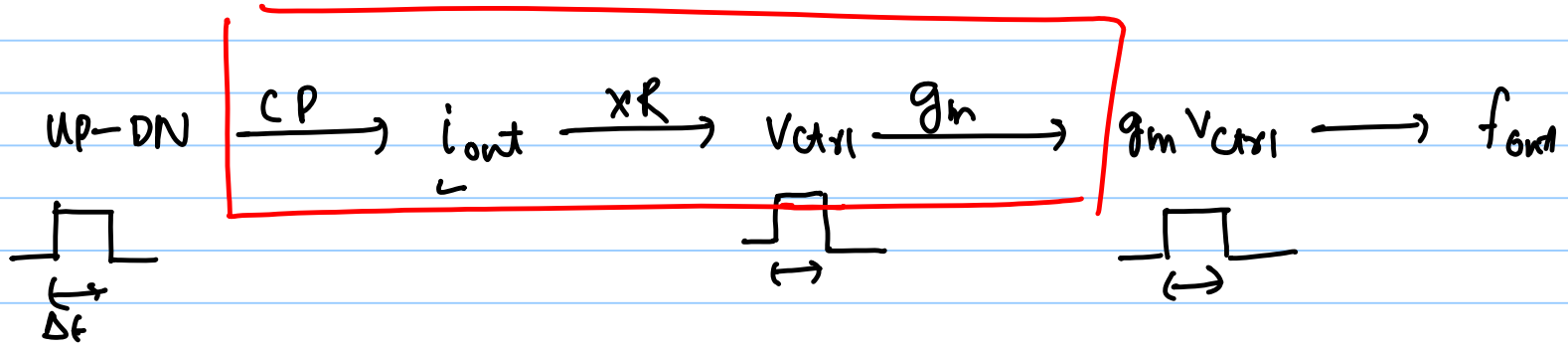


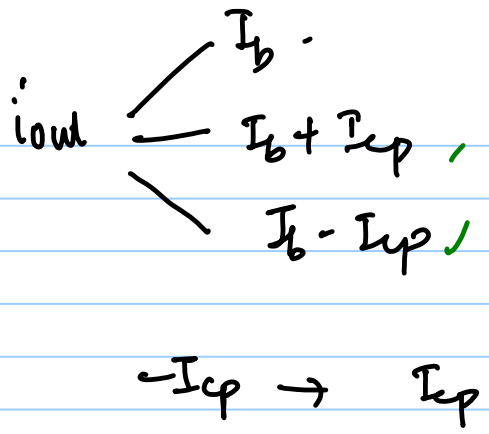
PFD
UP
DN
D
CP
$K_I \frac{z^{-1}}{1-z^{-1}}$
DAC
z^{-1}
VCO

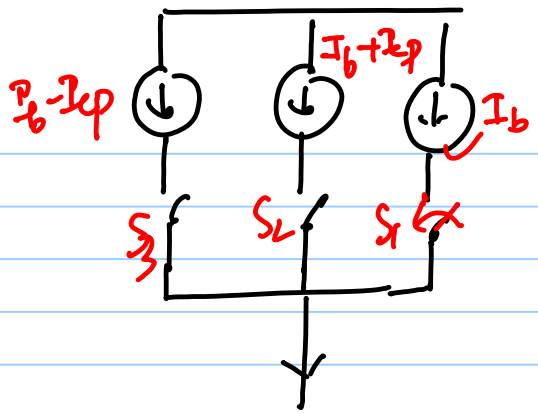
Φ

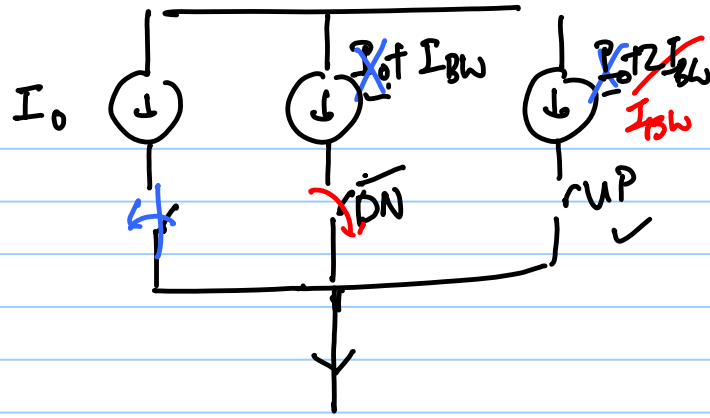

PFD
UP
DN
CP
D
Q
$K_I \frac{z^{-1}}{1-z^{-1}}$
DAC
÷N


T
UP
I_{cp}
I_b
I_{cp}
i_{out}
DN


UP−DN
CP
i_{out}
×R
V_{Ctrl}
g_m
$g_m V_{Ctrl}$
f_{out}
Δt







$0 \rightarrow 2I_{BW}$

I_0 ✓ $\quad -I_{BW}$

$I_0 + I_{BW} \rightarrow I_b$ ✓

$I_0 + 2I_{BW} \rightarrow I_{BW}$