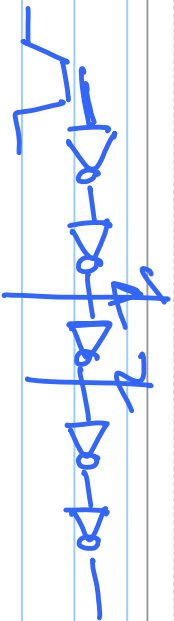


Lecture # 37.

Digital cells

$I_p < I_n$



$$\frac{W_p}{L_p} = \frac{0.68 \mu m}{0.18 \mu m}$$

$$I_p = \mu_p C_{ox} \frac{W}{L} \left((V_{sc} - V_{th}) V_{SD} - \frac{V_{SD}^2}{2} \right)$$

$$\frac{W_n}{L_n} = \frac{0.24 \mu m}{0.18 \mu m}$$

$$I_p = \mu_p C_{ox} \frac{W}{2L} (V_{sc} - |V_{tn}|)^2$$

cubic \rightarrow sub-threshold \rightarrow saturation \rightarrow linear.

NMOS : $\frac{W}{L} = \frac{0.24 \mu m}{0.18 \mu m}$

$L_{min} = 0.18$

12-16% clock period.



trise / fall = 26-36%
10-96%

trise \rightarrow tfall

trise-fall-del = tfall-rise-del trise-fall delay W_p : 0.24 $\mu m \rightarrow$ + 0.18 μm

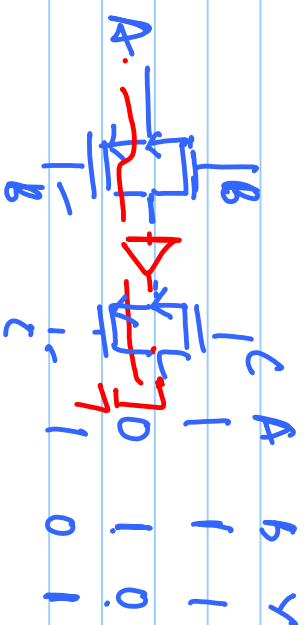
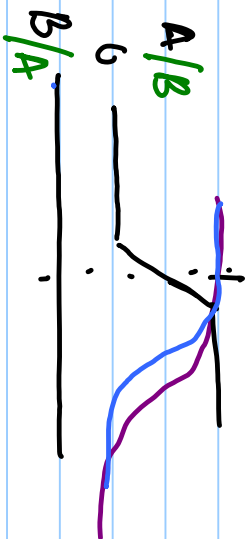
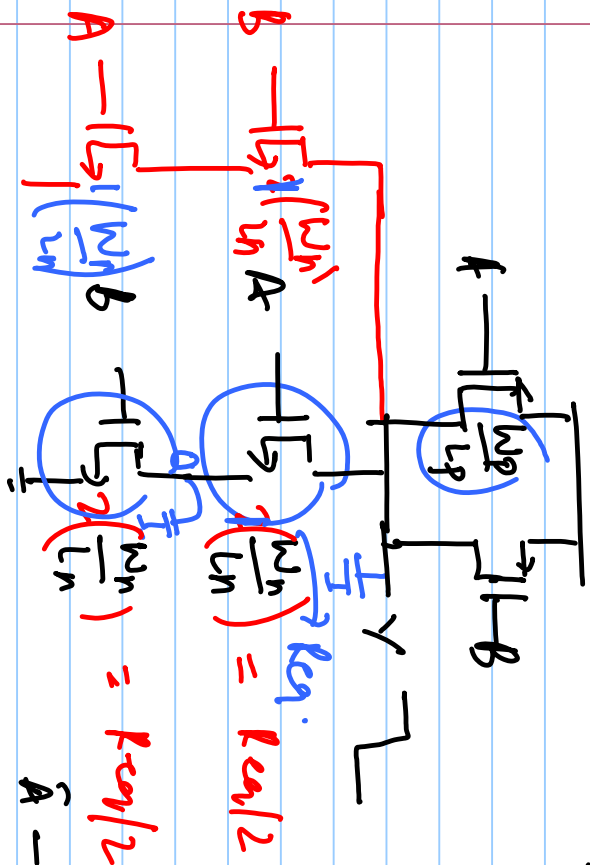
Nand Gate $Y = A \cdot B$

$$\frac{W_n}{L_n} = \frac{0.24}{0.18}$$

$R_{eq} = R_{nmos}$

$$\frac{W_p}{L_p} = \frac{0.68}{0.18}$$

$R_{eq} = R_{pmos} = R_{nmos}$



$$Y = A\bar{B} + \bar{A}B$$

$$Y = A\bar{B} + \bar{A}B \checkmark$$

