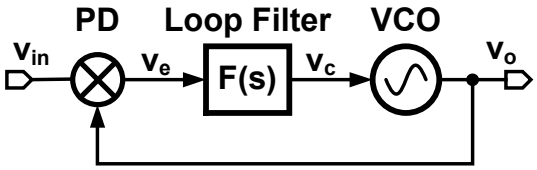
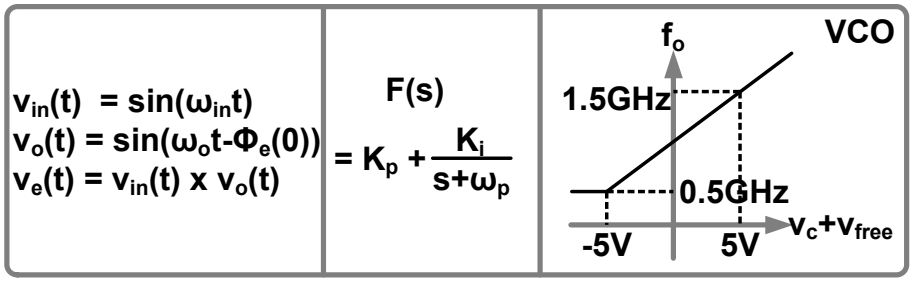
Assignment: #3

Due Date: 5:00PM, Sep. 8, 2017

PROBLEM 1. Phase and frequency acquisition in Type-II PLL.
Consider a Type-II PLL with real integrator as shown below. v_{free} is external bias voltage. Loop filter F(s) has a proportional path gain $K_p = 10$ and integral path gain $K_i = 1.2566 \times 10^9$ with $\omega_p = 12.566\,\text{Mrad/s}$. Let $f_{in} = 1.0\,\text{GHz}$.

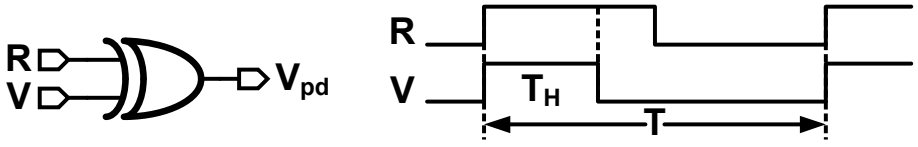




(a) Evaluate lock-in range, pull-in range, and hold-in range of the PLL with loop filter as described above.

(b) Model the above PLL at behavioral level and simulate while demonstrating PLL's behavior near lock-in, pull-in, and hold-in ranges. Plot the control voltage (v_c) for frequency errors near lock-in/pull-in/hold-in range. (Hint: To observe the lock-in/pull-in/hold-in behavior you may need to simulate PLL over a range of frequency errors around the calculated frequency range.)

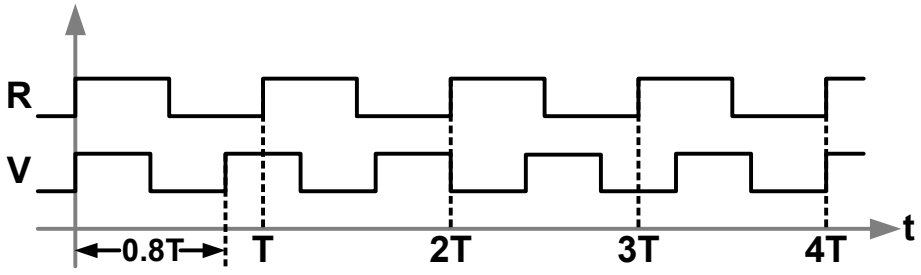
PROBLEM 2. Phase Error Detector
XOR-based phase error detector with inputs R and V is shown below.



(a) Find average phase error detector output ($\overline{V_{pd}}$) as a function of phase error.

(b) Plot $\overline{V_{pd}}$ vs. phase error, Φ_{er}, between R and V.

PROBLEM 3. Frequency Error Detector
Input signals R and V of a XOR-based phase error detector are shown below. R and V have 50% duty cycle and different frequencies.

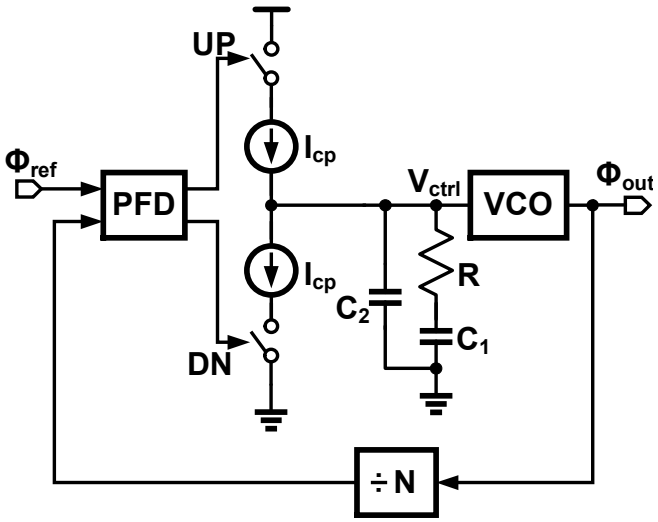


(a) Plot phase error detector output vs. time.

(b) Find the average value of phase error detector output.

(c) Find the average value of 3-state PFD output with same inputs R and V as shown above.

PROBLEM 4. Charge-pump PLL
Block diagram of a charge-pump PLL is shown below. The PLL has reference frequency f_{ref} = 40 MHz, N = 64, and VCO gain K_{vco} = 100 MHz/V.



(a) Find and plot magnitude and phase of open loop gain of the PLL.

(b) Find and plot magnitude and phase of closed loop gain (Φ_{out}/Φ_{ref}) of the PLL.