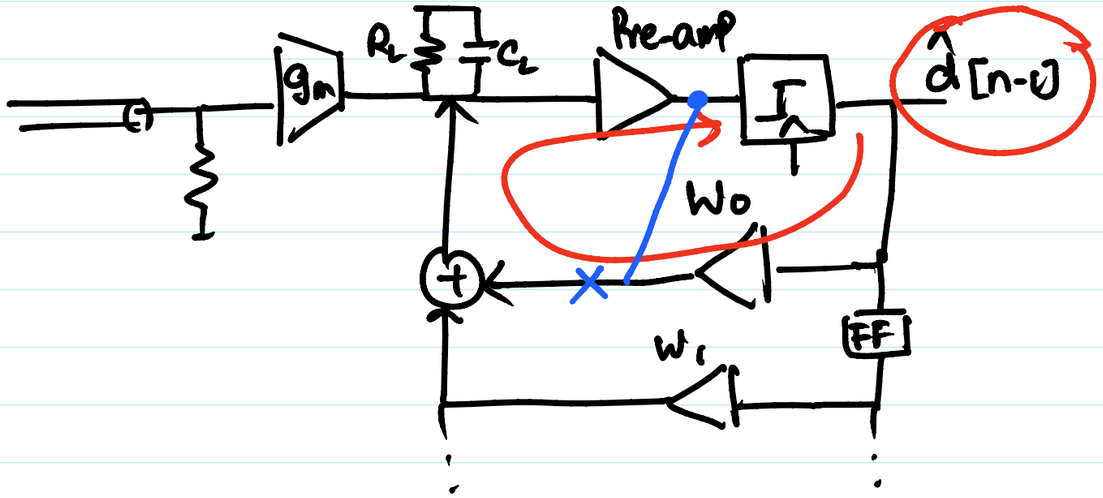
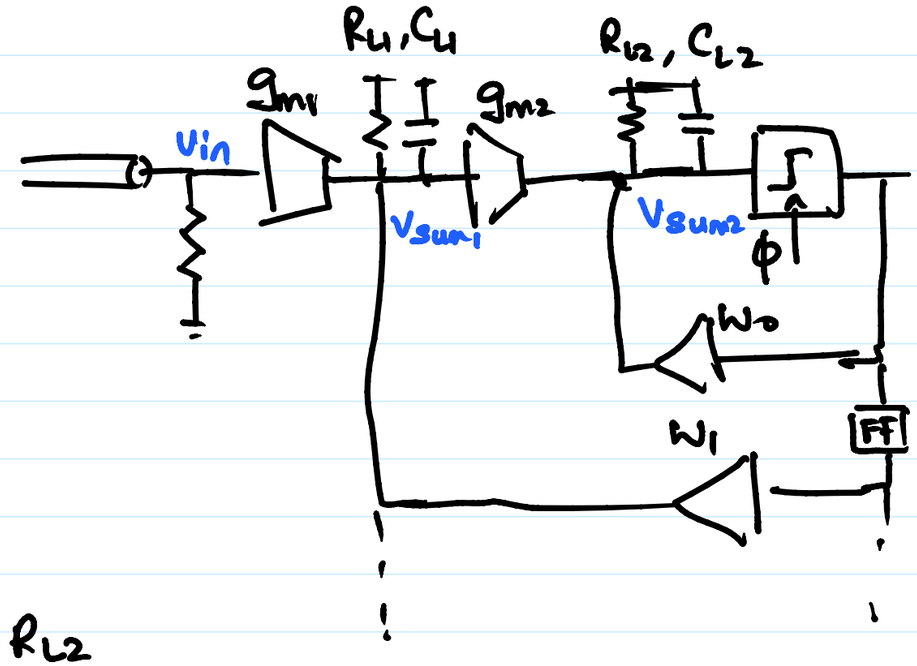
Lecture 45

Thursday, November 3, 2016 10:56 AM

DFE Implementation w/ faster 1st tap loop.





$$V_{sum2} = \left(g_{m2} V_{sum1} - I_{DFE1} \right) \frac{R_{L2}}{1+sC_{L2}R_{L2}}$$

$$= \left(g_{m2} \left(\underbrace{g_{m1} V_{in}}_{V_{cursor}+V_{ISI}} - I_{DFEx} \right) \frac{R_{L1}}{1+sC_{L1}R_{L1}} - I_{DFE1} \right) \frac{R_{L2}}{1+sC_{L2}R_{L2}}$$

$$= g_{m2} g_{m1} V_{cursor} \frac{R_{L1}}{1+sC_{L1}R_{L1}} \times \frac{R_{L2}}{1+sC_{L2}R_{L2}}$$

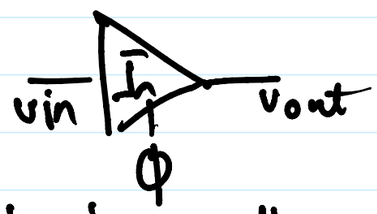
$$g_{m2} \left(g_{m1} V_{ISI} - I_{DFEx} \right) \frac{R_{L1}}{1+sC_{L1}R_{L1}} - I_{DFE1} = 0$$

After settling, $g_{m2} g_{m1} V_{ISI} R_{L1} - g_{m2} R_{L1} I_{DFEx} - I_{DFE1} = 0$

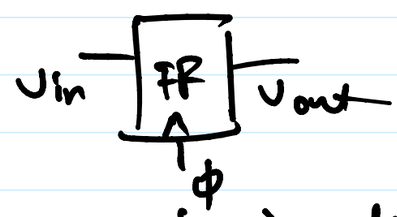
* C_{L2} = i/p capacitance of comp. + o/p cap. of pre-amp + o/p summing tap.

* C_{L1} = i/p cap. of pre-amp + o/p cap. of g_{m1} + (N-1) tap. of each tap.

* time constant of pre-amp $\tau_{pre\text{-}amp} = R_{L2}C_{L2} < \tau_{sum\text{-}node} = R_{L1}C_{L1}$

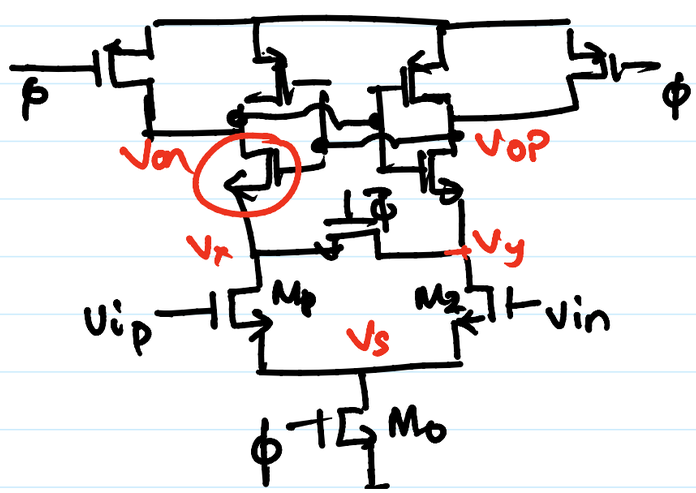


vin is small analog i/p

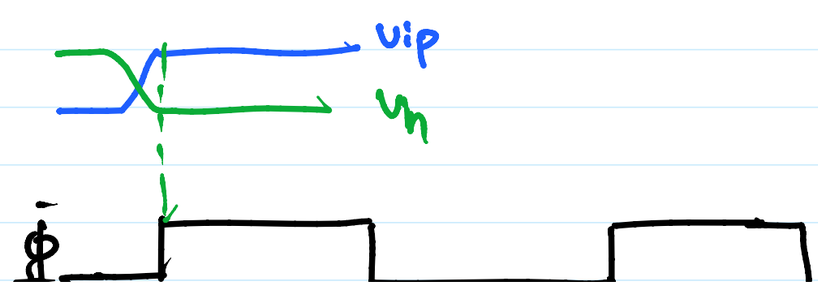


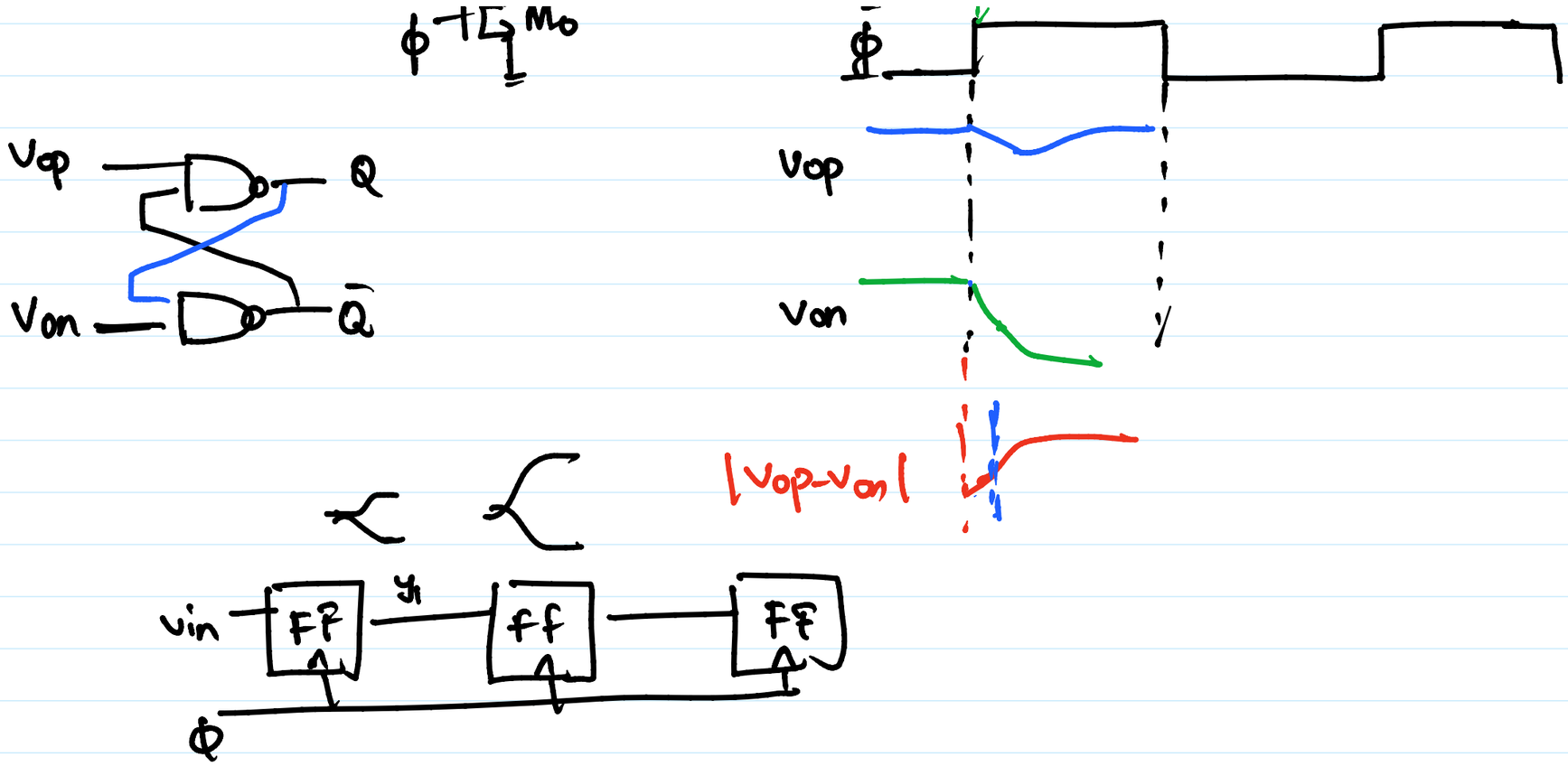
vin is digital (full swing) i/p

Sense-Amplifier based ff.



Φ	VOP	Von
0	VDD	VDD

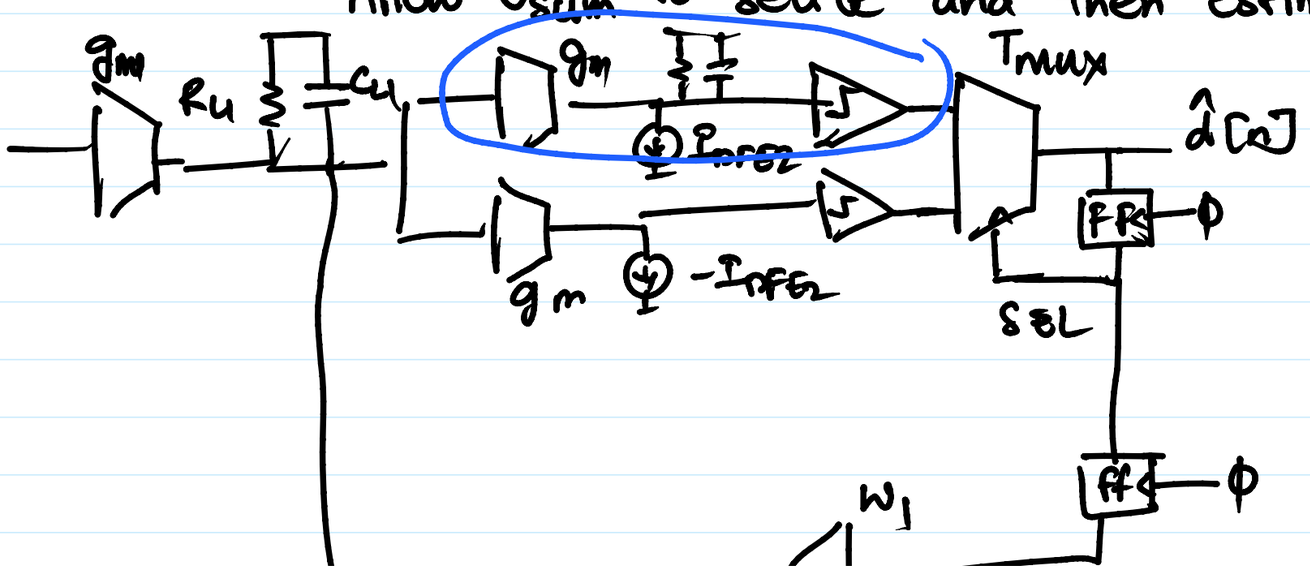




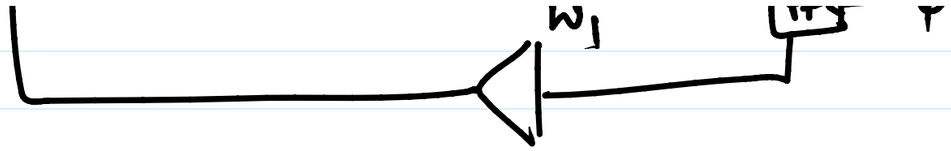
DFE — Take a decision on V_{sum} at $\bar{\phi}$ ($\hat{d}[n-1]$)

Add or sub $\pm I_{DFE}$ from V_{sum} for following bit

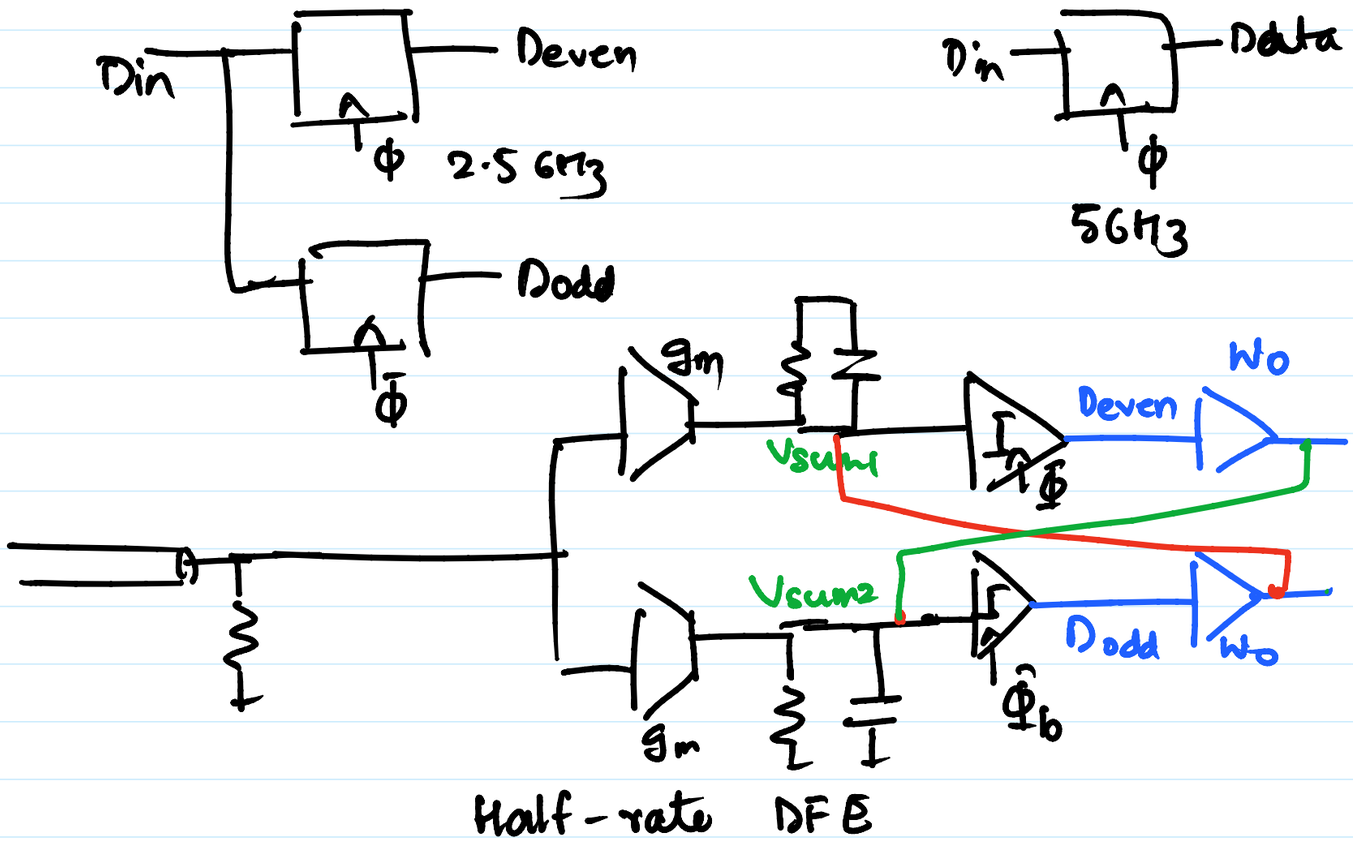
Allow V_{sum} to settle and then estimate next bit



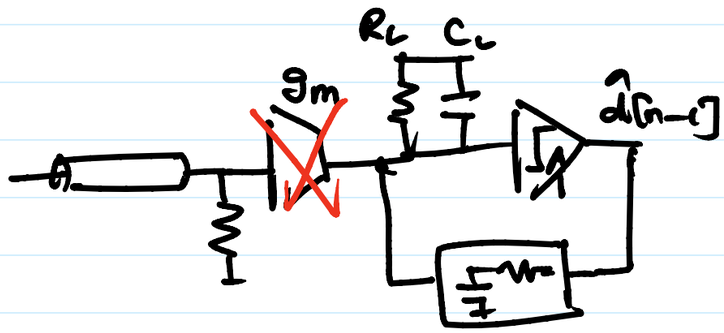
Loop unrolled DFE



$T_{CK-Q} + T_{settle} + T_{set-up} < 1$ bit period.



IIR – DFE



$e^{-t/RC}$