Lecture 39

Monday, October 24, 2016 9:59 AM

Lecture 39

Equalization in VM o/p driver

1.) Varying conductance linearly w.r.t output swing
   - Non-linear and increased power

2) Varying conductance non-linearly w.r.t o/p swing
   - Constant current consumption $V_{DD}/4R_T$

3) Varying conductance linearly w.r.t o/p swing
   - non-linear but proportional to o/p swing power consu

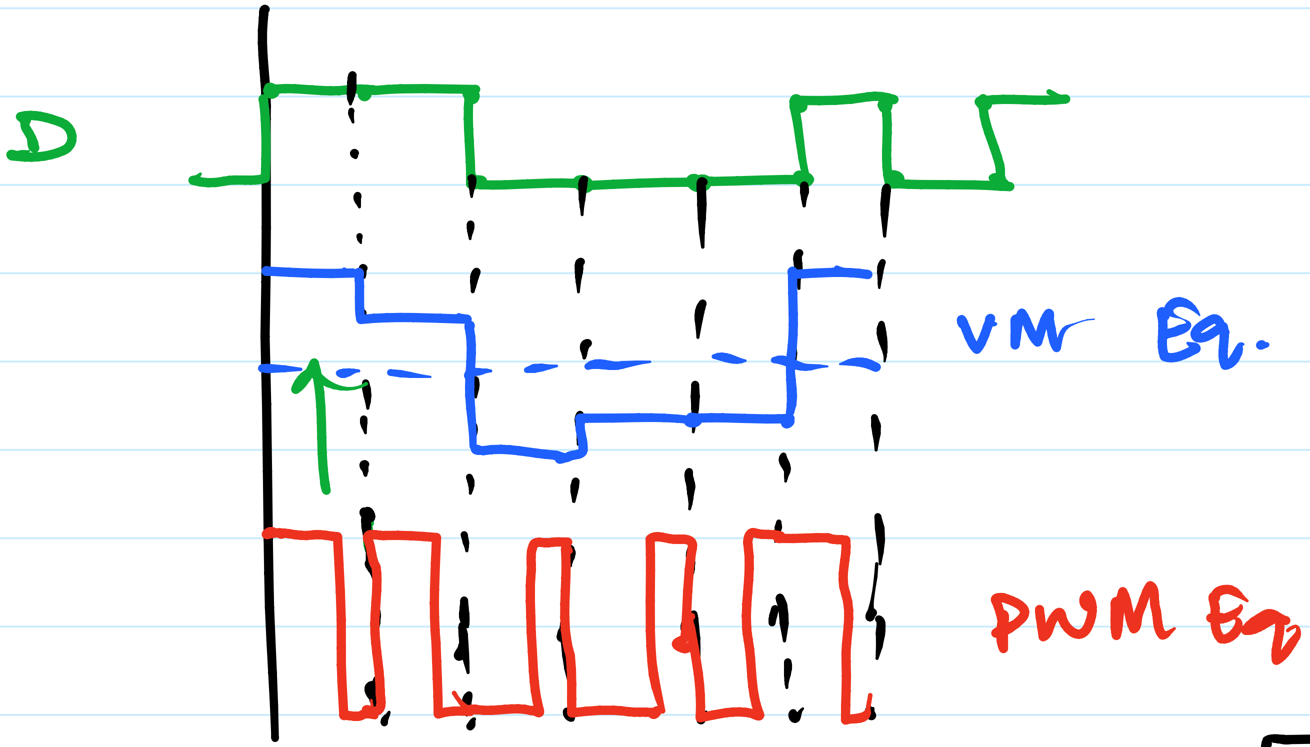
4) PWM (time-based) equalization
   - directly proportional to o/p swing.

Non-linear variation in conduction ⇒ More power consumption

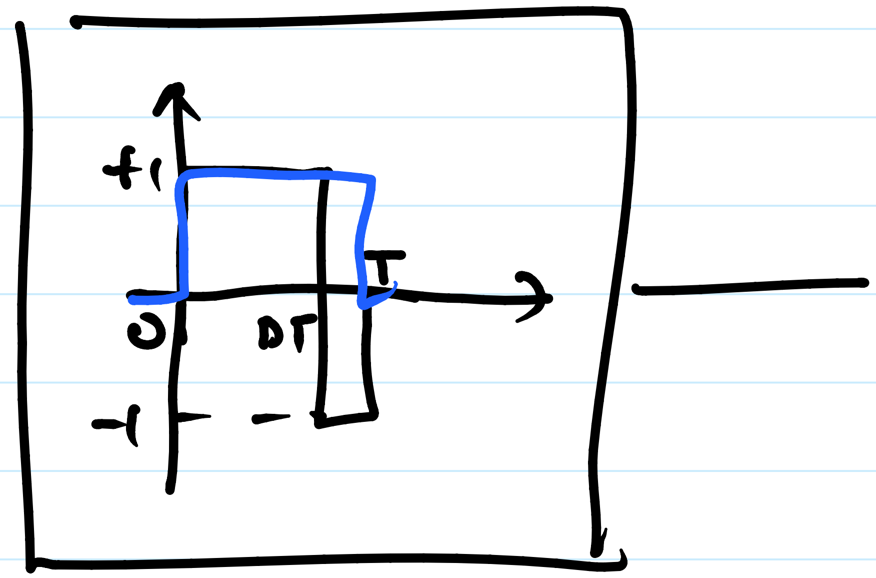
mption

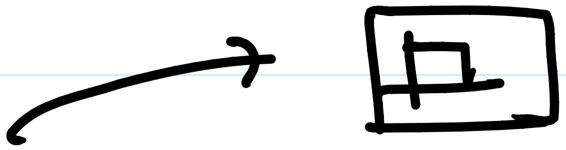
in pre-driver

$$h_{eq}(n) = 0.8\,\delta(n) - 0.2\,\delta(n-1)$$



d[n]





VM eq, $y(n) = d[n] * h_{eq}(n) = 0.8\,d[n] - 0.2\,d[n-1]$

$h_{eq}(n) \downarrow$ $0.8\,\delta(n) - 0.2\,\delta(n-1)$

$$y(t) = \left(0.8\,d[n] - 0.2\,d[n-1]\right) * p(t)$$ — $u(t) - u(t$

T bit

$$y(t) = \sum_{k=} \left(0.8\,d[k] - 0.2\,d[k-1]\right) p(t - kT)$$

$nT \le t$

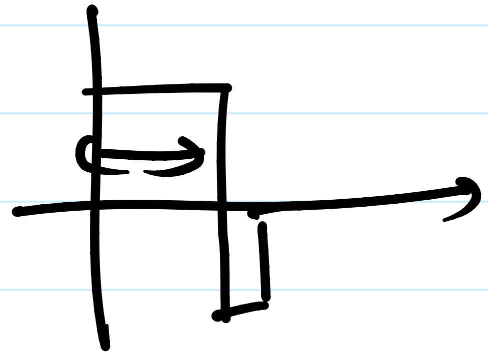
$-T)$

period

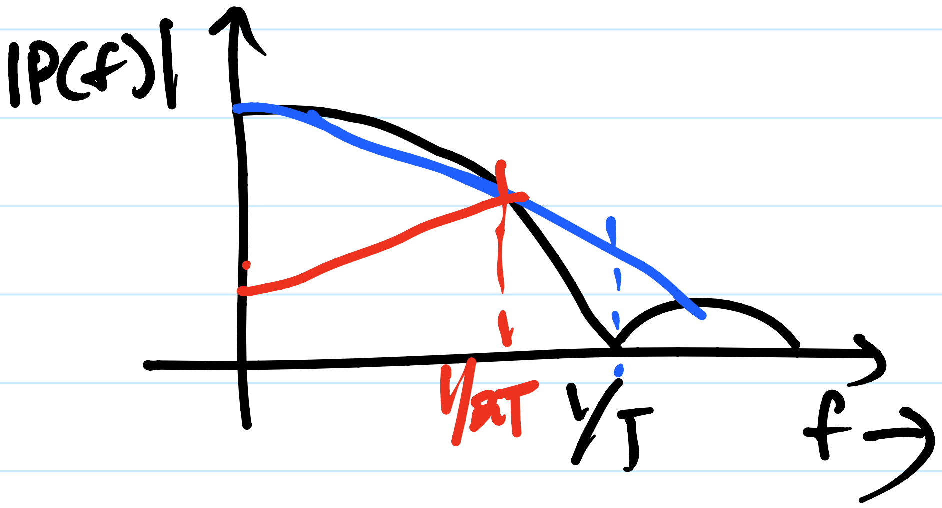
$<(n+1)\,T$

$$p(t) = \left(u(t) - u(t-DT) \right) - \left(u(t-DT) - u(t-T) \right)$$

$$= u(t) - 2u(t-DT) + u(t-T)$$



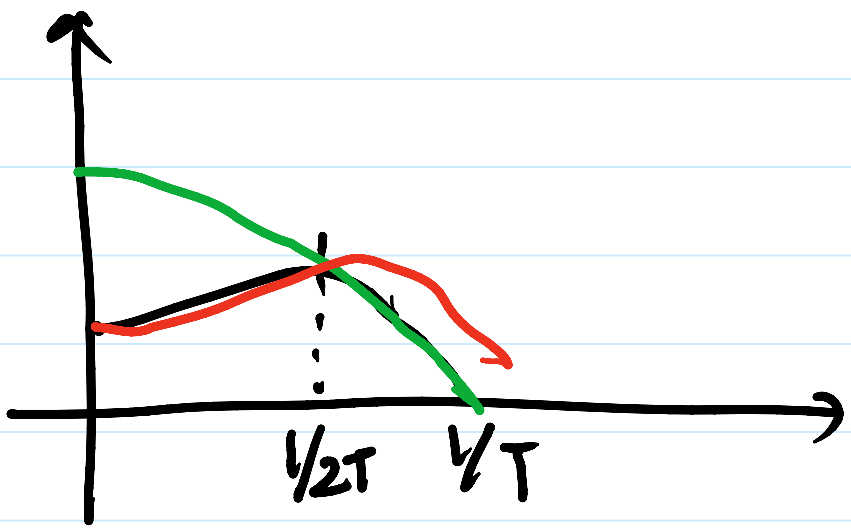
$$y(t) = d[nT] * p(t)$$



NRZ — $u(t) - u(t-T) = p(t$

$P(f)$ = sinc

PWM — $u(t) - 2u(t-DT) +$



FIR-2 / PWM ('D' duty cy

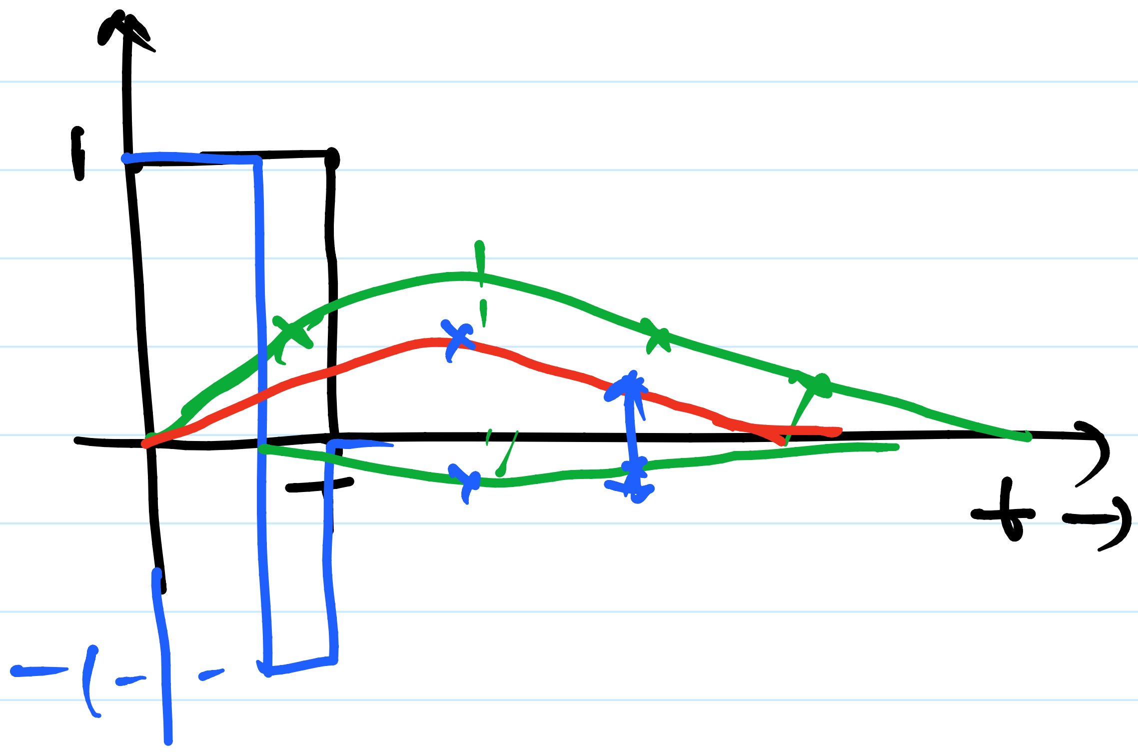
2 taps — Move loss

Main Cursor + Pre or Post

)

$u(t-T) = p(t)$

ycle control)
compensation.



$$H_{ch}(z) = 1+\alpha z^{-1}$$

$$H_{eq}(z) = \frac{1}{1+\alpha z^{-1}} , \quad y_{Tx}(n) = d[n] * h_{eq}(n)$$

$\max[y_{Tx}(n)]$ is limited by suppl

$$y_{Tx}(n) = \sum d[k]\, h_{eq}(n-k)$$

$$H_{eq}(z) = (1+\alpha z^{-1})^{-1} = \sum (-1)^k \alpha^k z^{-k}$$

$$h_{eq}(n) = \sum (-1)^k \alpha^k \delta(n-k) \qquad \Rightarrow y_{Tx}(n) = \sum (-$$

y voltage

$)^{k} \alpha^{k} \, d[n-k]$

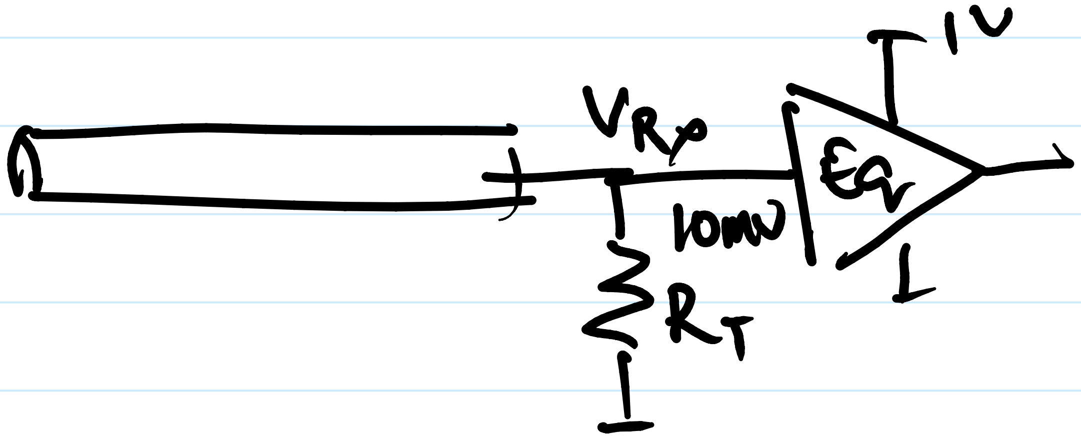
$$\max.(y_{Tx}(n)) = \sum |(-1)^k| \, |\alpha^k| = \sum \alpha^k = \frac{\quad}{1-}$$

$$y_{Tx}(n) = V_{sup} \frac{1}{1/(1-\alpha)} \sum d[k] \, h_{eq}(n-k)$$

$$y_{Rx}(n) = y_{Tx}(n) * h_{ch}(n)$$

$$= (1-\alpha) V_{sup}$$

⇒ Supply limit actuall



Pre-emphasis — inc
a

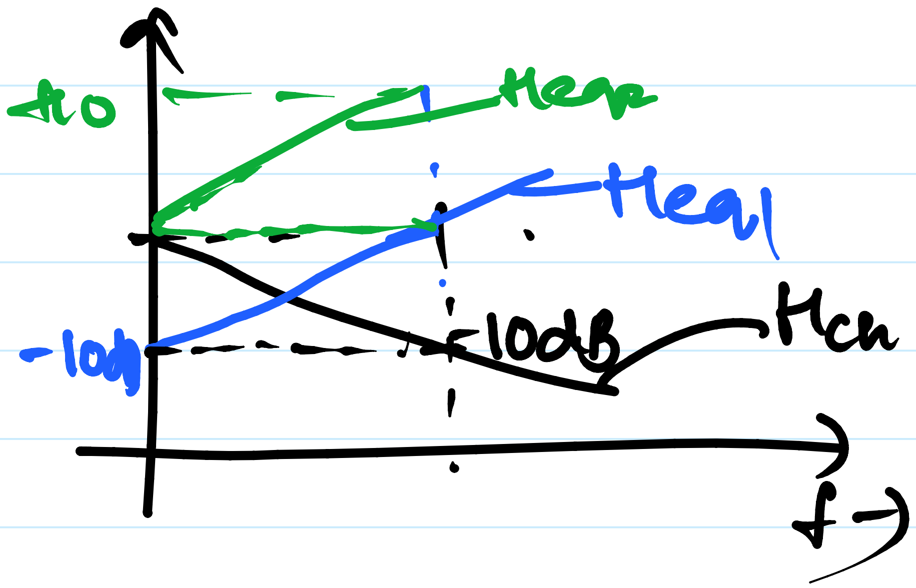
De-emphasis — de

$\frac{1}{\alpha}$

y lowers received
signal swing.

reased signal amp.
fter eq.

ecreased signal amp

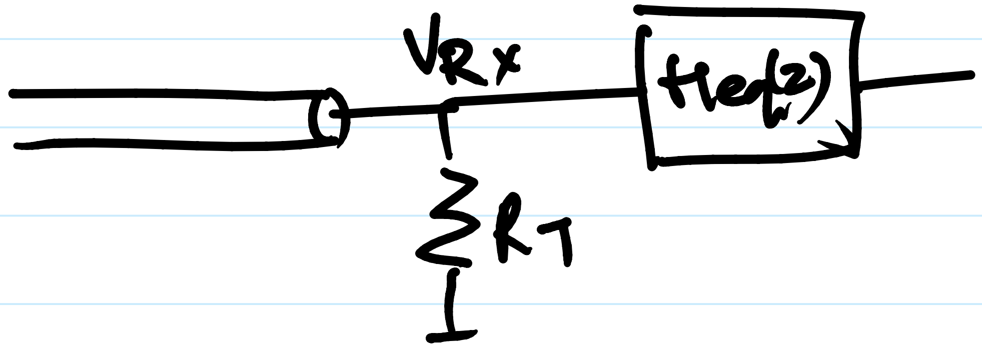


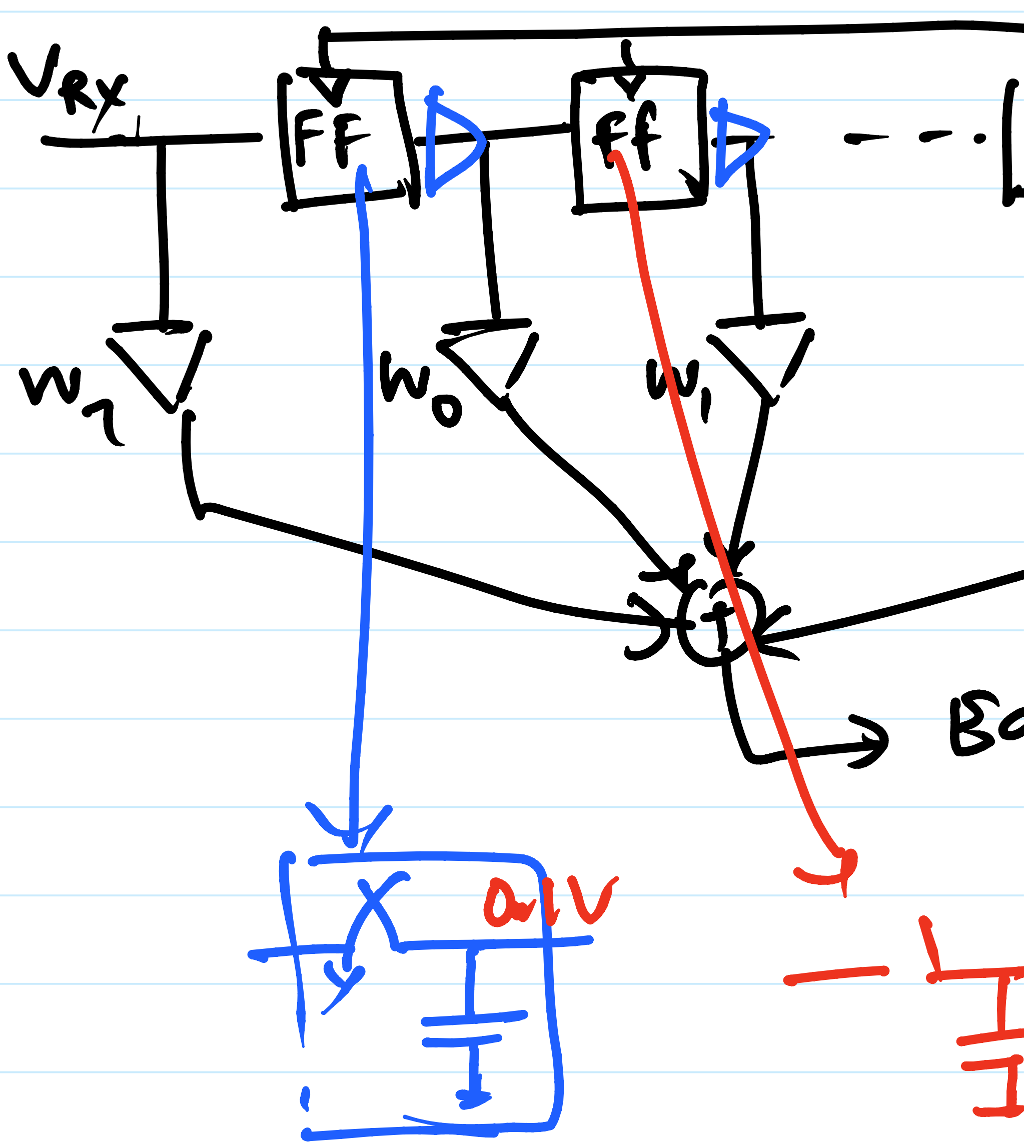
Heq1 — de-emphasis

Heq2 — pre-emphasis

Equalization on Rx. side

$V_{Tx} - d[n]$

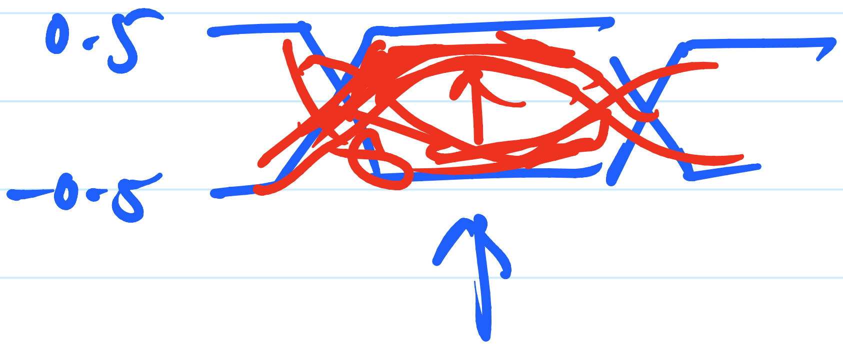


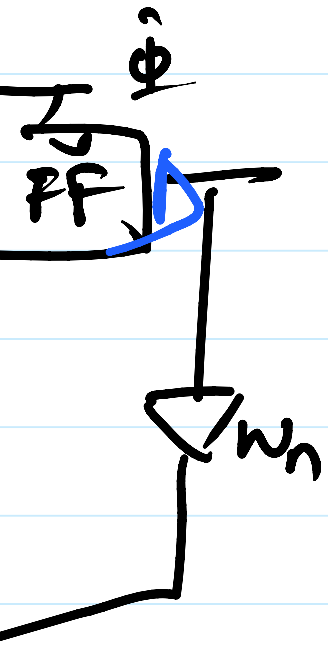


On Tx side — Digital FF

On Rx side — Analog FF

1) Clk-Q-delay





40 Gb/s

T = 25 ps

qualized Response

5th tap
0.09V

1) Clk - Q - delay
2) Clock feedthrough
3) Leakage of hold voltage.