1. Model a differential 12 in FR4 μ-stripline channel with 50 Ω characteristic impedance, as shown in Fig. 1.

1. Plot frequency response of the channel for series and differential termination on source and load sides, respectively.
2. Plot eye diagram at the output of the channel when PRBS7 data at 5 Gb/s is transmitted across the channel.
3. Find the worst case vertical and horizontal eye openings for 5 Gb/s transmission across the channel. Plot the worst case eye diagram.
4. Compensate the channel loss with 2-tap FIR equalizer for 5 Gb/s transmission. Plot the worst case vertical and horizontal eye openings at the output of the channel after equalization.

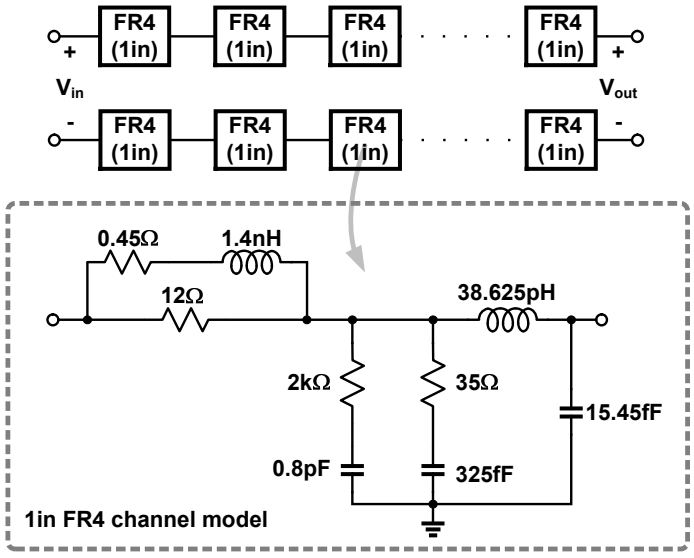

Figure 1: RLC model of a FR4 μ-stripline channel.

2. Design a 5 Gb/s current mode output driver (see Fig. 2) with the following attributes:

1. 0.5 V peak-to-peak differential transmit swing when the driver is terminated differentially with 100 Ω on the load side.
2. Current source M_1 is biased in saturation region at all times.

Plot the following for the designed output driver and comment on the results.

1. $\mathrm{VOP_{Tx}}$ and $\mathrm{VON_{Tx}}$ versus differential DC input $\mathrm{VIP_{Tx}} - \mathrm{VIN_{Tx}}$.
2. Plot differential output eye diagram when the CML driver is driven by PRBS7 differential input.

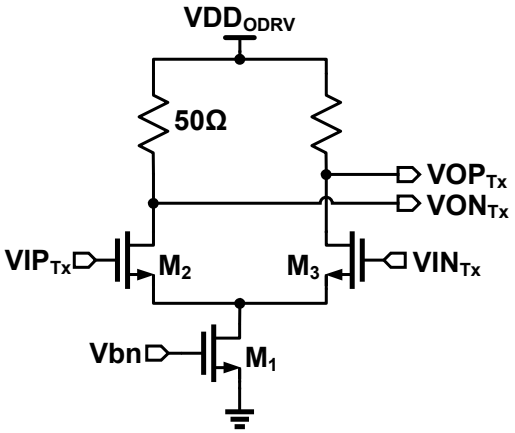

Figure 2: Schematic diagram of a current mode logic (CML) based output driver.

3. Design a 5 Gb/s CML based output driver implementing a 2-tap FIR equalizer for channel response in problem #1. The equalizer should have following attributes:

1. 50 Ω single-ended output impedance under all operating conditions.
2. 0.5 V maximum peak-to-peak differential output swing when the driver is terminated differentially.

Drive the CML output driver with PRBS7 input and plot the following. Comment on the results.

1. Differential eye diagram at CML driver output with differential termination and equalization enabled.
2. Differential eye diagram at the output of channel (w/ differential termination on Rx side) driven by CML output driver with equalization enabled. Verify if the equalizer coefficients obtained from peak distortional analysis are optimal. If not, determine optimal equalizer coefficients from circuit analysis and compare them with those obtained from behavioral simulations.

4. Design differential voltage mode (VM) output driver for 5 Gb/s data rate (see Fig. 3). The output driver should have following attributes:

1. The output driver has 1 V peak-to-peak differential output swing when terminated differentially with 100 Ω.
2. Output impedance of PMOS/NMOS switches when they are ON should be 50 Ω.

Plot the following for above output driver design and comment on the results.

1. VOP_{Tx} and VON_{Tx} versus differential DC input $\text{VIP}_{\text{Tx}} - \text{VIN}_{\text{Tx}}$.
2. Plot differential output eye diagram when driven by PRBS7 differential input.

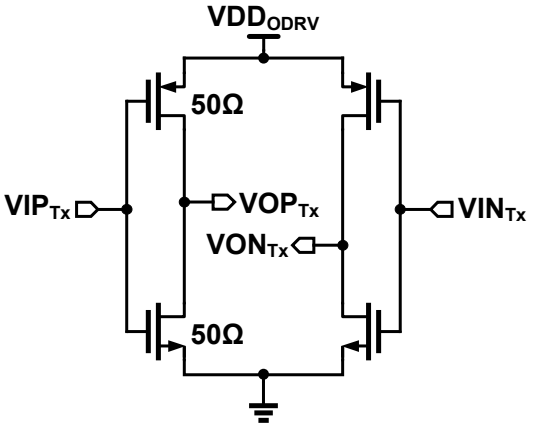

Figure 3: Voltage mode output driver with active output impedance.

5. Design a 5 Gb/s VM output driver implementing a 2-tap FIR equalizer for channel response in problem #1. The equalizer should have following attributes:

1. 50 Ω single-ended output impedance under all operating conditions.
2. 1.0 V peak-to-peak differential output swing when the driver is differentially terminated with 100 Ω.

Drive the VM output driver with PRBS7 input and plot the following for the designed equalizer. Comment on the results.

1. Differential eye diagram at VM driver output with 100 Ω differential termination and equalization enabled.
2. Differential eye diagram at the output of channel (w/ 100 Ω differential termination) driven by VM output driver with equalization enabled. Verify if the equalizer coefficients obtained from peak distortional analysis are optimal. If not, determine optimal equalizer coefficients from circuit analysis and compare them with those obtained from behavioral simulations.

6. Design differential voltage mode (VM) output driver for 5 Gb/s data rate with following attributes.

1. The output driver has 0.5 V peak-to-peak differential output swing when terminated differentially with 100 Ω.
2. Single-ended driver output impedance is 50 Ω.

Plot the following for above output driver design and comment on the results.

1. $\mathrm{VOP_{Tx}}$ and $\mathrm{VON_{Tx}}$ versus differential DC input.
2. Plot differential output eye diagram when driven by PRBS7 differential input.