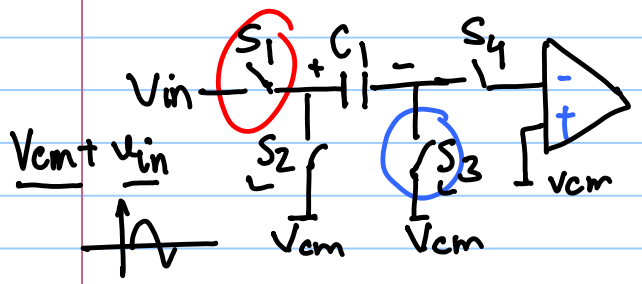
Lecture #46

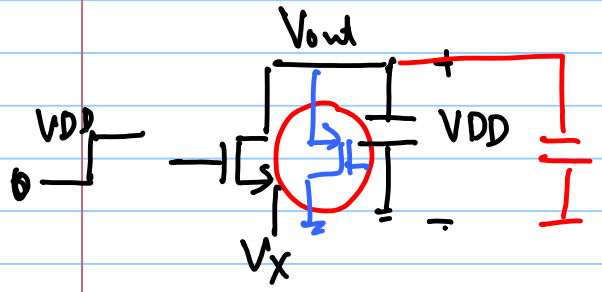
Note Title 23-04-2019



NMOS : $I = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$, S_2, S_3

PMOS :

Transmission Gate : S_1, S_4



NMOS: X } Δt_1, C_{P1}

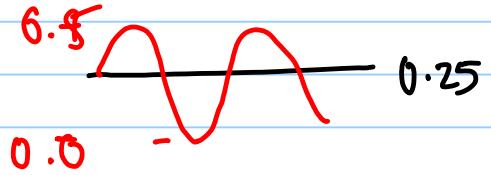
PMOS: Y }

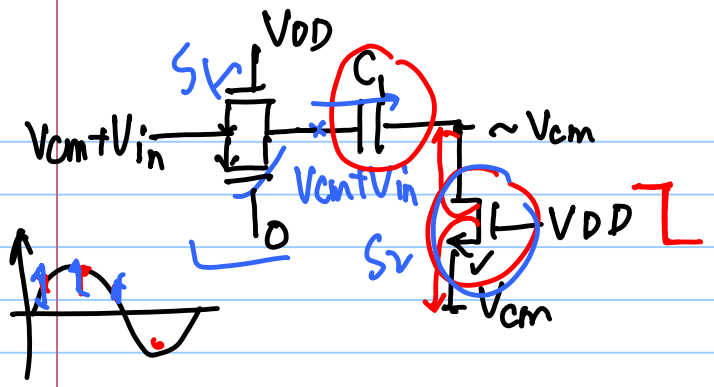
NMOS: X+Y, } Δt_2 , C_{P1}
} $< \Delta t_1$

$V_x = 0$ ✓ NMOS

$V_x = \frac{3VDD}{4}$ ✓ PMOS

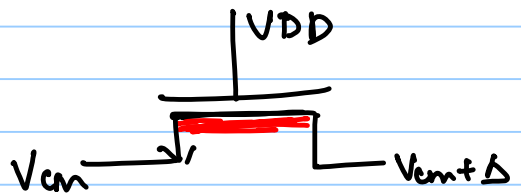
$V_x = \frac{VDD}{4}$ ✓ NMOS

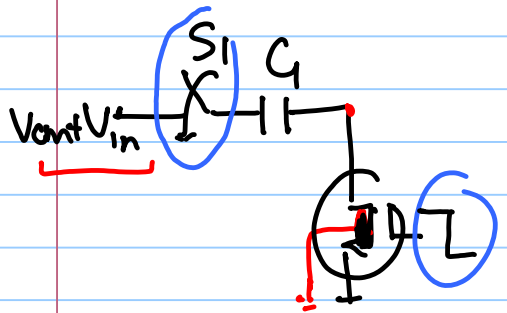




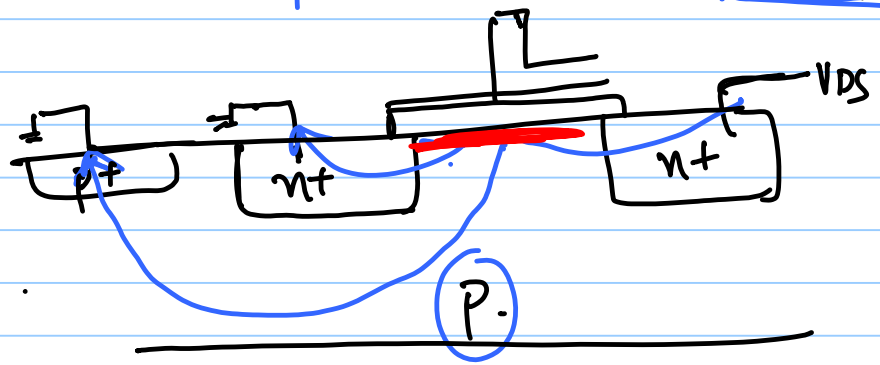
$$I = \mu_n C_{ox}\left(\frac{W}{L}\right)_n \left[(V_{DD} - V_{cm} - V_{tn})\, V_{DS} - \frac{V_{DS}^2}{2}\right]$$

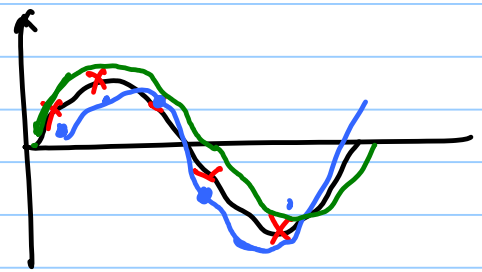
$\frac{V_{DS}^2}{2} \approx 0$

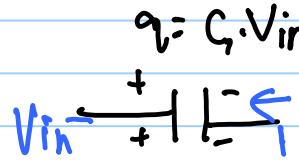




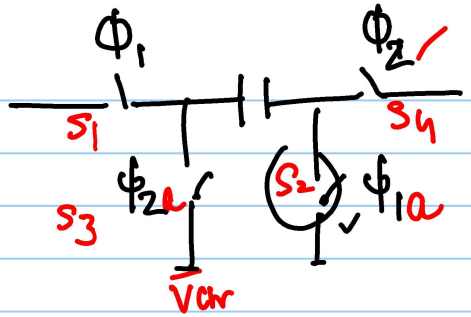
$$q_1 = (WL)\, C_{ox}\, (V_{DD} - V_{cm} - V_{tn}) \longrightarrow \Delta V = \frac{q_1}{C_1}$$



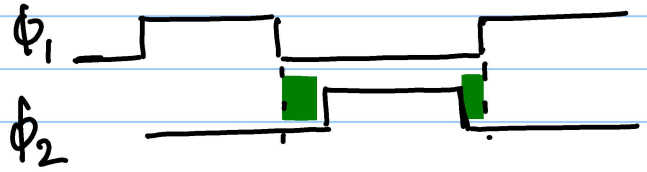


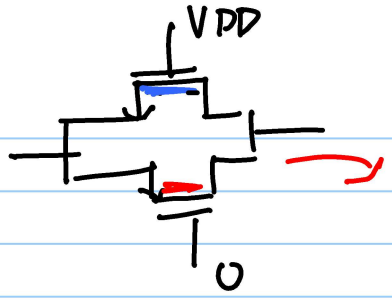


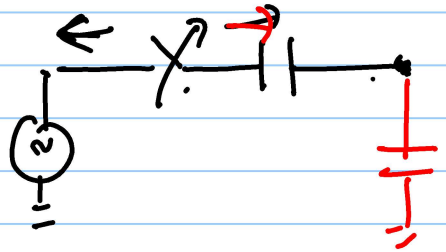
$$q_2 \propto V_{in} \longrightarrow \Delta V \propto \frac{V_{in}}{C_1}$$

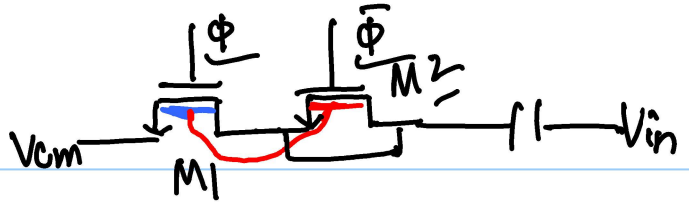


$\Phi_1 = \overline{\Phi_2}$









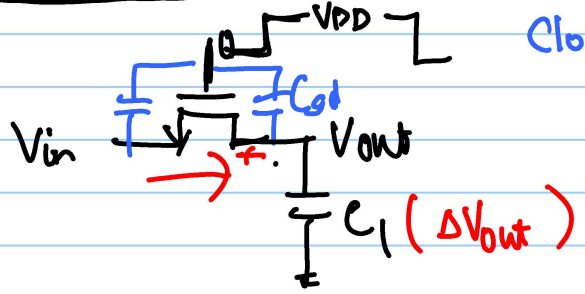
Φ is high : M_1 is ON
M_2 is OFF

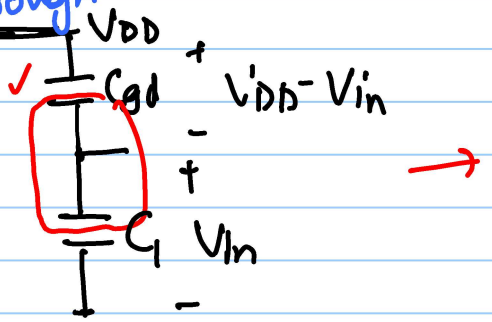
Φ is low :

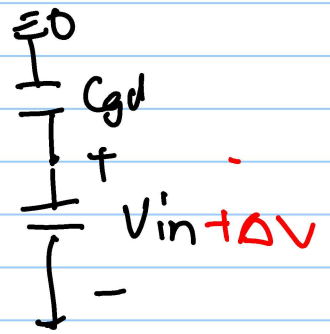
$$q_1 \propto \frac{(WL)_1}{2}$$

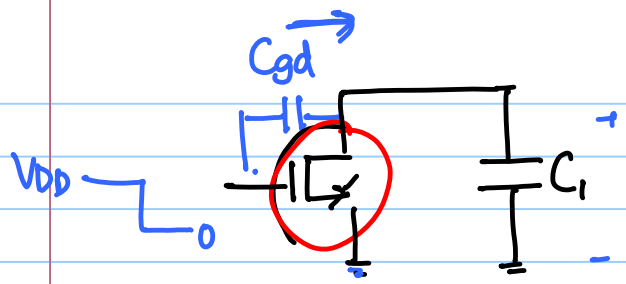
$$q_2 \propto (WL)_2$$

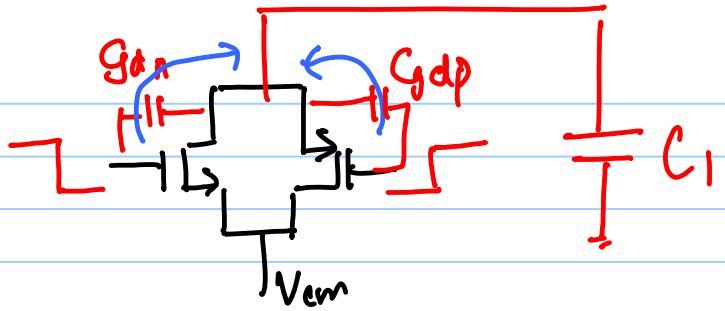
Clock Feed through

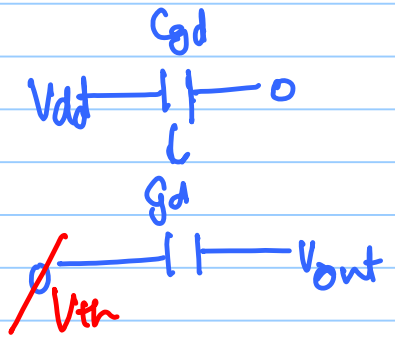


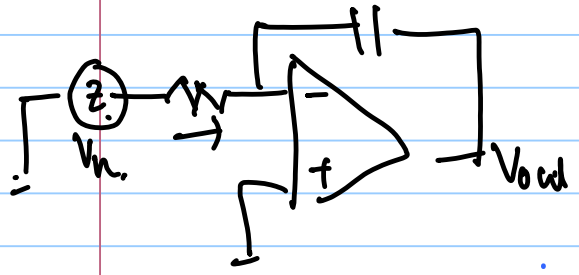


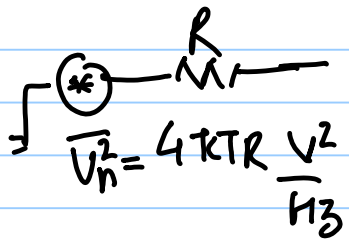


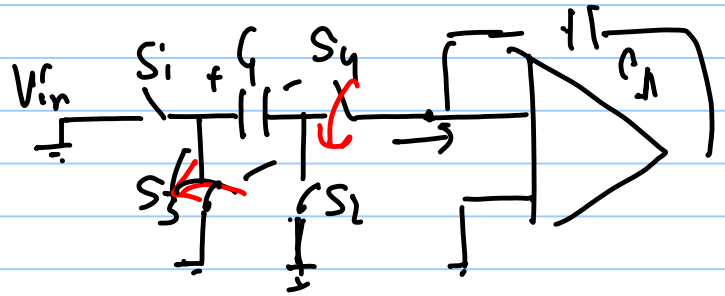

Cgd
VDD
0
C1


Cgdn
Cgdp
C1
Vem


Cgd
Vdd
0
Gd
Vout
Vem


Vn
Vout


R
$\overline{V_n^2} = 4KTR\,\frac{V^2}{Hz}$


Vin
S1
C1
S4
S3
S2
CA

$$\overline{V_{n,s}^2} = \frac{2kT}{C_1}$$

$$V_{C_1} = V_{in} + V_n$$