Negative Feedback System and Circuit Design

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  - Negative feedback amplifier realization
- Stability and compensation
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- Feedback around transistors
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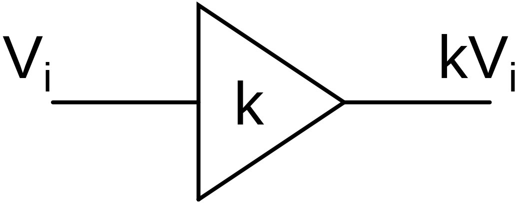
  - Negative Feedback in Single Transistor Circuits
- CMOS opamps—1, 2, and 3 stages
- Amplifier Nonlinearity in Negative Feedback Systems
- Case studies
  - A 7X Programmable 5^{th} Order Active-RC Filter
  - Lead lag compensation

Negative feedback amplifier basics

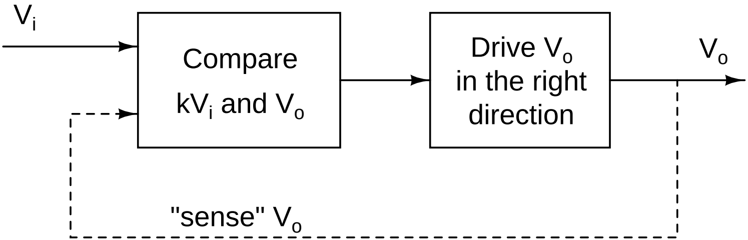
Goals



Realize an amplifier with a gain k using negative feedback

- with a high gain accuracy
- with a high speed

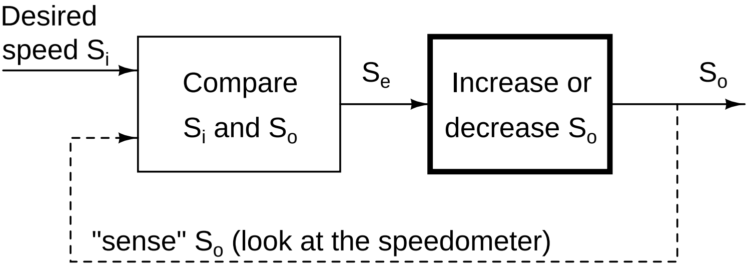
Negative feedback



Sense the difference between desired and actual output, and drive the output in the right direction

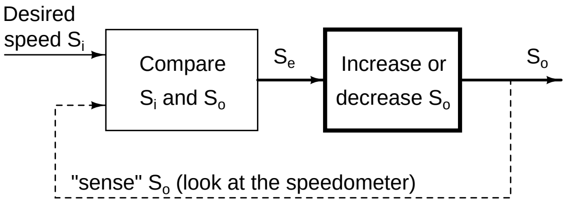
- Controlling the speed of a vehicle
- Controlling the volume of an audio player

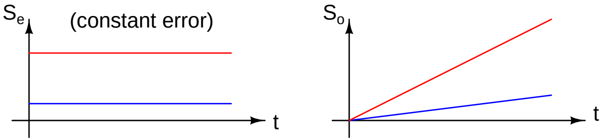
Speed control



- Input: Desired speed
- Sense: Speedometer reading
- Drive: Proportional to the difference

Speed control-driving block behavior

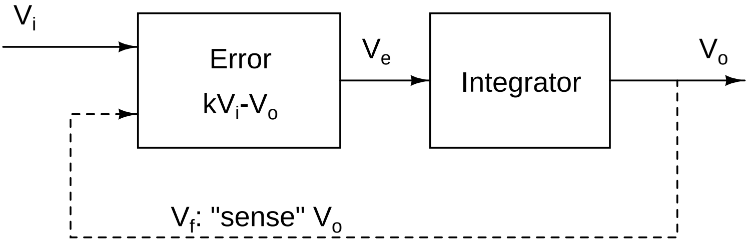




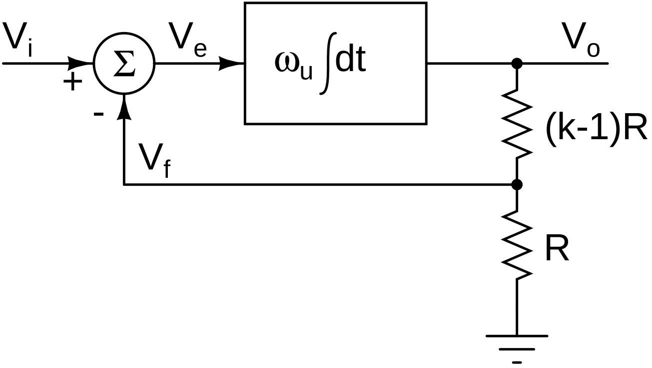
- Output ramps up for constant error
- Ramp rate proportional to error

Integrate the error S_e to drive the output

Integrator in the forward path

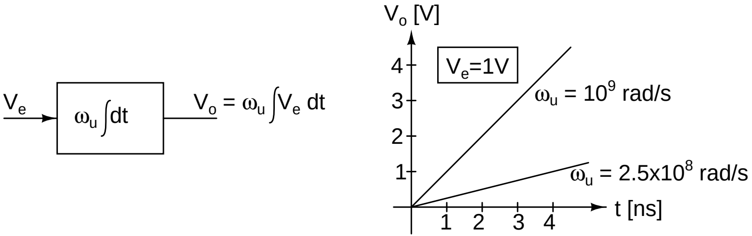


- At steady state, $V_f = V_i$ (constant input V_i)
- Zero steady state error



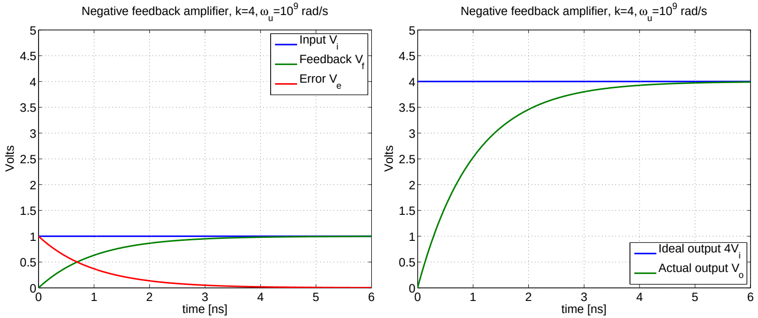
- Zero steady state error for constant inputs: $V_f = V_i$
- For an amplifier of gain k, $V_o = kV_i \Rightarrow$ use $V_f = V_o/k$

Integrator: Time domain



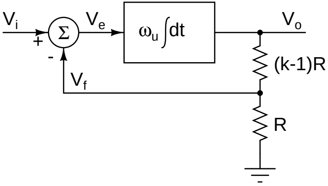
- Described by a single parameter ω_u
- Higher $\omega_u \Rightarrow$ faster integration

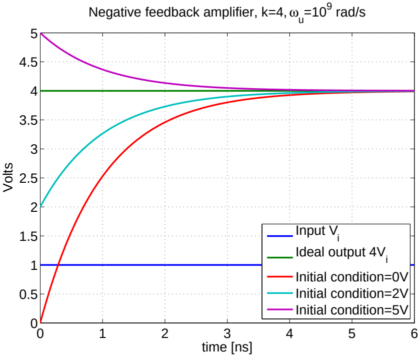
Negative feedback amplifier using an integrator



- Error reduces as feedback V_f ramps up
- Reduced error slows the rate of output ramp

Negative feedback amplifier: Constant input

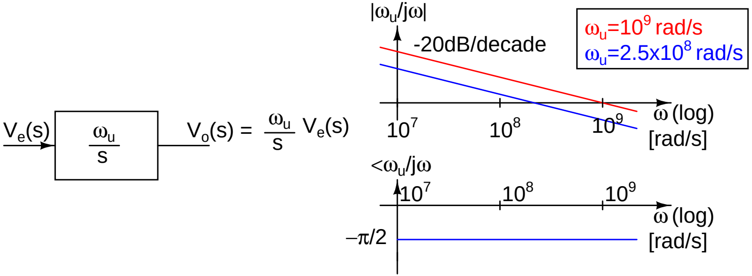




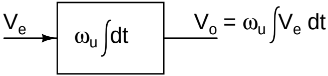
$$\frac{dV_o}{dt} = \omega_u \left(V_i - \frac{V_o}{k} \right)$$

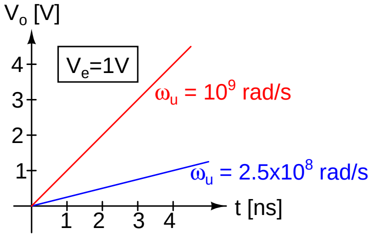
$$V_o(t) = kV_i \left(1 - \exp(-\frac{\omega_u}{k} t) \right) + V_o(0) \exp(-\frac{\omega_u}{k} t)$$

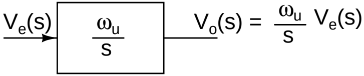
- Output exponentially approaches the steady state of kV_i

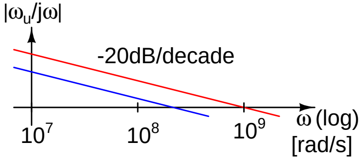


- Described by a single parameter ω_u
- ω_u: "unity gain frequency"
- Higher $\omega_u \Rightarrow$ higher gain magnitude for all frequencies

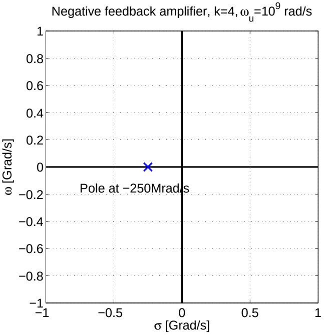

V_e
ω_u ∫dt
V_o = ω_u ∫V_e dt

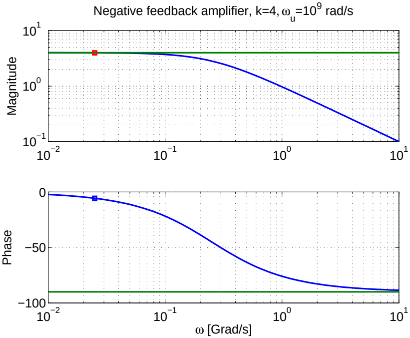

V_o [V]
V_e=1V
ω_u = 10^9 rad/s
ω_u = 2.5x10^8 rad/s
t [ns]
1
2
3
4
1
2
3
4


V_e(s)
ω_u / s
V_o(s) = ω_u / s V_e(s)


|ω_u/jω|
-20dB/decade
10^7
10^8
10^9
ω (log)
[rad/s]

Negative feedback amplifier: Frequency domain





$$V_o(s) = \frac{\omega_u}{s}\left(V_i - \frac{V_o}{k}\right)$$

$$\frac{V_o(s)}{V_i(s)} = \frac{k}{1 + \frac{s}{\omega_u/k}}$$

- First order response; DC gain $= k$, pole at ω_u/k

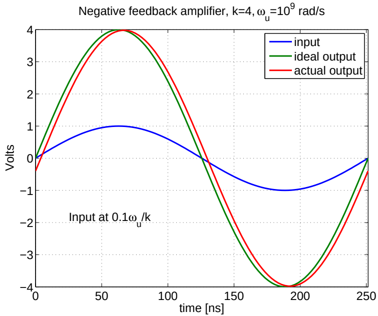
Negative feedback amplifier: Sinusoidal input

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{k}{1 + \frac{j\omega}{\omega_u/k}}$$

$$\left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \frac{k}{\sqrt{1 + \left(\frac{\omega}{\omega_u/k}\right)^2}} \quad ; \quad \angle\frac{V_o(j\omega)}{V_i(j\omega)} = -\tan^{-1}\frac{\omega}{\omega_u/k}$$

- dc gain: k ($=$ desired value)
- 3 dB bandwidth: ω_u/k

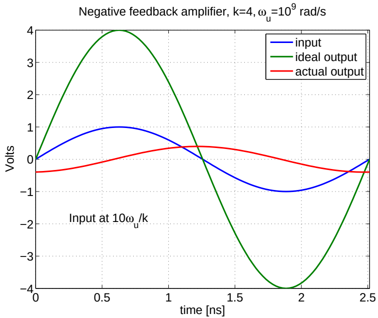
Negative feedback amplifier: Low frequency input



$$\left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \frac{k}{\sqrt{1+\left(\frac{\omega}{\omega_u/k}\right)^2}} \approx k$$

$$\angle\frac{V_o(j\omega)}{V_i(j\omega)} = -\tan^{-1}\frac{\omega}{\omega_u/k} \approx \frac{\omega}{\omega_u/k}$$

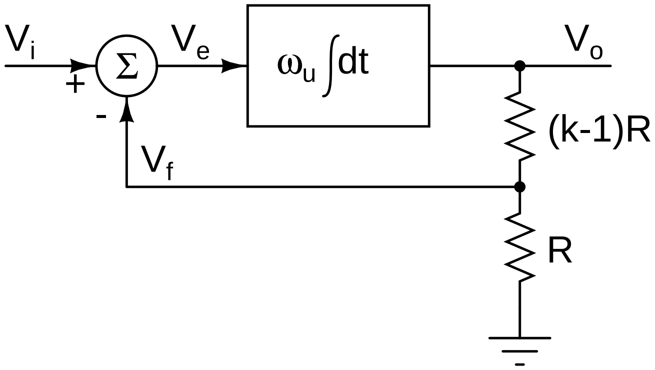
- Nearly ideal behavior
- Gain k, delay k/ω_u



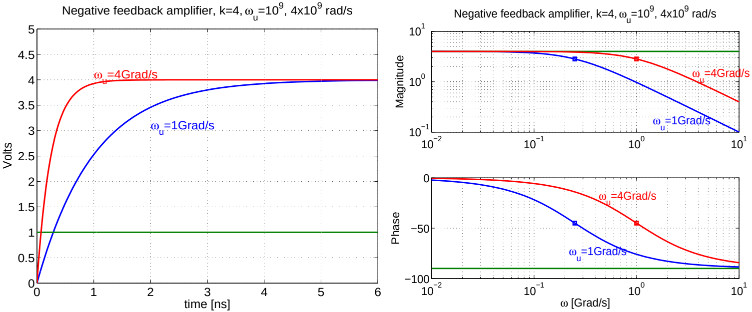
$$\left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \frac{k}{\sqrt{1+\left(\frac{\omega}{\omega_u/k}\right)^2}} \approx \frac{\omega}{\omega_u}$$

$$\angle\frac{V_o(j\omega)}{V_i(j\omega)} = -\tan^{-1}\frac{\omega}{\omega_u/k} \approx -\frac{\pi}{2}$$

- Attenuated output
- Nearly 90° phase lag

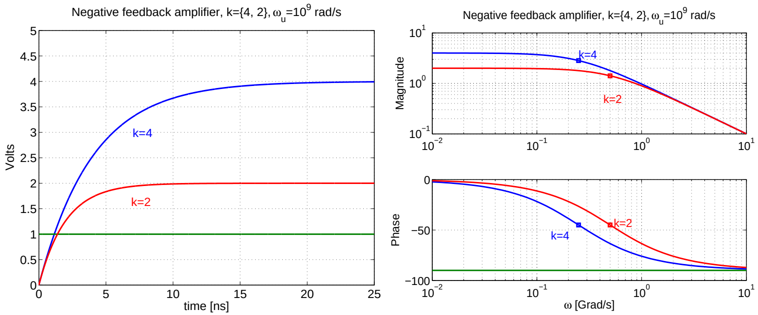


- Integrate the error $V_i - V_o/k$ to drive the output
- Ideal steady state output for constant inputs
- Nearly ideal output for “slow” inputs; constant delay k/ω_u
- Attenuated output for “fast” inputs; large phase lag



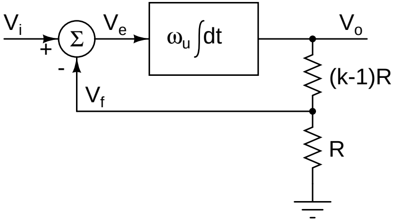
- Time constant: k/ω_u
- Higher $\omega_u \Rightarrow$ Faster response
- Bandwidth: ω_u/k
- Higher $\omega_u \Rightarrow$ Desired gain over a wider frequency range

Negative feedback amplifier: Effect of k



- Higher $k \Rightarrow$ longer time to reach steady state
- Gain bandwidth product: ω_u
- Bandwidth: ω_u/k
- Higher $k \Rightarrow$ Smaller bandwidth

Example



#1: $k = 4$, bandwidth $f_{3dB} = 100\,$MHz.

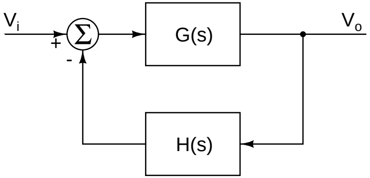
- Bandwidth (in rad/s) = $\omega_u/k = 2\pi f_{3dB}$
- Require an integrator with $\omega_u = 8\pi \times 100\,$Mrad/s $= 2.514\,$Grad/s

#2: $k = 4$, 99% settling time $\tau_s = 20\,$ns

- Require an integrator with $\omega_u = 2k\ln(10)/\tau_s = 0.92\,$Grad/s

(These numbers apply only to the configuration shown in the above figure)

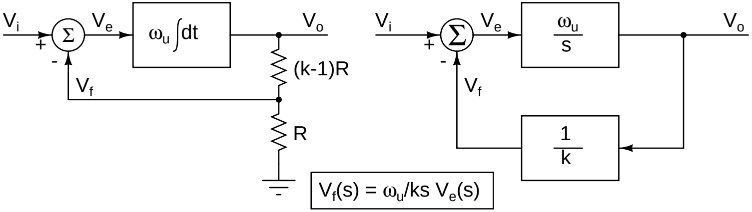
Feedback system and loop gain



$$\frac{V_o(s)}{V_i(s)} = \frac{G(s)}{1+G(s)H(s)} = \frac{1}{H(s)} \frac{1}{1+\frac{1}{G(s)H(s)}}$$
$$\approx \frac{1}{H(s)} \qquad |GH| \gg 1$$
$$\approx G(s) \qquad |GH| \ll 1$$

- Loop gain $L(s) = G(s)H(s)$
- Feedback effectively broken when $|L| \ll 1 \therefore V_o/V_i \approx G(s)$

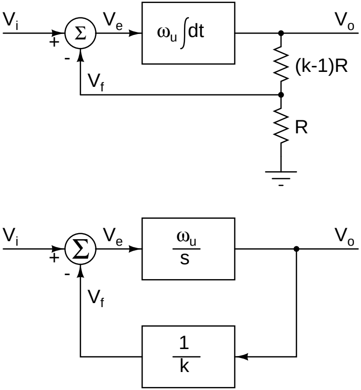
Feedback system and loop gain



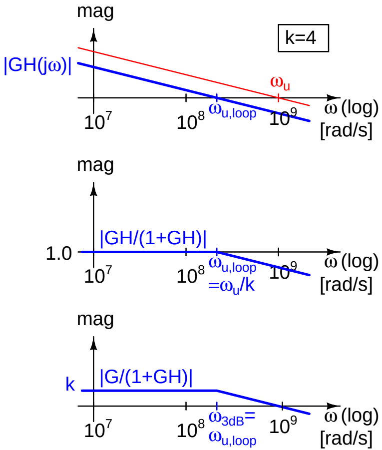
$$L(s) = \frac{\omega_u}{ks}$$ Loop gain

$$\omega_{u,loop} = \frac{\omega_u}{k}$$ Unity loop gain frequency

- Nearly ideal behavior below $\omega_{u,loop}$
- Nonideal behavior above $\omega_{u,loop}$



V_i
+
-
Σ
V_e
ω_u ∫dt
V_o
(k-1)R
V_f
R
V_i
+
-
Σ
V_e
ω_u / s
V_o
V_f
1 / k



mag
k=4
|GH(jω)|
ω_u
ω (log)
[rad/s]
10^7
10^8
ω_u,loop
10^9
mag
1.0
|GH/(1+GH)|
10^7
10^8
ω_u,loop
=ω_u/k
10^9
ω (log)
[rad/s]
mag
k
|G/(1+GH)|
10^7
10^8
ω_3dB=
ω_u,loop
10^9
ω (log)
[rad/s]

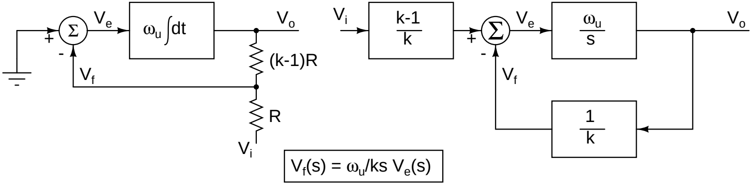
Feedback system and loop gain

- 3 dB bandwidth $= \omega_{u,loop}$, the unity loop gain frequency
- In general closed loop system bandwidth (region of ideal behavior) comprises regions of high loop gain

For our amplifier

- Unity loop gain frequency $\omega_{u,loop} = \omega_u/k$
- $\omega_{u,loop}$ *is not always* ω_u divided by the closed loop gain k!
- $\omega_{u,loop}$ is the unity gain frequency of $G(s)H(s)$

Inverting amplifier



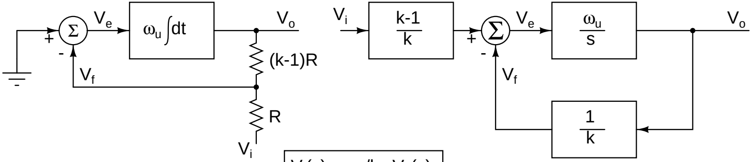
$$\frac{V_o}{V_i} = -\frac{k-1}{1+\frac{s}{\omega_{/}k}}$$

$$L(s) = \frac{\omega_u}{ks}$$ Loop gain

$$\omega_{u,loop} = \frac{\omega_u}{k}$$ Unity loop gain frequency

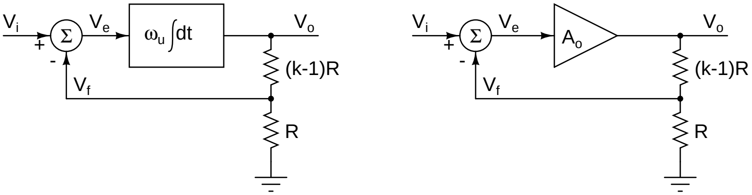
- $\omega_{u,loop}$ depends on the feedback factor, not the closed loop gain

Inverting amplifier



$V_f(s) = \omega_u/ks\ V_e(s)$

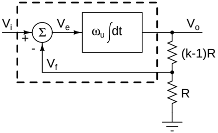
- Loop gain, stability are properties of the loop
- Transfer function depends on the input/output locations

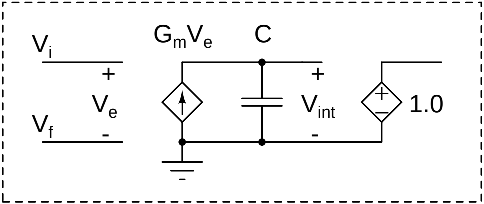


- Easily related to intuitive notion of feedback
- Incorporates delay/finite bandwidth
- Ideal behaviour for constant inputs
- All feedback systems have “integrator-like” behaviour over some range
- $\omega_u = \infty$: Ideal behavior for all frequencies

Negative feedback amplifier realization

Negative feedback amplifier: Realization



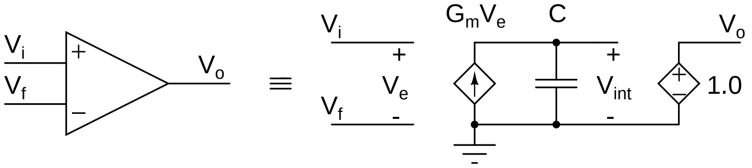


$$V_o(s) = \frac{G_m}{sC} V_e(s)$$

- Difference input to sense $V_i - V_f$
- Integration using $G_m - C$; $\omega_u = G_m/C$
- Buffer to isolate the load

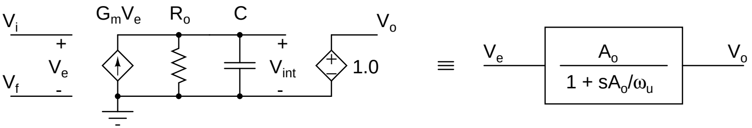
Combination of differencing and integration: **opamp**

Operational amplifier (opamp)



Combination of differencing and integration: **opamp**

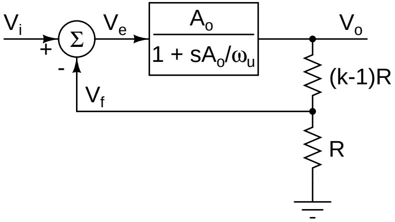
Integrator: Finite dc gain



$$V_o(s) = \frac{G_m R_o}{1 + sCR_o} V_e(s)$$
$$= \frac{1}{\frac{sC}{G_m} + \frac{1}{G_m R_o}} V_e(s)$$
$$= \frac{1}{\frac{s}{\omega_u} + \frac{1}{A_o}} V_e(s)$$

- Controlled current source has a finite output resistance R_o
- Finite dc gain $A_o = G_m R_o$
- Pole at $-\omega_u / A_o$ instead of the origin

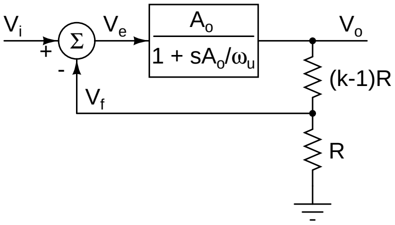
Negative feedback amplifier: Finite dc gain



$$\frac{V_o(s)}{V_i(s)} = \frac{k}{1 + \frac{k}{A_o} + s\frac{k}{\omega_u}}$$

- Non zero steady state error for a constant input
- DC gain: $k/(1 + k/A_o)$
- Relative error inversely proportional to dc loop gain A_o/k
- Pole: $\omega_u/k(1 + k/A_o) \approx \omega_u/k$

Example



#1: $k = 4$, error $\delta = 1\%$

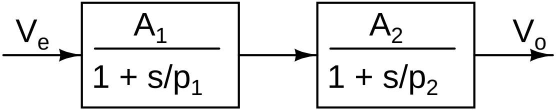
- $k/(1 + k/A_o) = k(1 - \delta)$
- $k/A_o \approx \delta = 0.01$
- Need an opamp with a dc gain $A_o = 400$
- Larger A_o required for higher accuracy
- Larger A_o required for higher gain k

(These numbers apply only to the configuration shown in the above figure)

Negative feedback amplifier: Increasing gain accuracy

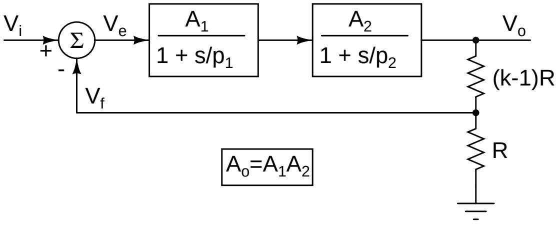
- DC gain: $k/(1+k/A_o)$
- Increase dc loop gain to increase gain accuracy
- Limited $G_m R_o \Rightarrow$ Cascade many stages

Two stages in cascade



$$\boxed{A_o = A_1 A_2}$$

- DC gain $A_o = G_{m1}R_{o1}G_{m2}R_{o2}$
- Two poles at $-p_1 = -1/R_{o1}C_1$, $-p_2 = -1/R_{o2}C_2$



$$\frac{V_o}{V_i} = \frac{k}{1 + \frac{k}{A_o} + s\left(\frac{1}{p_1} + \frac{1}{p_2}\right)\frac{k}{A_o} + \frac{s^2}{p_1 p_2}\frac{k}{A_o}}$$

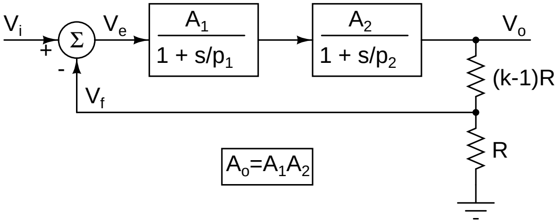
$$dcgain \quad \frac{k}{1 + \frac{k}{A_o}}$$

A_o much larger than before

$$\zeta = \frac{1}{2}\sqrt{\frac{k}{A_o}}\left(\sqrt{\frac{p_2}{p_1}} + \sqrt{\frac{p_1}{p_2}}\right)$$

Damping factor

Two stage amplifier in negative feedback

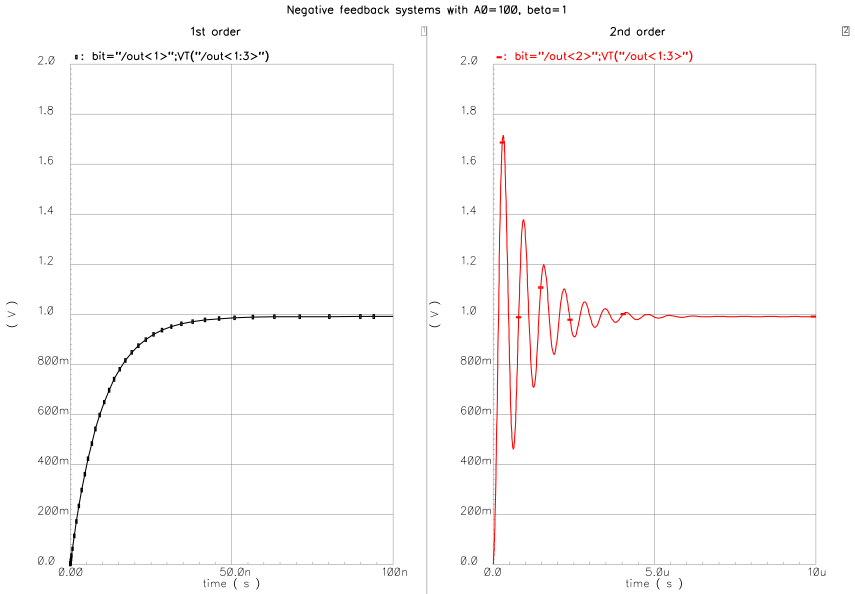


$$\zeta = \frac{1}{2}\sqrt{\frac{k}{A_o}}\left(\sqrt{\frac{p_2}{p_1}} + \sqrt{\frac{p_1}{p_2}}\right)$$

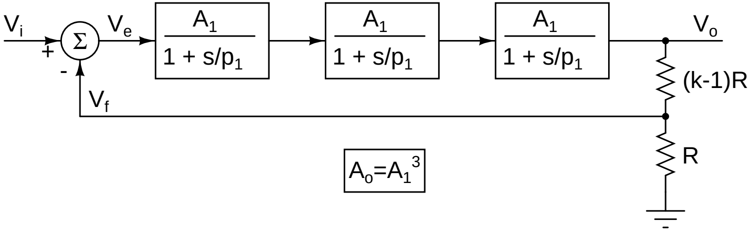
Damping factor

- Higher $A_o/k \Rightarrow$ reduced steady state error
- Small damping factor for large A_o/k—Lot of ringing
- Damping factor increased by increasing the ratio p_2/p_1
- Poles well separated $\Rightarrow$ less ringing

Two stage amplifier in negative feedback



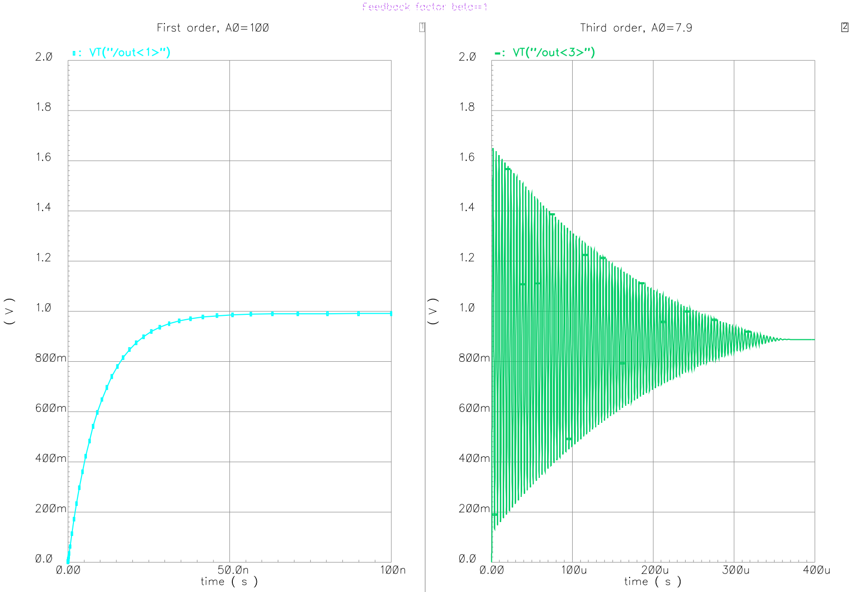
Three stage amplifier in negative feedback



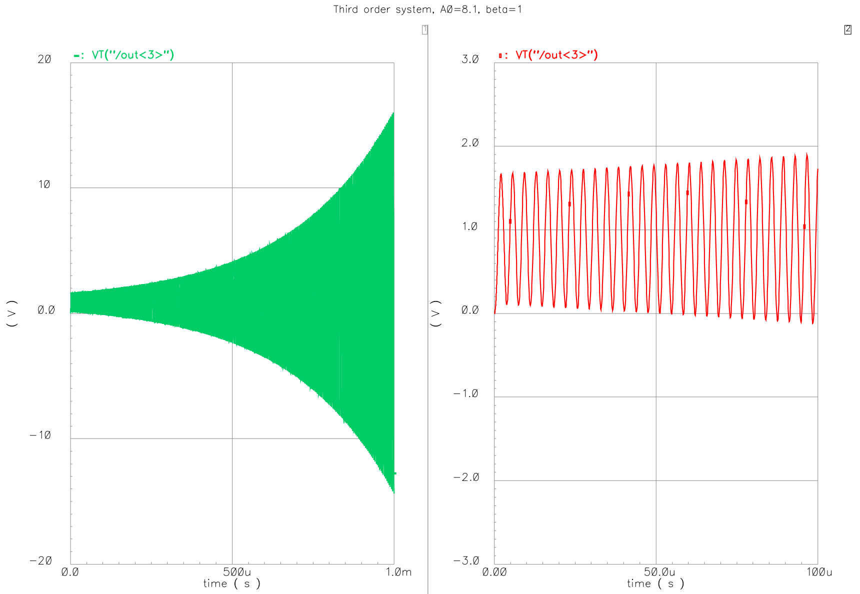
$$\frac{V_o}{V_i} = \frac{k}{1 + \frac{k}{A_o} + 3\frac{s}{p_1}\frac{k}{A_o} + 3\frac{s^2}{p_1^2}\frac{k}{A_o} + \frac{s^3}{p_1^3}\frac{k}{A_o}}$$

- Amplifier has 3 poles at $-p_1$
- Poles at $\pm j\sqrt{3}p_1$ for $A_o/k = 8$
- Instability for $A_o/k \geq 8$, but require *much* larger values!

Three stage amplifier in negative feedback



Three stage amplifier in negative feedback



Realizing accurate amplifiers: Problem

- Large A_o/k required for high accuracy
- Stage A_o limited by finite R_o
- Larger A_o from cascaded stages, but ... low damping, ringing, instability

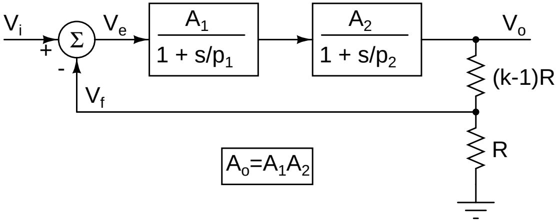
Realizing accurate amplifiers: Remedy

$$\zeta = \frac{1}{2}\sqrt{\frac{k}{A_o}}\left(\sqrt{\frac{p_2}{p_1}} + \sqrt{\frac{p_1}{p_2}}\right) \qquad \text{Damping factor}$$

Results from two cascaded stages provides a possible way out

- Move the poles apart
- Ratio of poles should be $\sim A_o/k$ (damping factor around 1)

For a damping factor of $\sqrt{2}$



$$\zeta = \frac{1}{2}\sqrt{\frac{k}{A_o}}\left(\sqrt{\frac{p_2}{p_1}} + \sqrt{\frac{p_1}{p_2}}\right) = \frac{1}{\sqrt{2}}$$

$$\zeta \approx \frac{1}{2}\sqrt{\frac{k}{A_o}}\left(\sqrt{\frac{p_2}{p_1}}\right)$$

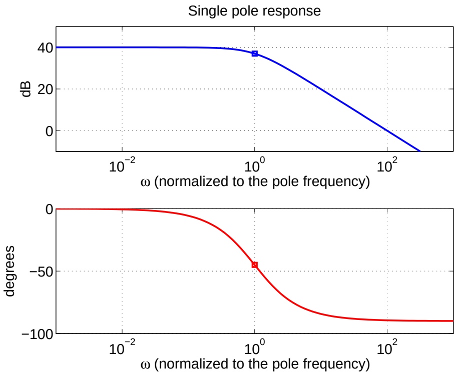
$$p_2 = 2\frac{A_o p_1}{k}$$

Multiple poles: Frequency domain view

$$\frac{V_o(s)}{V_i(s)} = \frac{G(s)}{1 + G(s)H(s)} = \frac{1}{H(s)} \frac{1}{1 + \frac{1}{G(s)H(s)}}$$

- Instability if loop gain $L = GH = -1$, i.e. $|L| = 1$ and $\angle L = -\pi$
- When GH has only poles and no zeros, instability if $|L| > 1$ and $\angle L = -\pi$
- Avoid this condition to ensure stability

Single real pole: Bode plot

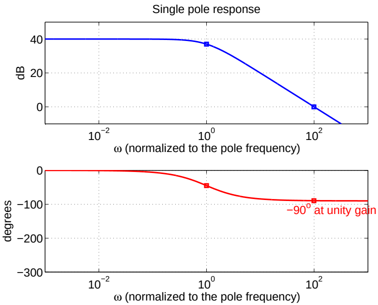


Magnitude:

- Constant for frequencies less than the pole frequency
- Rolloff for frequencies more than the pole frequency

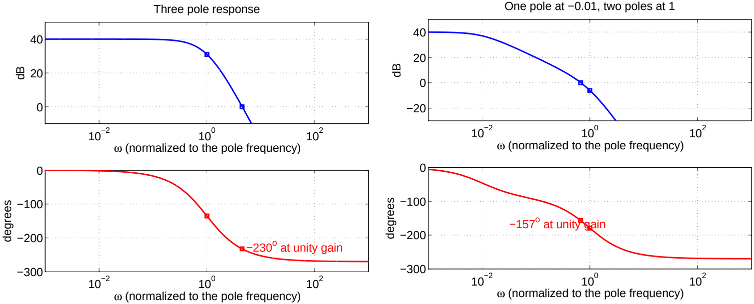
Phase:

- Phase change before and after the pole frequency
- $\pi/4 = 45^\circ$ lag at the pole frequency

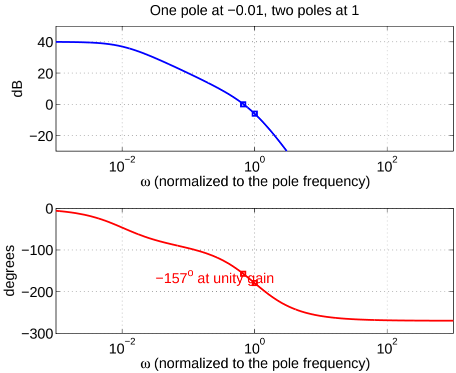


- With multiple poles close to each other, $\angle L$ drops off to or below $-\pi$ before $|L|$ rolls off to unity $\Rightarrow$ instability
- Risk of instability is worst when the loop gain is high and poles are close to each other

Poles far from each other



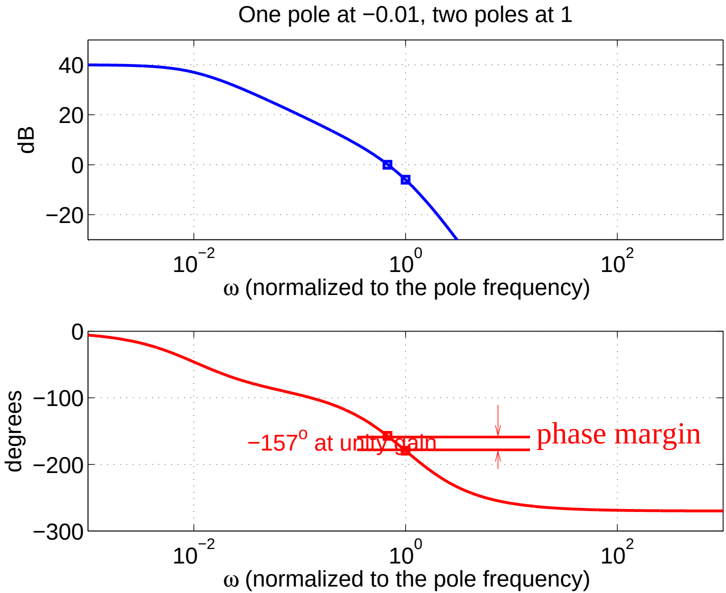
- With one pole at a much lower in frequency compared to others, magnitude rolls off to unity before phase approaches $-\pi$



- One pole at a low frequency (*)
- Remaining poles beyond the unity gain frequency
- $< 180^\circ$ phase lag at the unity loop gain frequency

(*) This condition is sufficient, but not necessary

Have “sufficient phase margin” for stability



Stability in Negative Feedback Systems

The Nyquist Criterion

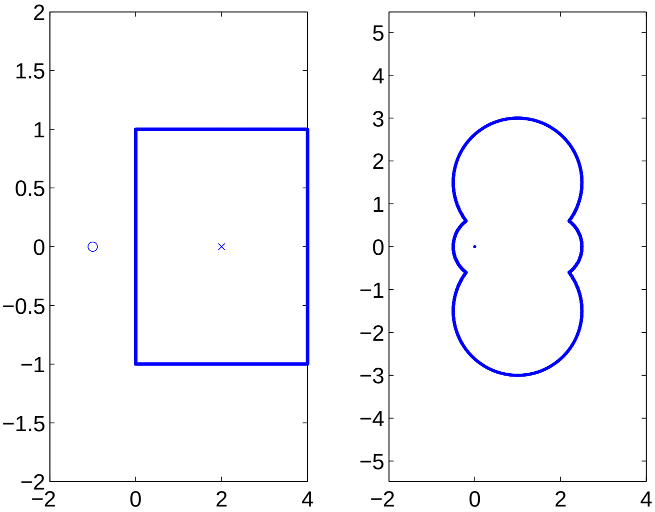
- The loop gain is $G(s)H(s)$
- Closed loop transfer function is $\frac{G(s)}{1+G(s)H(s)}$
- For stability, the closed loop poles must be in the Left Half Plane (LHP).
- The Nyquist Criterion : A technique to reliably predict the number of closed loop poles in the RHP from $G(s)H(s)$.

Preliminaries : Cauchy's Principle of Argument

- Consider a function $F(s)$, a ratio of polynomials in s
- Draw a closed contour in the s plane
- The contour must not pass through any singular points
- If the contour in the s-plane encloses **one** pole of $F(s)$, the locus of $F(s)$ encircles the origin of the $F(s)$ plane **once** in the **counterclockwise** direction

Preliminaries : Cauchy's Principle of Argument

$$F(s) = \frac{s+1}{s-2}$$

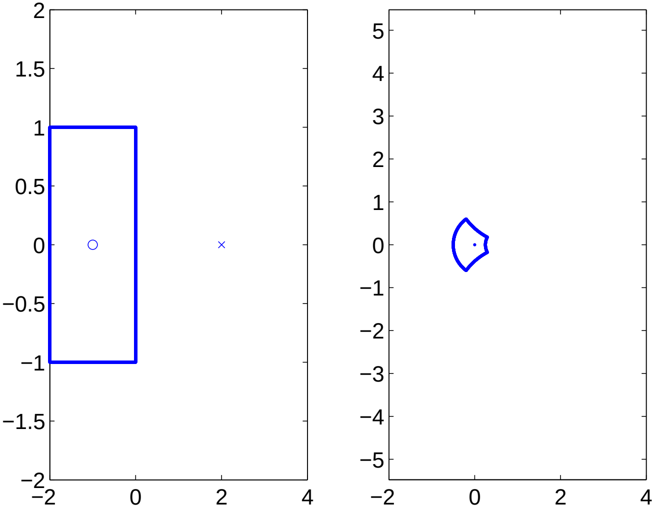


Preliminaries : Cauchy's Principle of Argument

- If the contour in the s-plane encloses **one** zero of $F(s)$, the locus of $F(s)$ encircles the origin of the $F(s)$ plane **once** in the **clockwise** direction

Preliminaries : Cauchy's Principle of Argument

$$F(s) = \frac{s+1}{s-2}$$

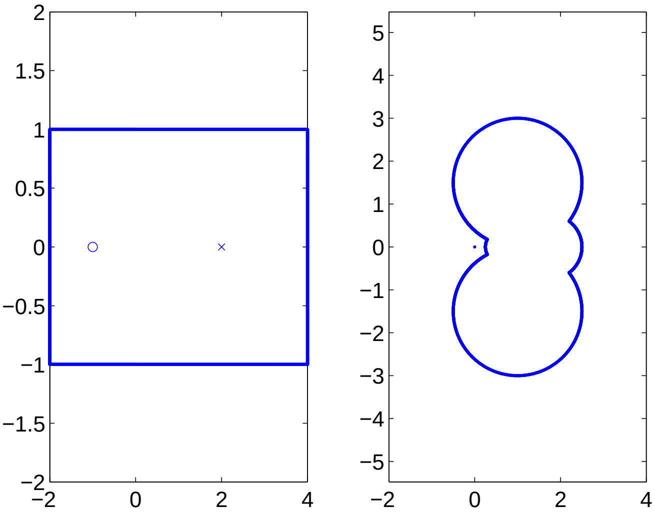


Preliminaries : Cauchy's Principle of Argument

- If the contour in the s-plane encloses **one** pole and **one** zero of $F(s)$, the locus of $F(s)$ does not encircle the origin

Preliminaries : Cauchy's Principle of Argument

$$F(s) = \frac{s+1}{s-2}$$

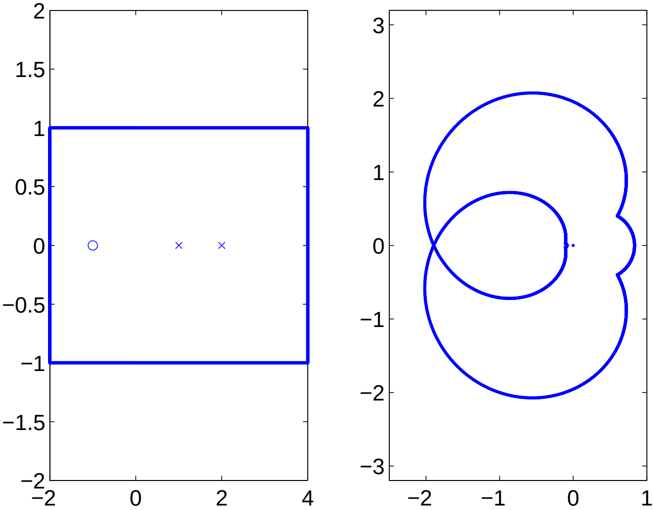


Summary : Cauchy's Principle of Argument

- If the contour in the s-plane encloses **N** poles and **M** zeros of $F(s)$, the locus of $F(s)$ encircle the origin **(N - M)** times in the counter-clockwise direction

Example

$$F(s) = \frac{s+1}{(s-2)(s-1)}$$



The Nyquist Criterion

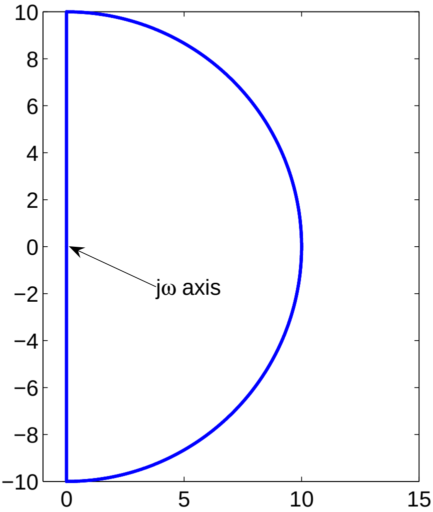
- Want to find if the poles of the closed loop system are in the RHP
- Closed loop poles are the roots of $1 + G(s)H(s) = 0$
- In other words, closed loop poles are the zeros of $1 + G(s)H(s)$
- In circuit work, the open loop system is always stable
- $\Rightarrow$ The poles of the open loop system are the the LHP
- The poles of $1 + G(s)H(s)$ and $G(s)H(s)$ are the same
- $\Rightarrow 1 + G(s)H(s)$ has poles in the LHP

The Nyquist Criterion

- Apply Cauchy's Principle to $F(s) = 1 + G(s)H(s)$
- $F(s)$ has poles in the LHP
- Apply Cauchy's Principle to find the location of the zeros of $F(s)$

The Nyquist Criterion

- Travel along a countour that encloses the entire RHP

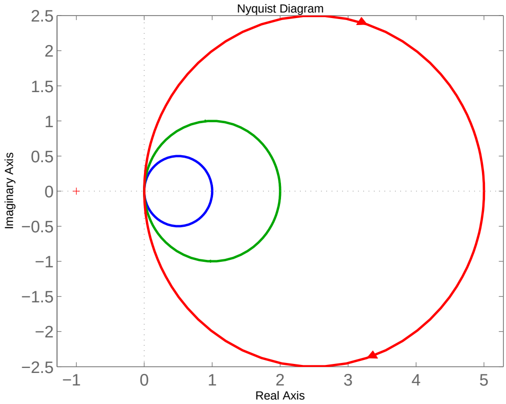


The Nyquist Criterion

- If $F(s)$ has zeroes in the RHP, there will be encirclements about the origin
- Since $F(s)$ has no poles in the RHP
  number of encirclements = number of RHP zeros of F(s)
  = number of RHP poles of the closed loop system
- $F(s)$ encircling the origin is equivalent to $G(s)H(s)$ encircling the point (-1,0)
- **Find the number of encirclements of $G(j\omega)H(j\omega)$ around the point (-1,0)**

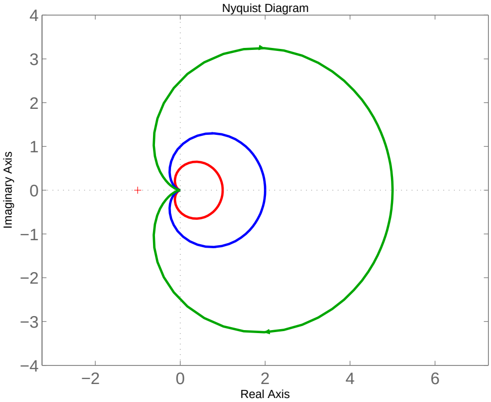
Nyquist by Example
All Pole Systems

First Order System : Unconditionally Stable



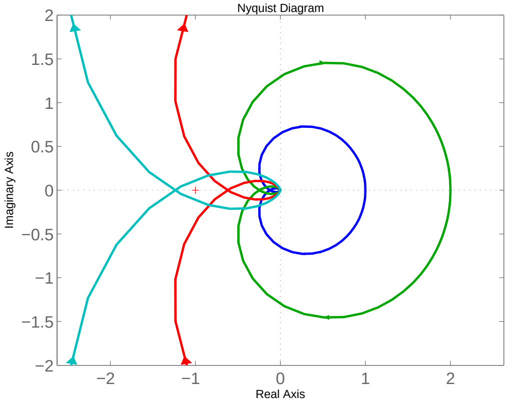
$$G(s)H(s) = \frac{K}{s+1}, K = 1, 2, 5$$

Second Order System : Unconditionally Stable



$$G(s)H(s) = \frac{K}{(s+1)^2}, K = 1, 2, 5$$

Third Order System : Conditionally Stable



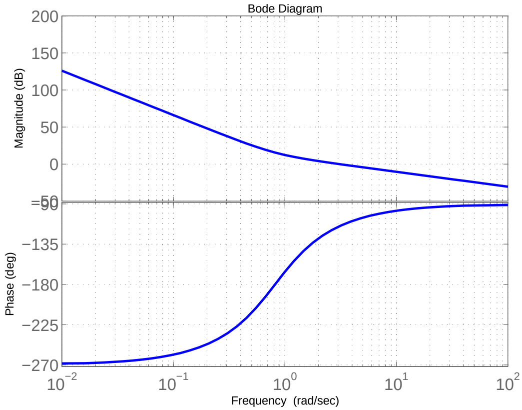
$$G(s)H(s) = \frac{K}{(s+1)^3}, K = 1, 2, 5, 10$$

All-pole Loop Gain Summary

- First & second order systems are unconditionally stable
- Third and higher order systems are conditionally stable
- Magnitude and phase are monotonically decreasing
- $\Rightarrow$ With a sufficiently large gain, will become unstable
- Example : Third order system becomes unstable for $K > 8$
- This intuition (wrongly) applied to other systems can cause confusion

Question

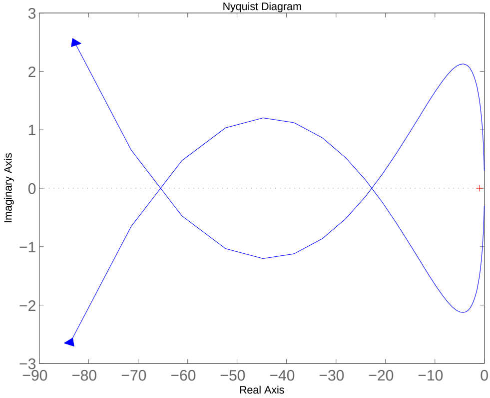
The loop gain of a feedback amplifier has a magnitude greater than 1, and a phase lag larger than 180 degrees. Is it possible that the closed loop system is stable ?



Answer : ?

- Example : $G(s)H(s) = \frac{3s^2+4s+2}{(s+\delta)^3}$, where $\delta \rightarrow 0$
- Closed loop poles the roots of $s^3 + 3s^2 + 4s + 2$
- Poles are at $-1, -1 \pm j$
- Phase lag @ DC is 0^o
- Phase lag @ low frequencies is 270^o
- Magnitude @ low frequencies $>> 1$

The Nyquist Plot



- Phase crosses 180^o twice
- There is **no** encirclement of (-1,0)
- $\Rightarrow$ There are no RHP poles
- System is stable !

Common Misconception I

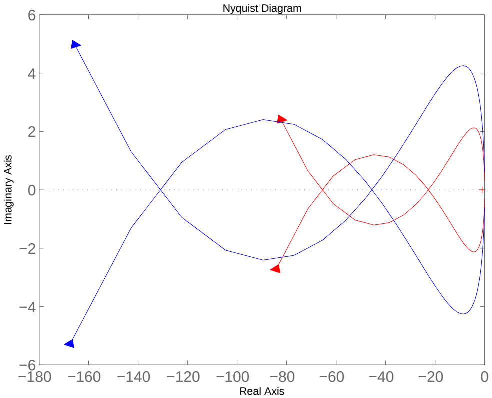
- Statement :If the magnitude is greater than 0 dB and the phase lag is greater than $180^o \Rightarrow$ instability
- True only for all pole $G(s)H(s)$
- **Incorrect** when the loop gain has zeros (as demonstrated by the example in the previous slides)

Question

I have a feedback system on the verge of instability. I now *increase* the loop gain by a factor $K > 1$. The closed loop system becomes nice and stable. Is this possible ?

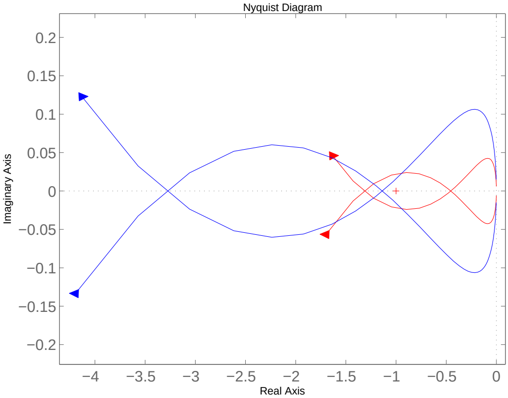
I have a stable feedback system. I now *decrease* the loop gain by a factor $K > 1$. The closed loop system starts oscillating. Is this possible ?

The Nyquist Plot



- Plot for high gain does not encircle (-1,0)
- System is “more” stable !

The Nyquist Plot



- Plot for low gain encircles (-1,0) twice
- $\Rightarrow$ There are **two** RHP poles
- System is unstable !

Common Misconception II

- Statement : Increasing gain is bad news for stability or reducing loop gain improves stability
- True only for all pole $G(s)H(s)$
- **Incorrect** when the loop gain has zeros (as demonstrated by the examples in the previous slides)
- These “anomalies” can be explained by the Nyquist plot

Closing Comments on Stability and Phase Margin

- For stability, the magnitude plot must have a slope of 20 dB per decade around the unity gain frequency.
- There can be any number of poles to the left or right of the unity gain cross over, and the system will be stable as long as these poles are sufficiently far away from the cross over frequency
- The phase margin is a valuable metric to assess stability even in high order systems
- To stabilize a high order system, it must be made to “look” like a first order system at and around its unit gain cross over point

Dominant pole frequency compensation

Dominant pole frequency compensation

Modify the frequency response such that there is

- One pole at a low frequency
- Remaining poles beyond the unity loop gain frequency
- $\omega_{u,loop} \approx (A_o/k)|p_1|$, where p_1 is the dominant pole
- 20 dB/decade rolloff at unity loop gain

This condition is sufficient, but not necessary

Two pole example

Damping factor of $1/\sqrt{2}$

$$\zeta = \frac{1}{2}\sqrt{\frac{k}{A_o}}\left(\sqrt{\frac{p_2}{p_1}}+\sqrt{\frac{p_1}{p_2}}\right) = \frac{1}{\sqrt{2}}$$

$$\zeta \approx \frac{1}{2}\sqrt{\frac{k}{A_o}}\left(\sqrt{\frac{p_2}{p_1}}\right)$$

$$p_2 = 2\frac{A_o p_1}{k} = 2\omega_{u,loop}$$

$$\phi_m = 90^\circ - \tan^{-1}\frac{\omega_{u,loop}}{p_2}$$

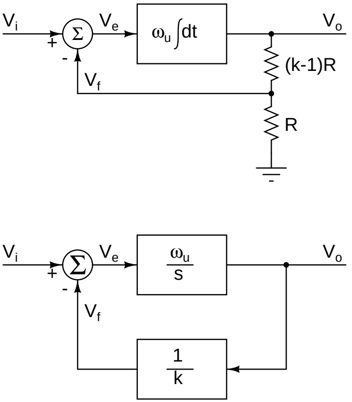
$$= 63.5^\circ$$

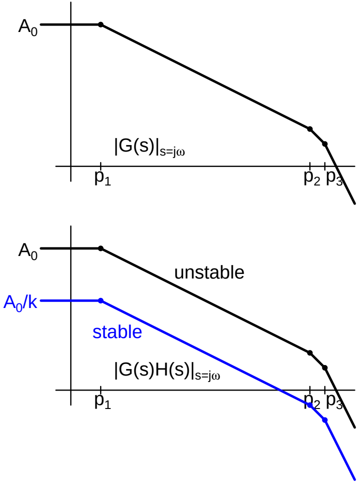
Two pole example

Phase margin of 60°

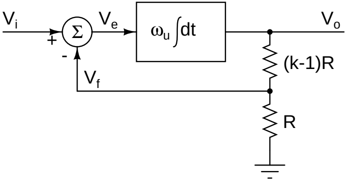
$$
\begin{aligned}
-90^\circ - \tan^{-1}\frac{\omega_{u,loop}}{p_2} &= -120^\circ \\
\frac{\omega_{u,loop}}{p_2} &= \frac{1}{\sqrt{3}} \\
p_2 &= \sqrt{3}\omega_{u,loop} \\
\zeta &= \frac{\sqrt{\sqrt{3}}}{2} \\
&= 0.66
\end{aligned}
$$

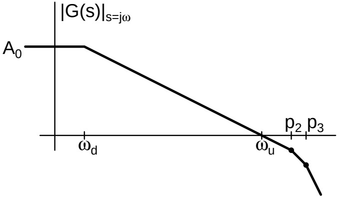
Dependence of stability on feedback factor

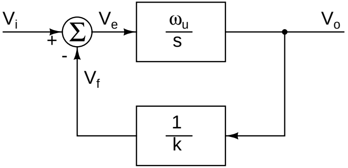


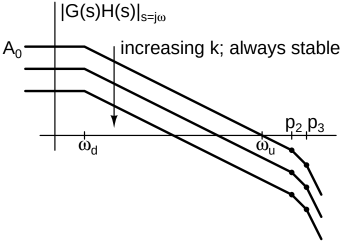


Unity gain compensation



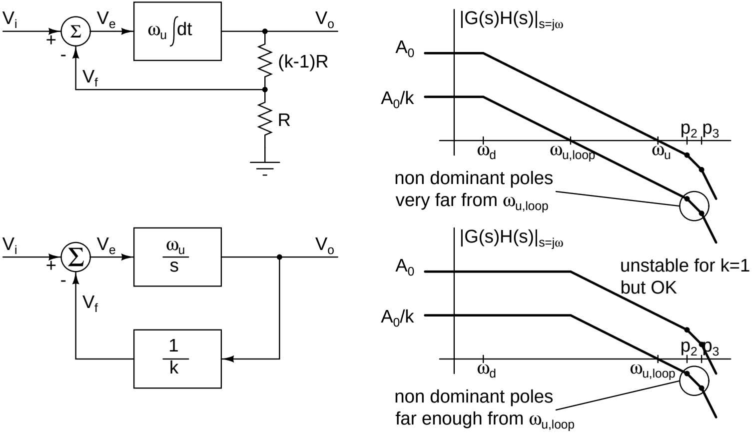






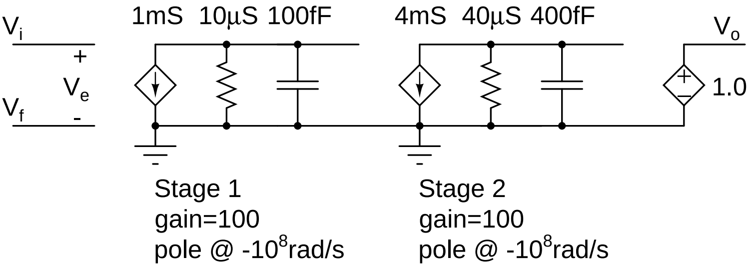
- Variable feedback factor: compensate for lowest *k*
- General purpose opamps: unity gain compensated
- e.g.: LM741, LF356, OPA656

Why not always compensate for unity gain?



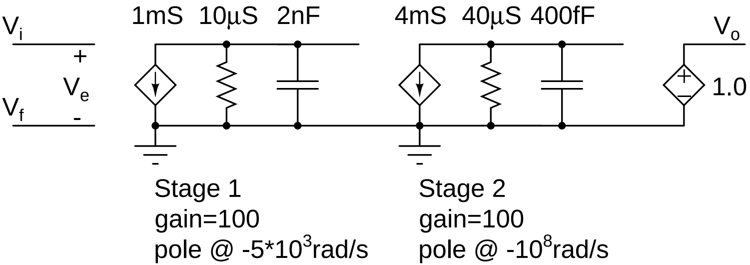
- Sub optimal bandwidth for non unity feedback
- Compensate *only* for the required feedback factor
- OPA657: compensated for feedback factors $\leq 1/8$

Two stage amplifier example



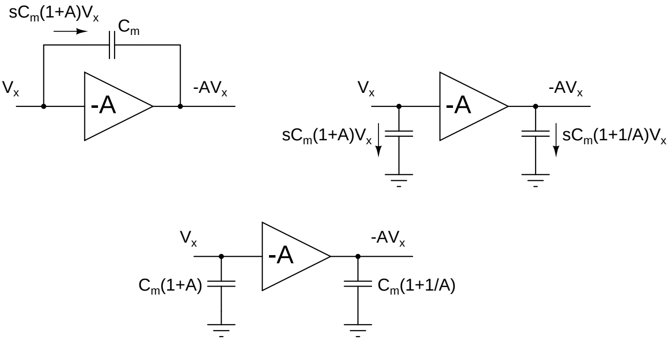
- DC gain $A_o = 10^4$ (80 dB)
- Two poles at -10^8 rad/s
- Insufficient phase margin

Dominant pole compensation



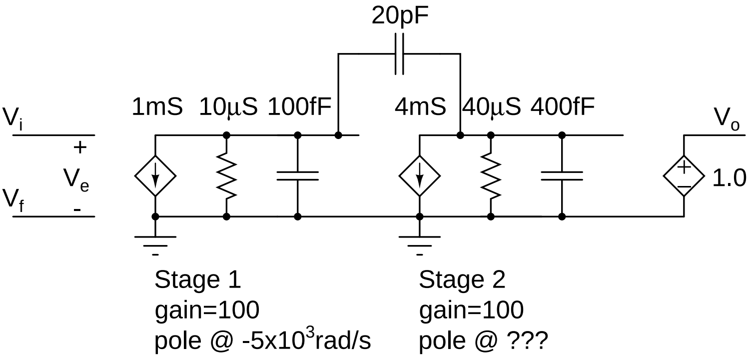
- Move one of the poles to -5×10^3 rad/s
- Other pole remains at the original frequency
- Unity gain frequency $\omega_u = 5 \times 10^7$ rad/s $= |p_2|/2$
- 2 nF compensation capacitor: too large on an IC

Miller effect



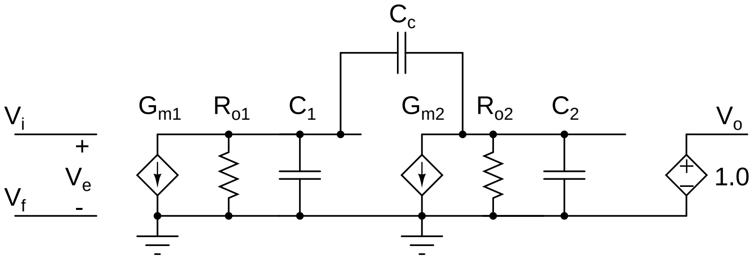
(amplifier: ideal voltage controlled voltage source)

- 2 nF can be realized using 20 pF across a gain of 100



- Dominant pole at 5×10^3 rad/s
- Simulated frequency response <u>does not show</u> the second pole at -10^8 rad/s

Miller compensated amplifier-analysis



$$\frac{V_o}{V_e} = A_o \frac{1 - \frac{sC_c}{G_{m2}}}{1 + a_1 s + a_2 s^2}$$

$$A_o = G_{m1} R_{o1} G_{m2} R_{o2}$$

$$a_1 = \frac{C_1}{G_{o1}} + \frac{C_c}{G_{o1}} \left(\frac{G_{m2}}{G_{o2}} + 1 + \frac{G_{o1}}{G_{o2}} \right) + \frac{C_2}{G_{o2}}$$

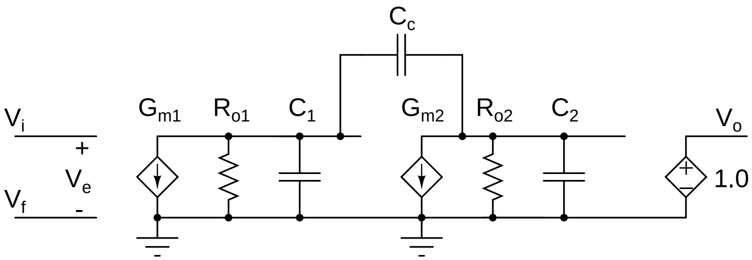
$$a_2 = \frac{C_1 C_c + C_c C_2 + C_2 C_1}{G_{o1} G_{o2}}$$

Approximate solution to a quadratic equation

$$
\begin{aligned}
a_2 s^2 + a_1 s + 1 &= 0 \\
a_1 p_1 + 1 &\approx 0 \\
p_1 &\approx -\frac{1}{a_1} \\
a_2 p_2^2 + a_1 p_1 &\approx 0 \\
p_2 &\approx -\frac{a_1}{a_2}
\end{aligned}
$$

- Works for widely separated (real) poles i.e. $|p_2| \gg |p_1|$

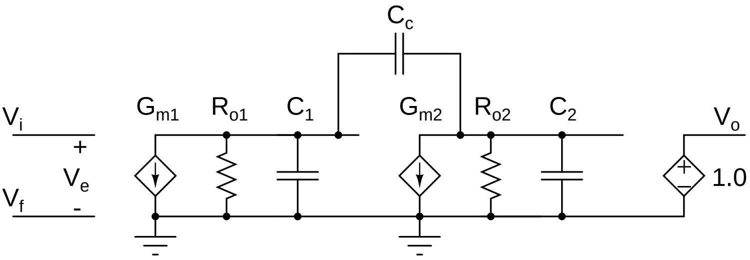
Miller compensated amplifier-analysis



$$p_1 \approx -\frac{G_{o1}}{C_1 + C_c\left(\frac{G_{m2}}{G_{o2}} + 1 + \frac{G_{o1}}{G_{o2}}\right)}$$

$$p_2 \approx -\frac{C_c\left(G_{m2} + G_{o1} + G_{o2}\right) + C_2 G_{o1} + C_1 G_{o2}}{C_1 C_c + C_c C_2 + C_2 C_1}$$

$$= -\frac{\frac{C_c}{C_c + C_1} G_{m2} + G_{o2} + \frac{C_c + C_2}{C_c + C_1} G_{o1}}{\frac{C_c C_1}{C_c + C_1} + C_2}$$



Without C_c

$$p_1 = -\frac{G_{o1}}{C_1}$$

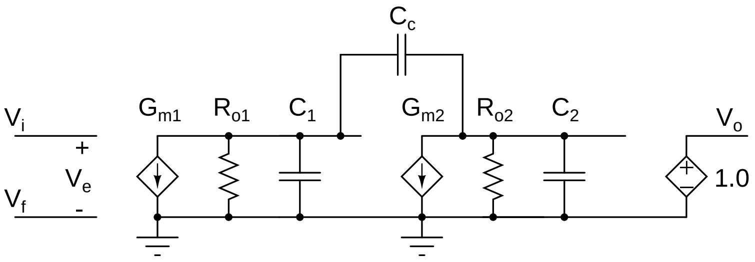
$$p_2 = -\frac{G_{o2}}{C_2}$$

With C_c

$$p_1 \approx -\frac{G_{o1}}{C_1 + C_c\left(\frac{G_{m2}}{G_{o2}} + 1 + \frac{G_{o1}}{G_{o2}}\right)}$$

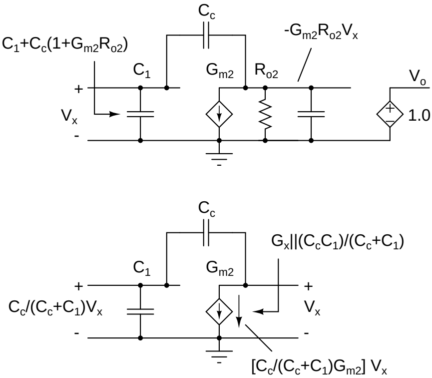
$$p_2 \approx -\frac{\frac{C_c}{C_c+C_1}G_{m2} + G_{o2} + \frac{C_c+C_2}{C_c+C_1}G_{o1}}{\frac{C_cC_1}{C_c+C_1} + C_2}$$

Miller compensated amplifier: pole splitting



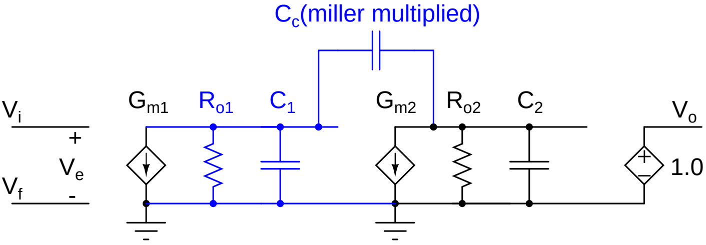
- p_1 moves to a lower frequency
- p_2 moves to a higher frequency
- Right half plane zero $z_1 = G_{m2}/C_c$; additional phase lag; reduced phase margin
- Unity gain frequency has to be lower than the *modified* p_2

Intuitive explanation

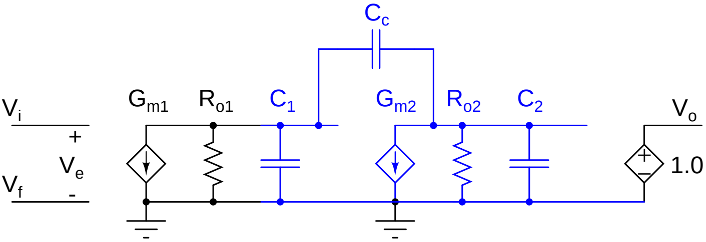


- Input capacitance increased due to miller multiplication
- Output conductance increased due to feedback around G_{m2}

Intuitive explanation

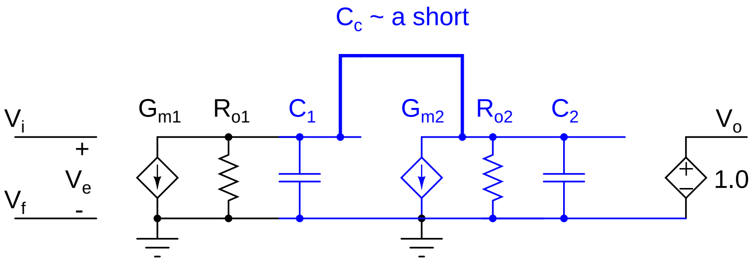


1st stage output pole $p_1 \sim -1/[R_{o1}(C_1+C_c(1+G_{m2}R_{o1}))]$



2^{nd} stage output pole $p_2 \sim -[G_{m2}(C_c/(C_1+C_c)+G_{o2}]/[C_2+C_cC_1/(C_c+C_1)]$

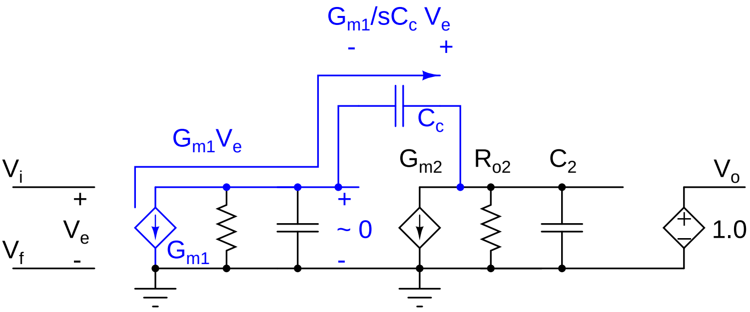
Output pole frequency



2[nd] stage output pole p_2 ~ $-G_{m2}/(C_1+C_2)$

- Crude approximation: $p_2 - \approx G_{m2}/(C_1 + C_2)$
- Works when $C_c \gg C_1$

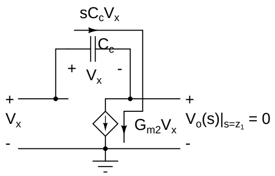
Unity gain frequency



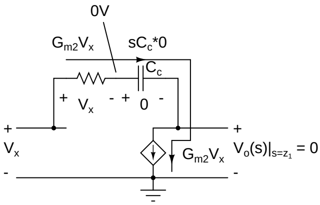
If one pole is dominant

$$
\begin{aligned}
\omega_u &\approx A_o|p_1| \\
&= G_{m1}R_{o1}G_{m2}R_{o2}\frac{G_{o1}}{C_1 + C_c\left(\frac{G_{m2}}{G_{o2}} + 1 + \frac{G_{o1}}{G_{o2}}\right)} \\
&= \frac{G_{m1}}{C_c\left(1 + \frac{G_{o2}}{G_{m2}} + \frac{G_{o1}}{G_{m2}}\right) + C_1\frac{G_{o2}}{G_{m2}}} \approx \frac{G_{m1}}{C_c}
\end{aligned}
$$

Right half plane zero



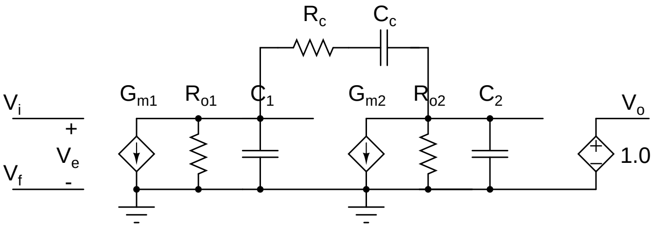
@ $s=z_1$, the zero frequency



@ $s=z_1$, the zero frequency

- Zero at G_{m2}/C_c
- Zero moves to ∞ for $R_c = 1/G_{m2}$

Tuning the zero



$$\frac{V_o(s)}{V_e(s)} = A_o \frac{1 - sC_c\left(R_f - \frac{1}{G_{m2}}\right)}{D_3(s)}$$

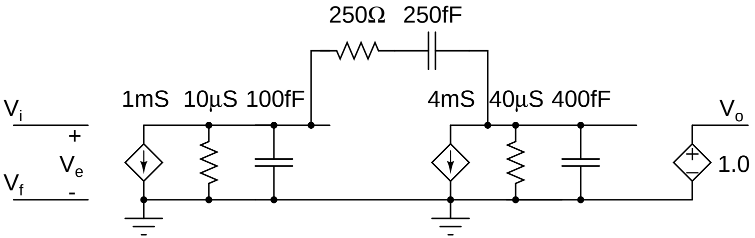
- Zero can be moved to ∞ or to LHP to cancel a non dominant pole
- Third order system-extra pole

Calculations

$$\begin{aligned}
\frac{G_{m1}}{C_c} &= \frac{1}{2} G_{m2} C_1 + C_2 \\
C_c &= 250\,\text{fF} \\
\omega_u &= \frac{G_{m1}}{C_c} = 4\,\text{Grad/s} \\
|p_2| &= \frac{G_{m2}}{C_1 + C_2} = 8\,\text{Grad/s}
\end{aligned}$$

- $C_c \gg C_1$ is not valid
- Refine the values using exact calculations/simulations
- Use $R_f = 1/G_{m2} = 250\,\Omega$ to cancel the RHP zero

Calculations



	with R_c	w/o R_c	
DC gain	10^4		
Poles	-3.92×10^5	-3.92×10^5	rad/s
	-6.88×10^9	-6.19×10^9	rad/s
	-5.93×10^{10}	—	rad/s
Zeros	∞	$+1.6 \times 10^{10}$	rad/s
ω_u	3.49×10^{10}	3.49×10^{10}	rad/s
Phase margin (unity feedback)	$60°$	$48°$	

Negative Feedback for Bias Stabilization

The Bias Stabilization Problem Determine the V_{GS} that I should apply to a MOS transistor (operating in saturation) so that the drain current $I_D = I_{ref}$.

Bias Stabilization

... involves the following tasks ....

- **Measure** the quiescent current
- **Compare** it with a reference current
- **Kick** the V_{GS} in the right direction

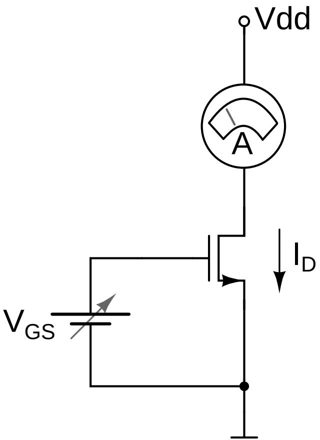
... ok, so how many ways can we do this ?

- In a MOSFET, $I_D = I_S \Rightarrow$ can measure quiescent current in two ways.
- Varying $V_{GS} \Rightarrow$ can be done in atleast two ways : keep V_S fixed & vary V_G, or viceversa.

... atleast four ways of stabilizing bias current.

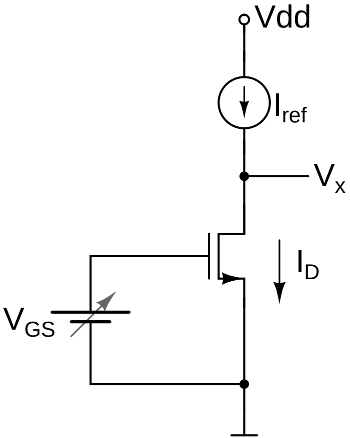
Basic Idea

Think : What will I do in a lab ?



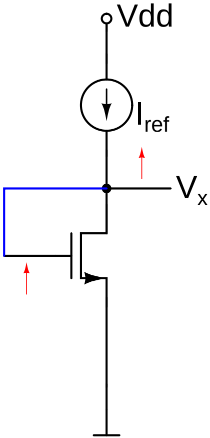
- Apply an arbitrary gate-source voltage.
- Measure I_D using an ammeter.
- Compare I_D with I_{ref}.
- If $I_D > I_{ref}$, the applied V_{GS} is too high, reduce it.
- If $I_D < I_{ref}$, the applied V_{GS} is too low, increase it.

Comparing Currents Without an Ammeter



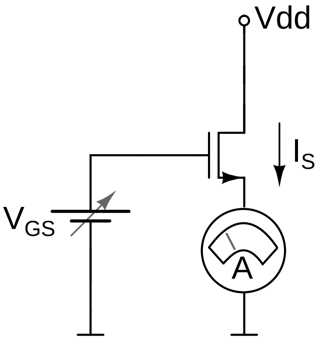
- Monitor V_x.
- If V_x increases with time, means $I_{ref} > I_D$.
- If V_x decreases with time, means $I_{ref} < I_D$.
- If $I_D > I_{ref}$, or equivalently, if V_x decreases $\Rightarrow$ the applied V_{GS} is too high, reduce it.
- If $I_D < I_{ref}$, or equivalently, if V_x increases $\Rightarrow$ the applied V_{GS} is too low, increase it.

Final Circuit



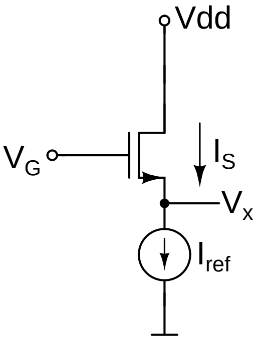
- The simple "diode-connected" transistor is a negative feedback system in disguise !
- Drain current is measured, and the V_{GS} is changed by keeping V_S fixed and varying V_G.

Measuring Current in the Source



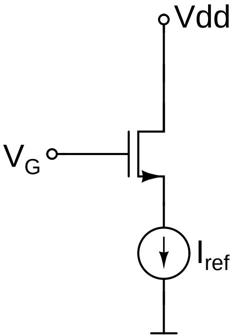
- Apply an arbitrary gate-source voltage.
- Measure I_S using an ammeter.
- Compare I_S with I_{ref}.
- If $I_S > I_{ref}$, the applied V_{GS} is too high, reduce it.
- If $I_S < I_{ref}$, the applied V_{GS} is too low, increase it.

Comparing Currents Without an Ammeter



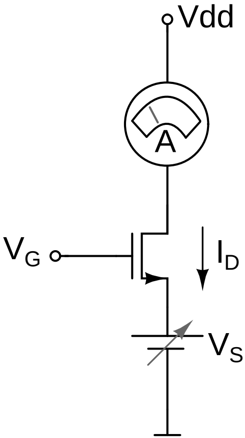
- Monitor V_x.
- If V_x increases with time, means $I_S > I_{ref}$.
- If V_x decreases with time, means $I_S < I_{ref}$.
- If $I_S > I_{ref}$, or equivalently, if V_x increases $\Rightarrow$ the applied V_{GS} is too high, reduce it.
- If $I_S < I_{ref}$, or equivalently, if V_x decreases $\Rightarrow$ the applied V_{GS} is too low, increase it.

Final Circuit



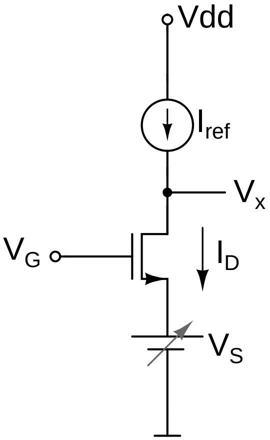
- Source current is measured, and the V_{GS} is changed by keeping V_G fixed and varying V_S.

Bias Stabilization : Measure I_D & Vary V_S



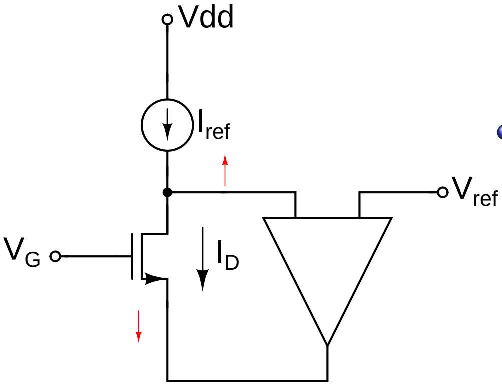
- Keep V_G fixed, apply an arbitrary source voltage.
- Measure I_D using an ammeter.
- Compare I_D with I_{ref}.
- If $I_D > I_{ref}$, the applied V_{GS} is too high, **increase** V_S.
- If $I_D < I_{ref}$, the applied V_{GS} is too low, **decrease** V_S.

Comparing Currents Without an Ammeter



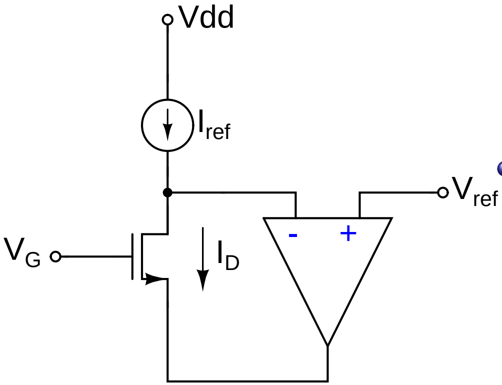
- Monitor V_x.
- If V_x increases with time, means $I_{ref} > I_D$.
- If V_x decreases with time, means $I_{ref} < I_D$.
- If $I_D < I_{ref}$, or equivalently, if V_x increases $\Rightarrow$ the applied V_{GS} is too high, increase V_S.
- If $I_D > I_{ref}$, or equivalently, if V_x decreases $\Rightarrow$ the applied V_{GS} is too low, decrease V_S.

Final Circuit



- Drain current is measured, and the V_{GS} is changed by keeping V_G fixed and varying V_S.

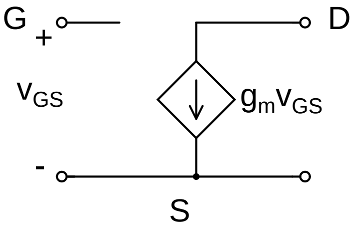
Final Circuit



- Opamp signs come out automatically.

Negative Feedback in Single Transistor Circuits

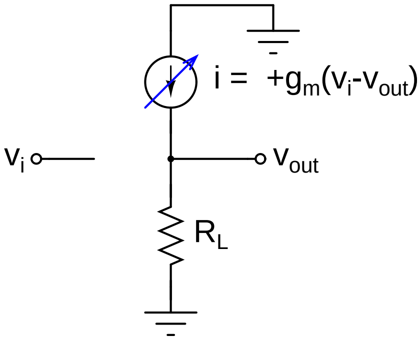
The Incremental MOSFET Equivalent Circuit



- A MOSFET biased in saturation is an incremental voltage controlled current source
- **In principle**, g_m can be made as large as one wants

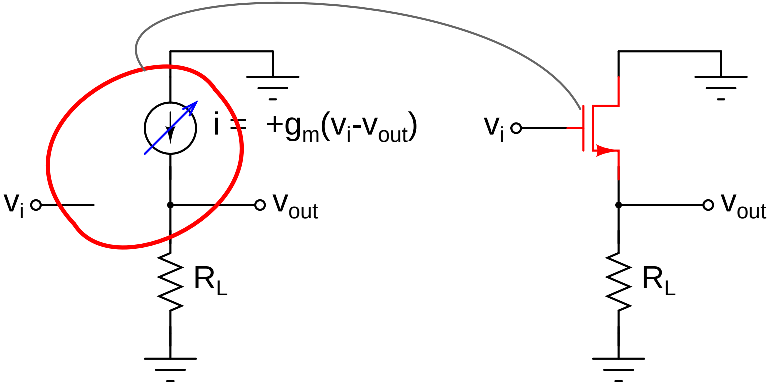
Making an Incremental VCVS with Gain=1

How do you make a VCVS when all you have is a variable current source ?



- Want $v_{out} = v_i$
- **Measure** v_{out}
- **Compare** it to v_i
- If $v_{out} < v_i$, pump current **into** v_{out}
- If $v_{out} > v_i$, pump current **out of** v_{out}
- The current source is controlled by $(v_i - v_{out})$

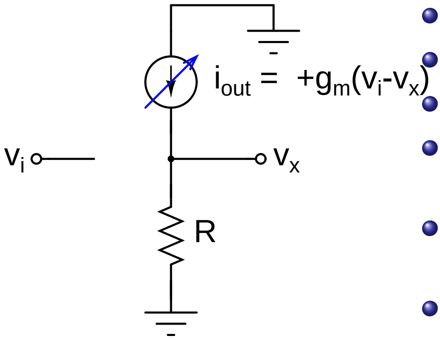
Identify the Transistor → Common Drain Stage



If $g_m \to \infty$, $v_{out} = v_i$, $R_{out} = 0$

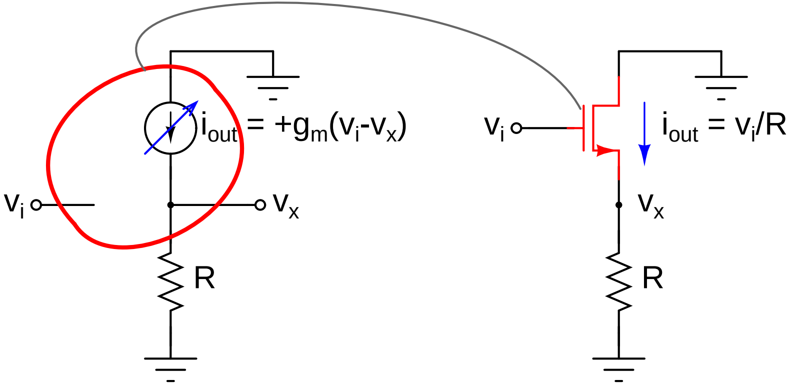
Make a VCCS with Transconductance of $1/R$

How do you make a VCCS when all you have is a variable current source ?



- Want $i_{out} = v_i/R$
- **Measure** $i_{out}R$, call it v_x
- **Compare** v_x to v_i
- If $v_x < v_i$, pump current **into** R
- If $v_x > v_i$, pump current **out of** R
- The current source is controlled by $(v_i - v_x)$

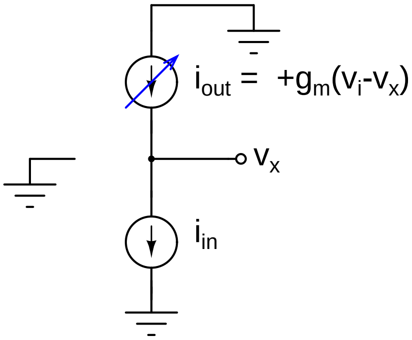
Identify the Transistor → Transconductance Stage



$$\text{If } g_m \rightarrow \infty,\ i_{out} = v_i/R$$

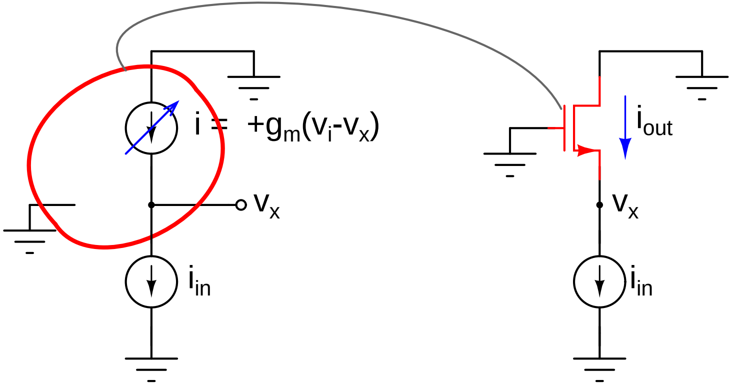
Make a CCCS with gain of 1

How do you make a CCCS when all you have is a variable current source ?



- Want $i_{out} = i_{in}$
- **Measure** potential v_x
- **Compare** v_x to 0
- If $v_x < 0$, i_{out} is too small, increase i_{out}
- If $v_x > 0$, i_{out} is too big, decrease i_{out}.
- The current source is controlled by $(0 - v_x)$

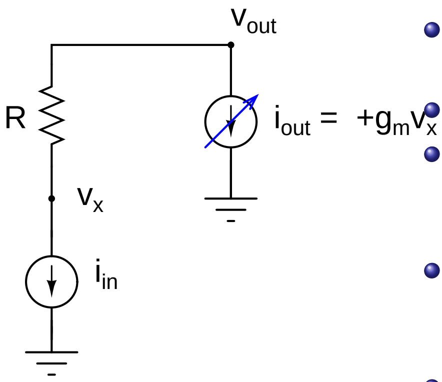
Identify the Transistor → Common Gate Stage



If $g_m \to \infty$, $i_{out} = v_i/R$

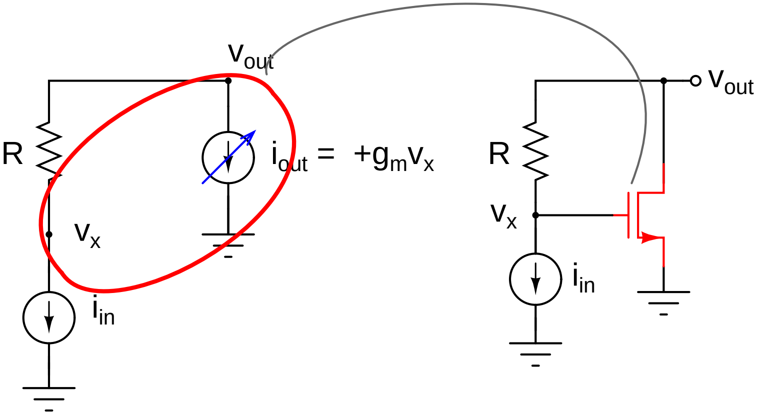
Make a CCVS with transimpedance R

How do you make a CCVS when all you have is a variable current source ?



- Want $v_{out} = i_{in}R$
- **Measure** $v_{out} - i_{in}R$, call it v_x
- **Compare** v_x to 0
- If $v_x > 0$, it means v_{out} is too high, pump current **out of** v_{out}
- If $v_x < 0$, it means v_{out} is too low, pump current **into** v_{out}
- The current source is controlled by v_x

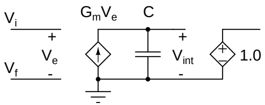
Identify the Transistor → Transimpedance Stage

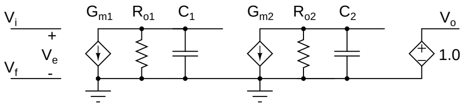


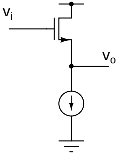
$$\text{If } g_m \rightarrow \infty,\ v_{out} = i_{in}R$$

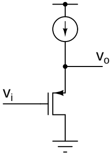
CMOS implementations

Negative feedback amplifier: Realization

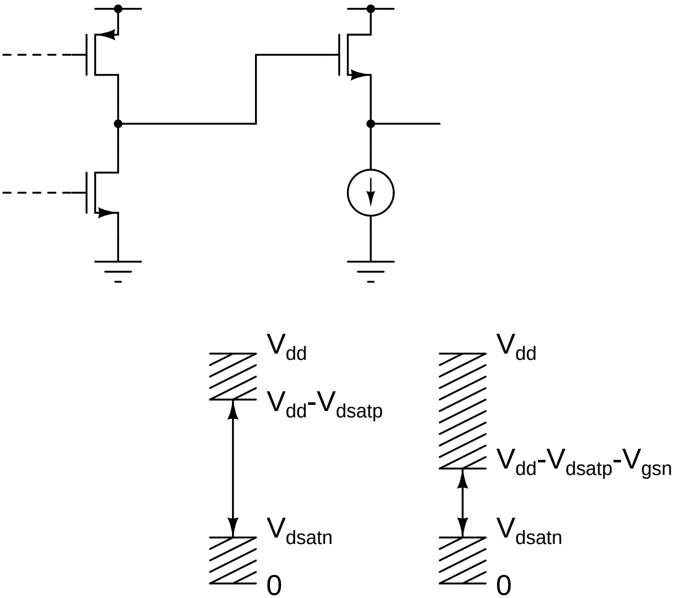




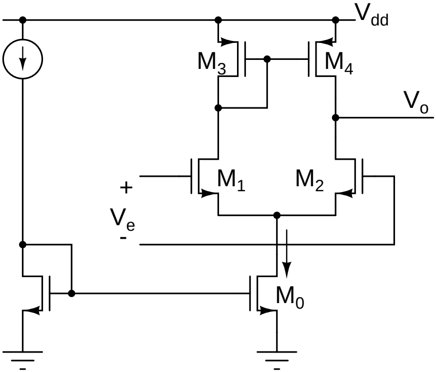


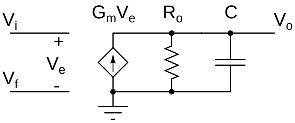


Buffers in CMOS



Single stage opamp



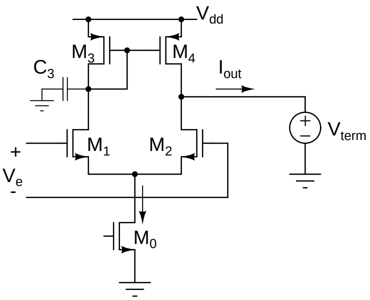


$M_1 = M_2$

$M_3 = M_4$

- $R_o = r_{ds1} || r_{ds3} || R_L$
- $C = C_{p,out} + C_L$
- $g_m = g_{m1}$
- $A_o = g_{m1} R_o$

Single stage opamp



$$\frac{I_{out}(s)}{V_e(s)} = g_{m1}\frac{1+s\frac{C_3}{2g_{m3}}}{1+s\frac{C_3}{g_{m3}}}$$

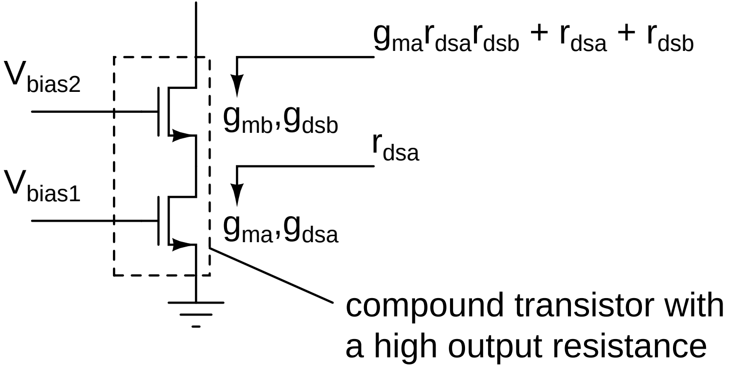
- Pole zero pair due to two paths

Single stage opamp-summary

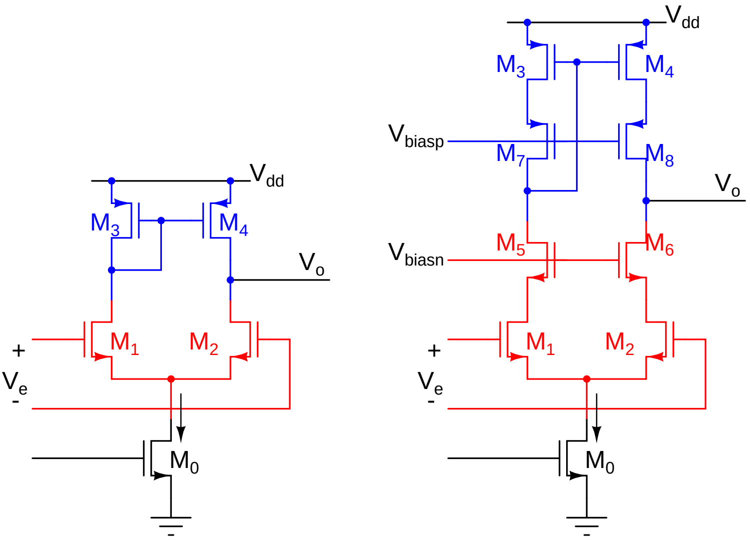
dc gain A_o	$g_{m1}/(g_{ds1}+g_{ds3})$
Unity gain frequency ω_u	$g_{m1}/(C_L+C_o)$
Additional poles/zeros	$p_2 = -g_{m3}/C_3$ $z_1 = -2g_{m3}/C_3$

- $A_o \sim g_m/g_{ds}$
- Increase dc gain by increasing L
- A_o limited to about 100
- Increase phase margin by increasing C_L
- Not preferred with resistive loads

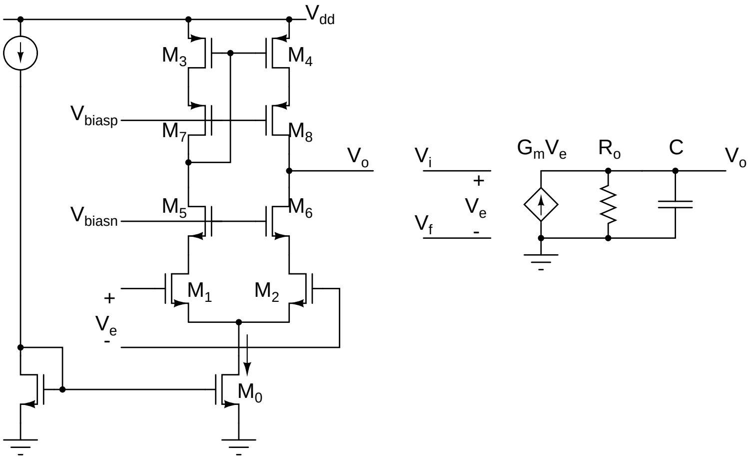
Cascode transistor



Telescopic cascode opamp



Telescopic cascode opamp

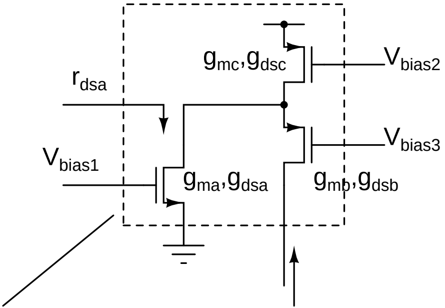


Telescopic cascode opamp-summary

$$
\begin{aligned}
A_o &\approx \frac{g_{m1}}{g_{ds1}g_{ds5}/g_{m5} + g_{ds3}g_{ds7}/g_{m7}} \\
\omega_u &= g_{m1}/(C_L + C_o) \\
p_2 &= -g_{m3}/C_3 \\
z_1 &= -2g_{m3}/C_3 \\
p_{3-6} &\sim g_{mx}/C_{px}
\end{aligned}
$$

- $A_o \sim (g_m/g_{ds})^2$
- $A_o \sim 10^4$ possible
- Increase phase margin by increasing C_L
- Not preferred with resistive loads

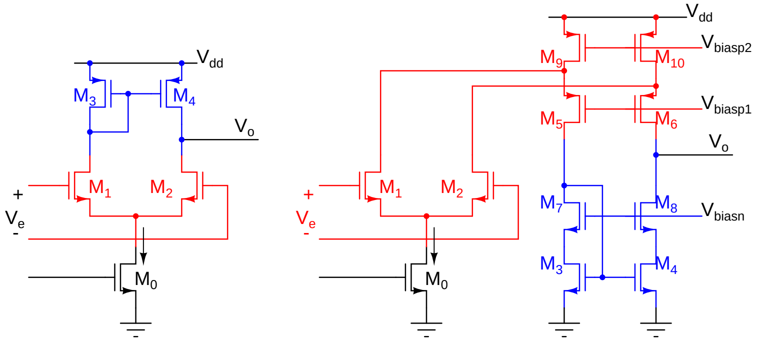
Folded cascode stage



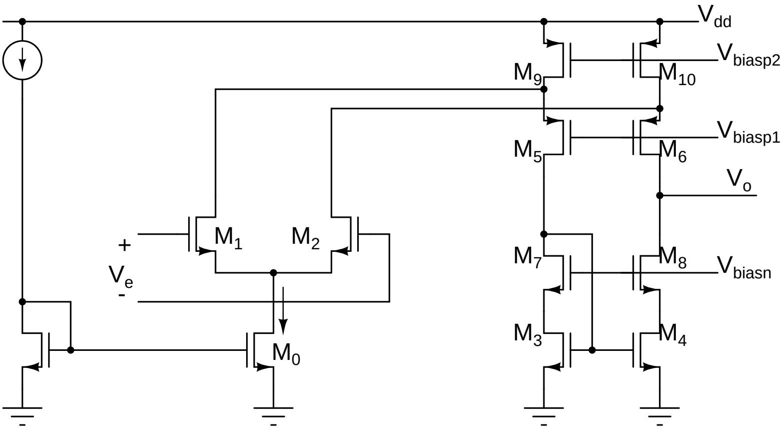
compound transistor with a high output resistance

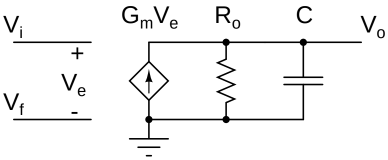
$g_{ma}(r_{dsa} || r_{dsc}) r_{dsb} + (r_{dsa} || r_{dsc}) + r_{dsb}$

Folded cascode opamp



Folded cascode opamp



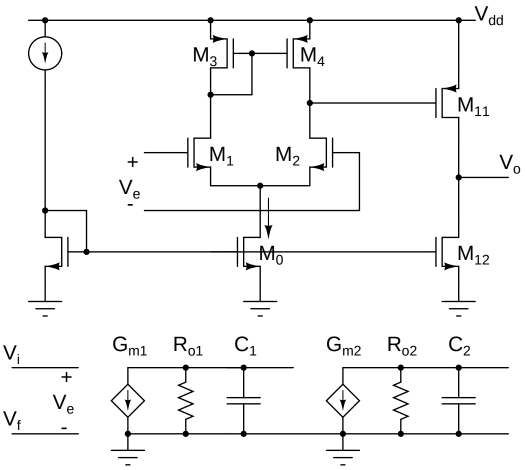


Folded cascode opamp-summary

$$
\begin{aligned}
A_o &\approx \frac{g_{m1}}{(g_{ds1}+g_{ds9})g_{ds5}/g_{m5}+g_{ds3}g_{ds7}/g_{m7}} \\
\omega_u &= g_{m1}/(C_L+C_o) \\
p_2 &= -g_{m3}/C_3 \\
z_1 &= -2g_{m3}/C_3 \\
p_{3-6} &\sim g_{mx}/C_{px}
\end{aligned}
$$

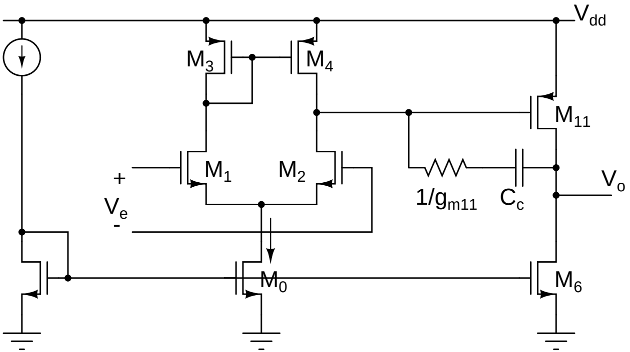
- $A_o \sim (g_m/g_{ds})^2$
- $A_o \sim 10^4$ possible
- Increase phase margin by increasing C_L
- Not preferred with resistive loads

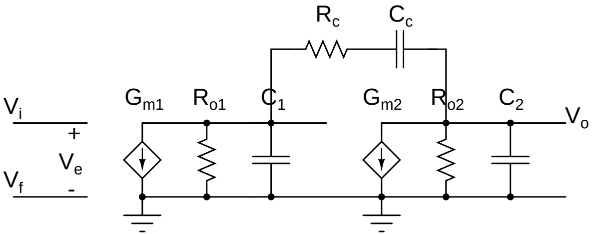
Two stage opamp



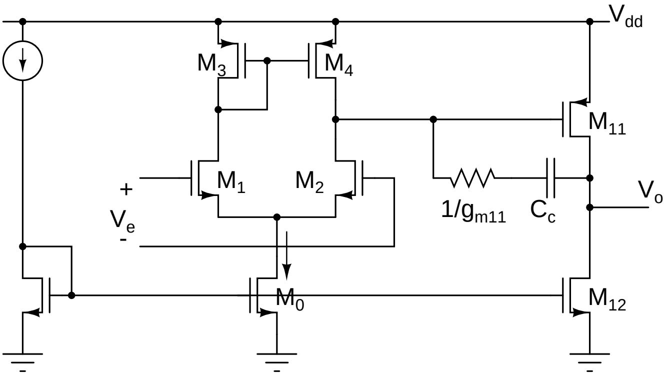
$$G_{m1} = g_{m1}$$
$$R_{o1} = r_{ds1}||r_{ds3}$$
$$G_{m2} = g_{m11}$$
$$R_{o2} = r_{ds11}||r_{ds12}||R_L$$
$$C_2 = C_{p,out} + C_L$$

Two stage opamp with compensation





Two stage opamp with compensation

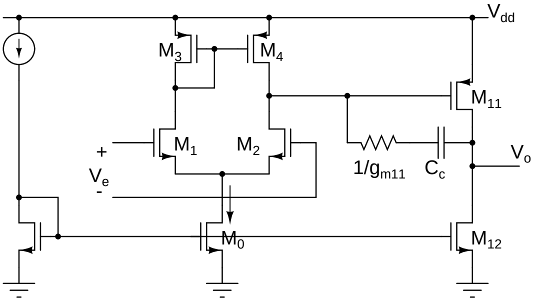


$$A_o = g_{m1}\left(r_{ds1}||r_{ds3}\right)g_{m11}\left(r_{ds11}||r_{ds11}||R_L\right) \qquad \omega_u = \frac{g_{m1}}{C_c}$$

$$p_2 = -\frac{\frac{C_c}{C_c+C_1}g_{m11}}{\frac{C_cC_{o1}}{C_c+C_{o1}}+C_L} \qquad p_3 = -g_{m3}/C_3$$

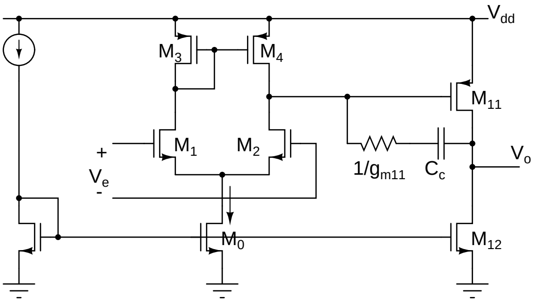
$$z_1 = -2g_{m3}/C_3$$

Two stage opamp design for a given C_L, ω_u



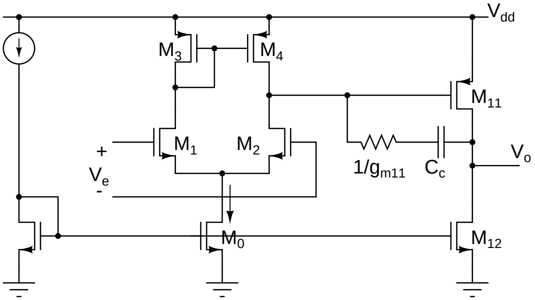
- Choose g_{m11} such that $g_{m11}/C_L > \omega_u$ (say $2.5\omega_u$)
- Choose g_{m1} and C_c such that $g_{m1}/C_c = \omega_u$
- Scale down g_{m1} and C_c until specs deteriorate (phase margin, noise)
- Iterate with a different value of g_{m11} to reach an optimum

Two stage opamp design for a given R_L, C_L, ω_u



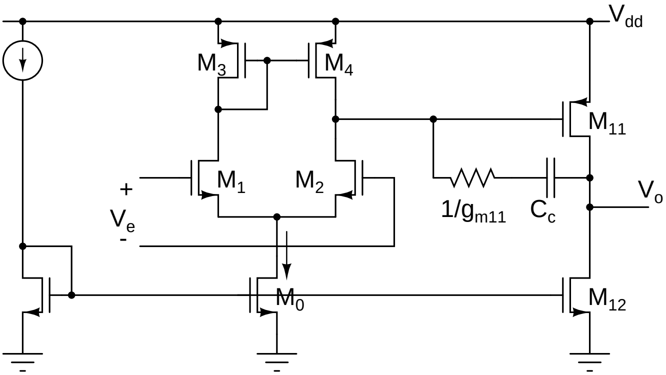
- Constraints for g_{m11}
  - $g_{m11}/C_L > \omega_u$ (say $2.5\omega_u$)
  - $g_{m11}R_L$ enough to reduce the first stage swing
- Choose g_{m1} and C_c such that $g_{m1}/C_c = \omega_u$
- Scale down g_{m1} and C_c until specs deteriorate
- Iterate with a different value of g_{m11} to reach an optimum

Two stage opamp design for an internal load and ω_u

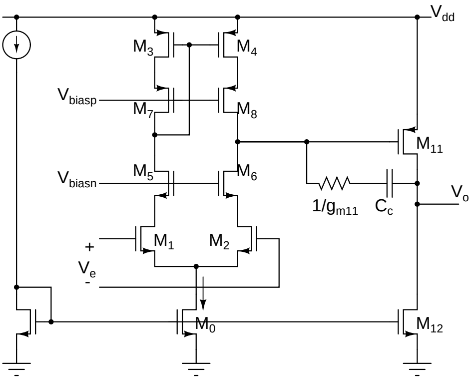


- Assume an internal load (e.g. an identical stage)
- Choose g_{m11} such that $g_{m11}/C_L > \omega_u$ (say $2.5\omega_u$)
- Choose g_{m1} and C_c such that $g_{m1}/C_c = \omega_u$
- Scale down stages until specs deteriorate

Two stage opamp design-obtaining dc gain

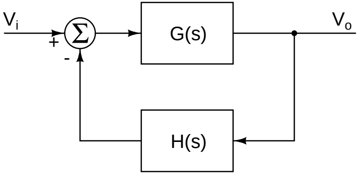


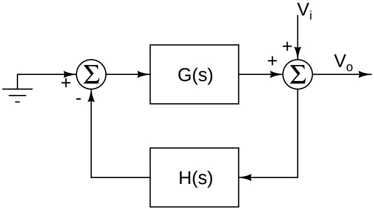
- Second stage $\sim$ min. length, esp. with heavy loads
- Optimize first stage for dc gain (L_{MOS})



- Use a telescopic cascode first stage
- $A_o \sim (g_m/g_{ds})^3$

Three stage opamp

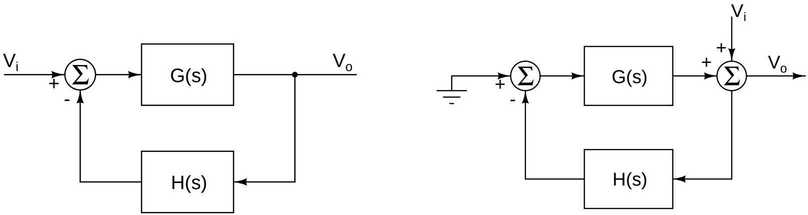




$$\frac{V_o(s)}{V_i(s)} = \frac{G(s)}{1+G(s)H(s)} = \frac{1}{H(s)}\frac{G(s)H(s)}{1+G(s)H(s)} = \frac{1}{H(s)}\frac{1}{1+\frac{1}{G(s)H(s)}}$$

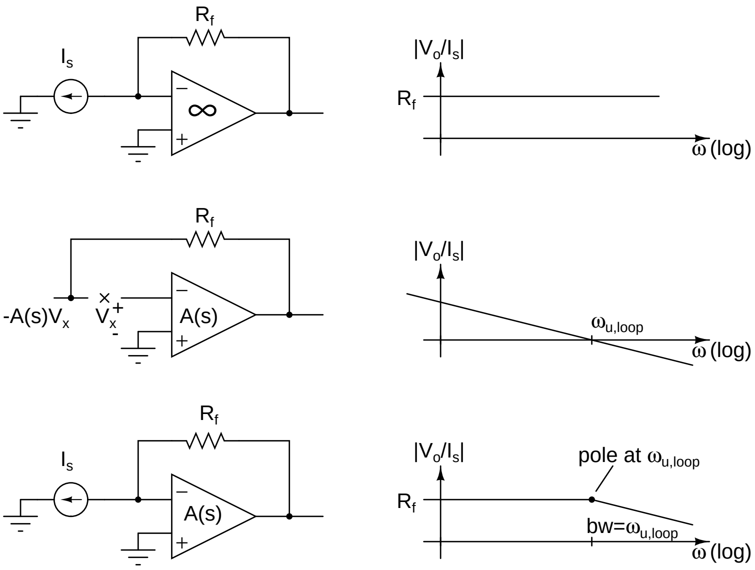
$$\frac{V_o(s)}{V_i(s)} = \frac{G(s)H(s)}{1+G(s)H(s)} = (1)\frac{G(s)H(s)}{1+G(s)H(s)} = (1)\frac{1}{1+\frac{1}{G(s)H(s)}}$$

Effect of loop gain

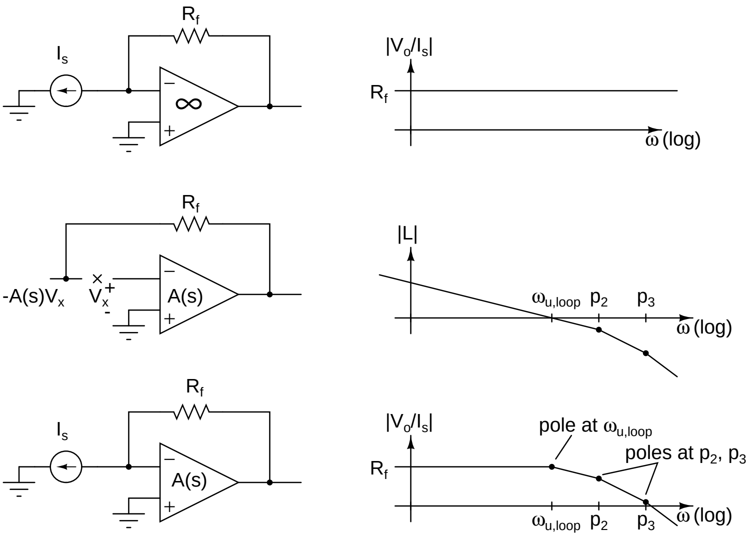


$$
\begin{aligned}
\frac{V_o(s)}{V_i(s)} &= H_{ideal}(s)\frac{1}{1+\frac{1}{L}} \\
&= H_{ideal}(s) \qquad |L| \gg 1 \\
&= H_{ideal}(s)L(s) \qquad |L| \ll 1
\end{aligned}
$$

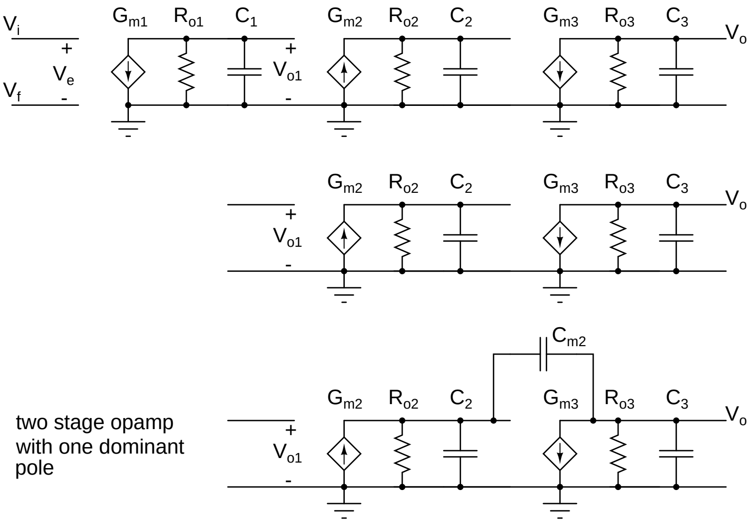
Effect of loop gain



Effect of loop gain

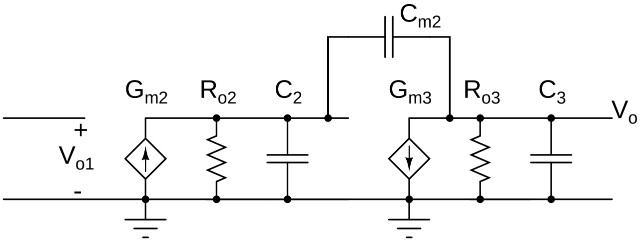


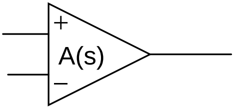
Three stages in cascade

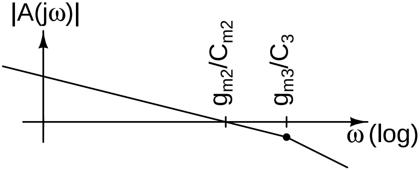


two stage opamp with one dominant pole

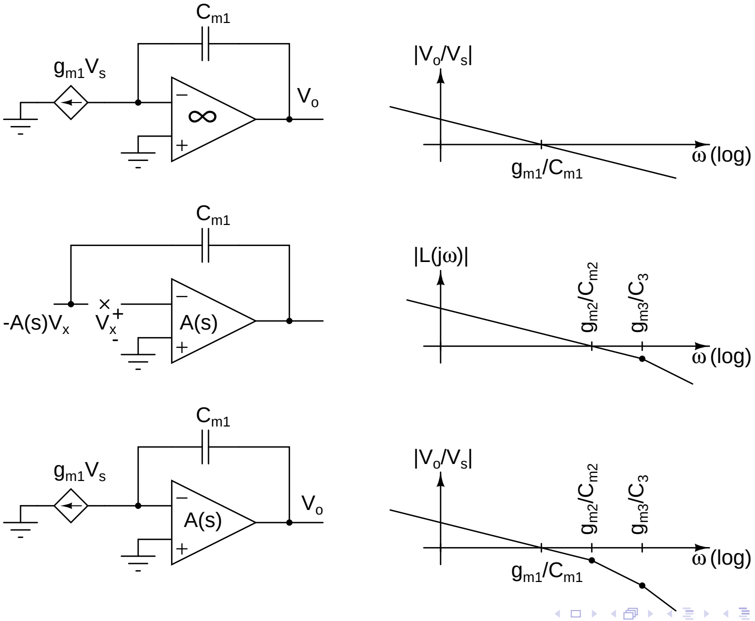
Frequency response of compensated last two stages



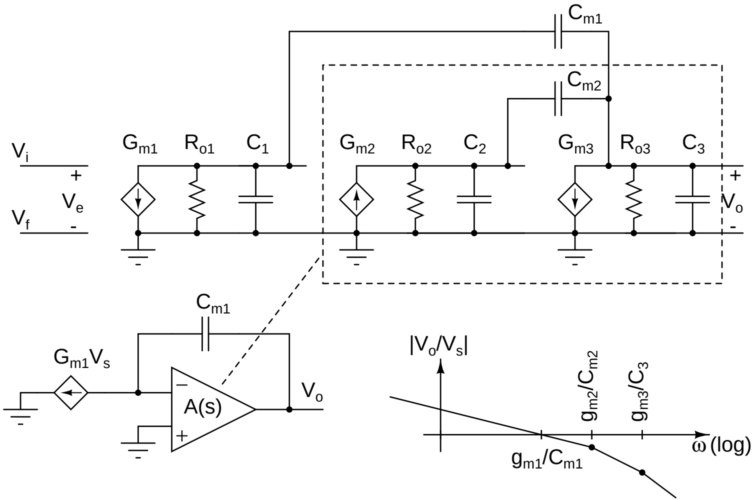




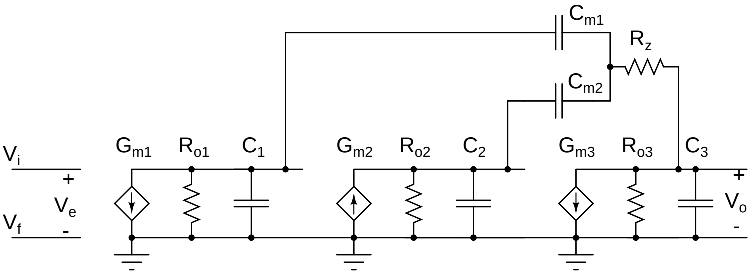
Three stage opamp equivalent circuit



Three stage opamp



RHP zero cancellation



- Has two zeros
- Approximate cancellation

Three stage opamp design for a given C_L, ω_u

$$\frac{G_{m3}}{C_L} > \omega_u$$

- Compensate the last two stages using C_{m2}

$$\frac{G_{m3}}{C_L} > \frac{G_{m2}}{C_{m2}} \quad ; \quad \frac{G_{m2}}{C_{m2}} > \omega_u$$

- Compensate the opamp using C_{m1}

$$\frac{G_{m1}}{C_{m1}} = \omega_u$$

- Scale down G_{m1} and C_{m1} within constraints (noise, phase margin)
- Scale down G_{m2} and C_{m2} within constraints (phase margin)

Three stage opamp design for a given R_L, C_L, ω_u

$$\frac{G_{m3}}{C_L} > \omega_u$$
$$G_{m3}R_L \sim 5$$

- $G_{m3}R_L$ sufficiently high to reduce internal swing
- Remaining steps as before

Three stage opamp design

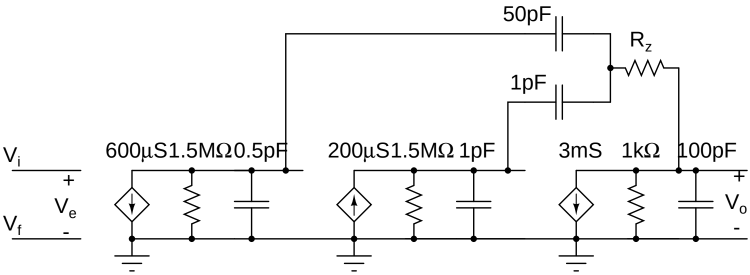
- Analytical expression very complicated—approximate
- Use above approximation as the starting point
- More optimization through simulation
  - Scale down G_m, C until constrained
  - Complex zeros may be better

Three stage opamp for a 16b audio DAC

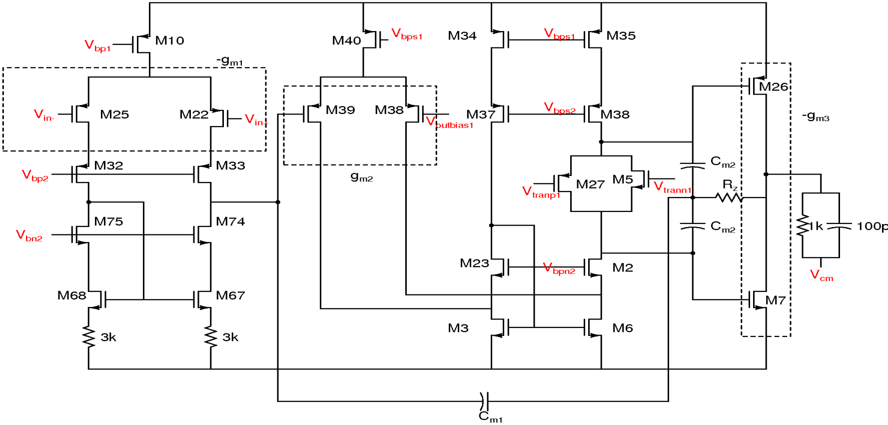
Specifications

A_o	100 dB
ω_u	1.75 MHz
R_L	1 kΩ
C_L	100 pF
Input ref. noise	3 μV rms (100 Hz-24 kHz)
Output swing	$1.5V_{ppd}^2$
V_{dd}	1.8 V
Technology	0.18 μm CMOS

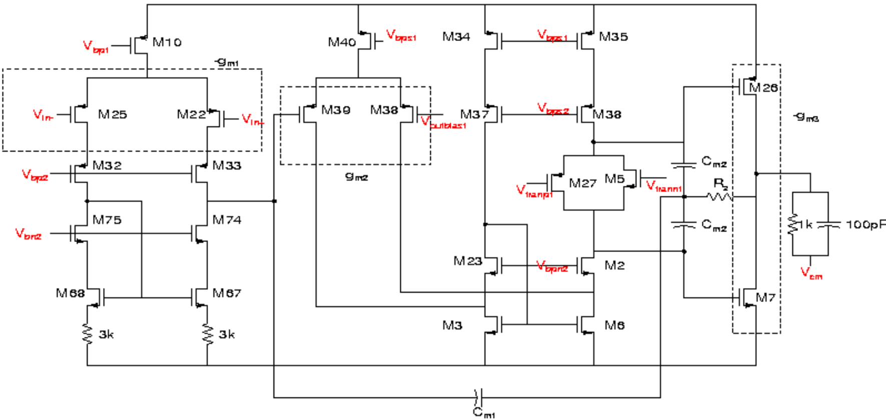
Three stage opamp for a 16b audio DAC



Three stage opamp for a 16b audio DAC

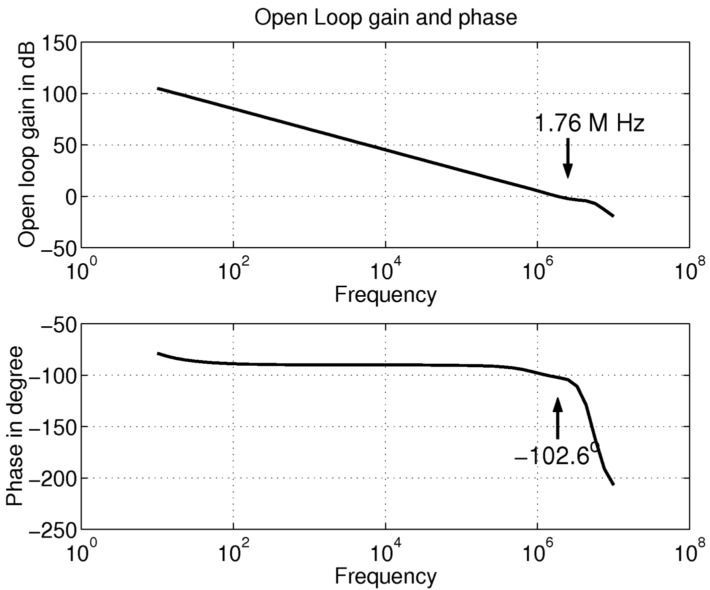


Three stage opamp for a 16b audio DAC

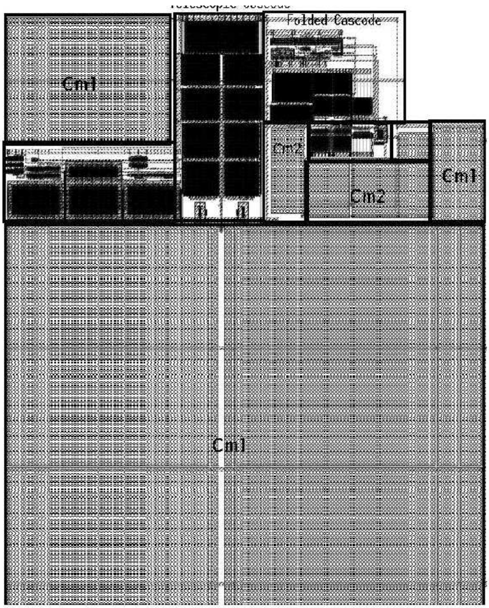


First-stage	Second-stage	
M10: 200(1μ/1μ) M22, M25, M32, M33 : 100(1μ/1μ) M75, M74, M68, M67 : 100(1.2μ/1μ)	M40 : 300(.5μ/0.25μ) M38, M39 : 20(1μ/1μ) M34, M35, M37, M38 : 80(0.5μ/.25μ) M23, M2 : 20(0.24μ/0.18μ) M79, M62 : 72(0.24μ/0.18μ)	M5, M27 : 0.45μ/0.18μ M7 : 30(0.24μ/0.18μ) M26 : 72(0.24μ/0.18μ)

Three stage opamp for a 16b audio DAC



Three stage opamp for a 16b audio DAC



Three stage opamp for a 16b audio DAC

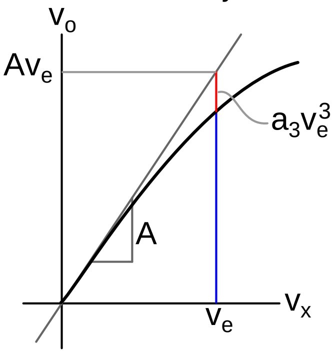
Specification	Value
Supply	1.8 V ($\pm$5%)
Loading Condition	100 pF // 1 kΩ
Technology	0.18-μm CMOS
DC-gain	105 dB
Phase Margin	77.4^o
UGF(MHz)	1.76
Output Swing	$0.2 \leq V_{out} \leq 1.6$
Slew Rate	$\pm$ 1 V/μs
THD @ 1 kHz input	-96.65 dB
C_{m1}	50 pF
C_{m2}	1 pF
Power(μW)	349 μW
Total Area	237$\times$297 μm^2 (70389μm^2)
Operational Amplifier Area	10109μm^2
Compensation Capacitance Area	60280μm^2

Amplifier Nonlinearity in Negative Feedback Systems

Nonlinearity in the Forward Amplifier

- Transistor stages are used to realize high gain
  Transistors are nonlinear $\Rightarrow$ The forward amplifier is nonlinear
- Assume fully differential operation $\Rightarrow$ only odd order nonlinearity
- Assume weak nonlinearity
- The transfer curve is approximated as
  $v_{out} = Av_x - a_3 v_x^3$
- Weak nonlinearity $\Rightarrow Av_x >> a_3 v_x^3$

Weak Nonlinearity

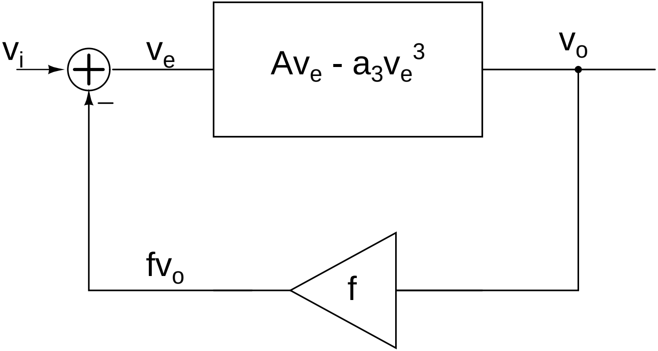


- Difference between the output of a linear amplifier with slope *A* and the nonlinear amplifier is relatively small

What does nonlinearity do to Amplifiers ?

- The transfer curve is $v_{out} = Av_x - a_3 v_x^3$
- Assume the amplifier is excited with input $V_{max}\,\sin(\omega t)$
- $v_{out} \approx AV_{max}\sin(\omega t) - \frac{a_3}{4}V_{max}^3\,\sin(3\omega t)$
- $HD_3 \approx \frac{a_3}{4A}V_{max}^2$
- What happens to distortion when this amplifier is embedded in a feedback loop ?

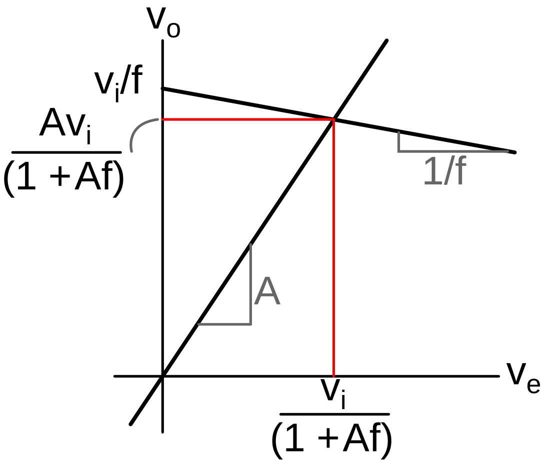
Nonlinear Forward Amplifier



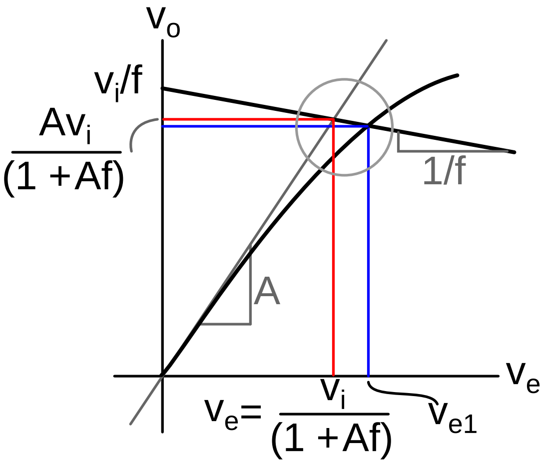
What is v_o versus v_i ?

Graphical Technique: The Linear Case

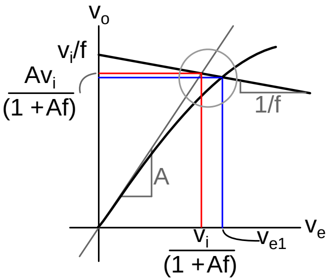
Motivation : A picture is worth a thousand equations

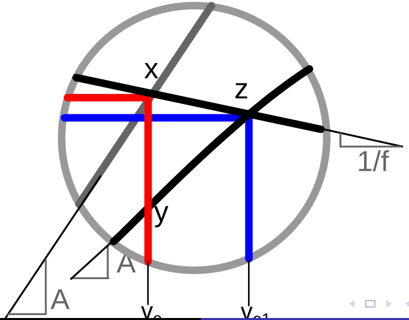


Graphical Technique : The Nonlinear Case

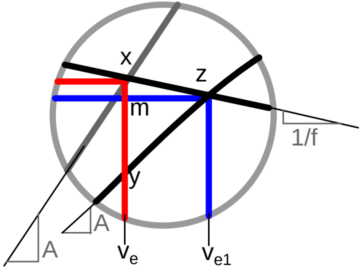


Graphical Technique : The Nonlinear Case





Graphical Technique : The Nonlinear Case

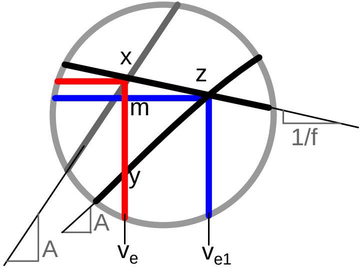


x : output of system with linear amp

z : output of system with nonlinear amp

- $v_e = \frac{v_i}{1+Af}$
- x : (v_e, Av_e)
- y : $(v_e, Av_e - a_3 v_e^3)$
- **Assumption** : Slope of the curve is A

Graphical Technique : The Nonlinear Case

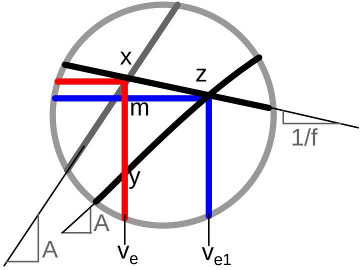


x : output of system with linear amp

z : output of system with nonlinear amp

- xy = xm + my = $a_3 v_e^3$
- xm = $(v_{e1} - v_e)/f$
- my = $A(v_{e1} - v_e)$
- $(v_{e1} - v_e)(\frac{1}{f} + A) = a_3 v_e^3$
- $v_o = Av_e - xm = Av_e - (v_{e1} - v_e)/f$

Graphical Technique : The Nonlinear Case

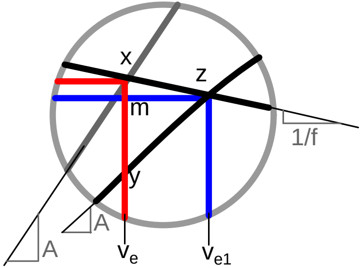


- $(v_{e1} - v_e)(\frac{1}{f} + A) = a_3 v_e^3$
- $v_{e1} = v_e + \frac{a_3 f v_e^3}{1+Af}$
- $v_o = Av_e - xm = Av_e - \frac{a_3 v_e^3}{(1+Af)}$

x : output of system with linear amp

z : output of system with nonlinear amp

Graphical Technique : The Nonlinear Case

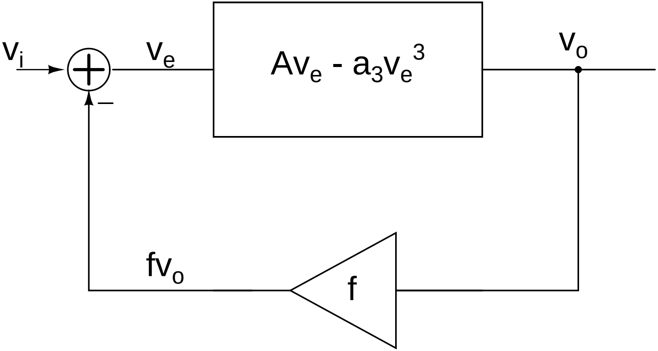


- $v_e = \frac{v_i}{1+Af}$
- $v_o = v_i \frac{1}{f} \frac{Af}{1+Af} - \frac{a_3 v_i^3}{(1+Af)^4}$

x : output of system with linear amp

z : output of system with nonlinear amp

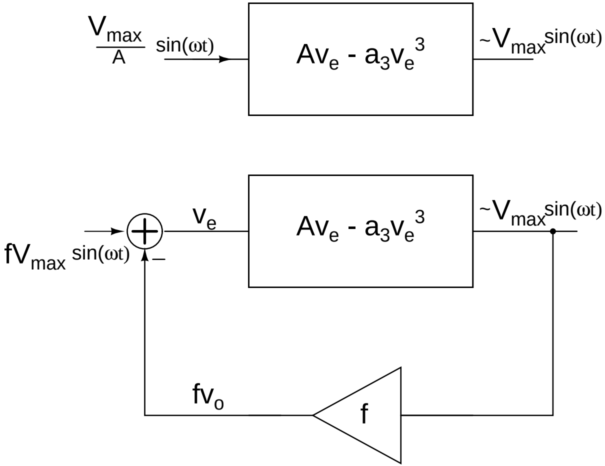
Nonlinear Forward Amplifier



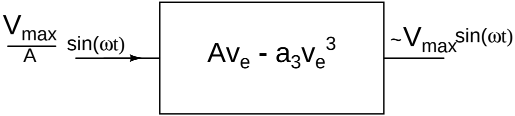
$$v_o = v_i \frac{1}{f} \frac{Af}{1+Af} - \frac{a_3 v_i^3}{(1+Af)^4}$$

Why does this make sense ?

Which System has more Output Distortion ?

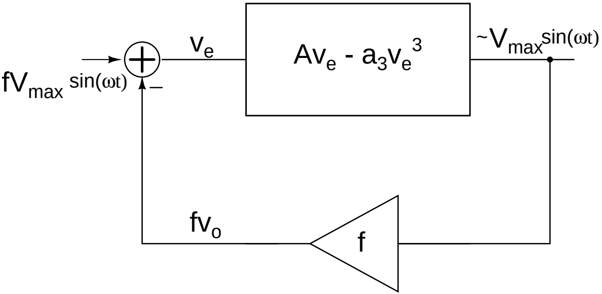


System A : Open Loop



$$\text{Third Harmonic} = \frac{a_3}{4}\left(\frac{V_{max}}{A}\right)^3$$

System B : Closed Loop



$$\text{Third Harmonic} = \frac{a_3}{4(1+Af)^4}(fV_{max})^3$$

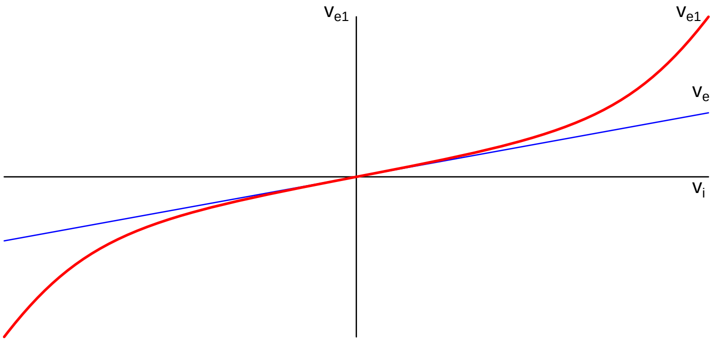
$$\approx \frac{a_3}{4}\left(\frac{V_{max}}{A}\right)^3 \frac{1}{Af}$$

System with negative feedback better by a factor of loop gain!

Why ?

v_{e1} versus v_i

$$v_{e1} = v_e + \frac{a_3 f v_e^3}{1+Af}$$



Distorion Reduction: Summary

- Negative feedback reduces distortion
- The input to the forward amplifier is very small
- The error v_e is **predistorted**
- This results in a distortion reduction by an extra factor of the loop gain, when compared to the openloop forward amplifier excited by a sinusoid with a small amplitude of the order of v_e
- Draw a picture! : gives you more insight and understanding

CASE STUDY

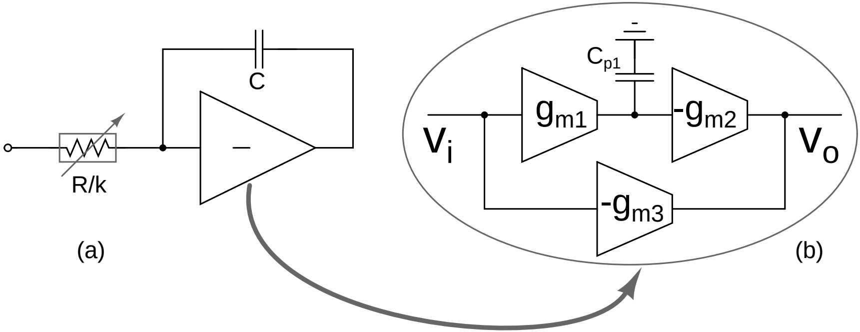
A 7X Programmable 5^{th} Order Active-RC Filter Design Targets

- VHF Active Filter
- Bandwidth programmable over a 7X range (from 44-300 MHz)
- 0.18μm CMOS process, 1.8 V supply
- Frequency response, dynamic range must be maintained over the entire programming range
- As low power as possible

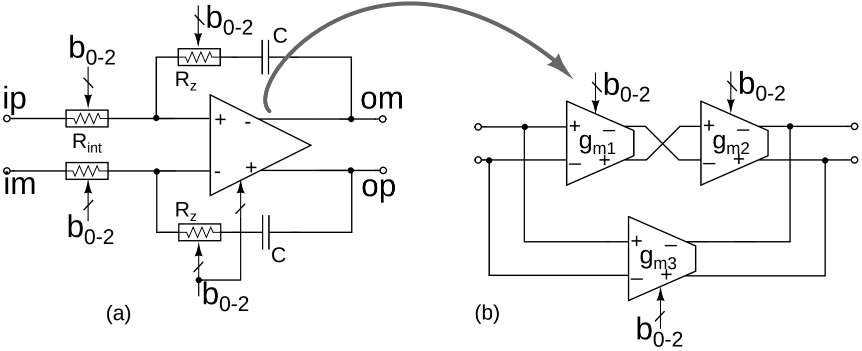
Why Active-RC ?

- Low excess noise of the integrators
- High swing possibilities
- Low distortion
- Parasitic insensitive

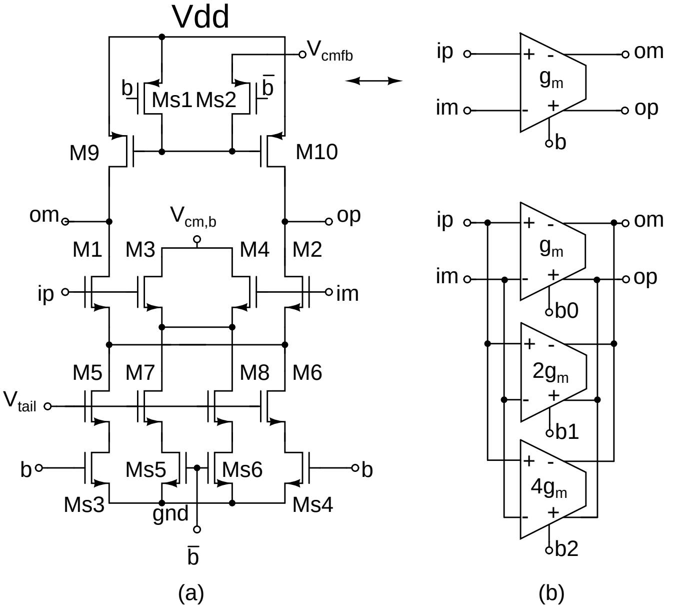
Programmable Integrator



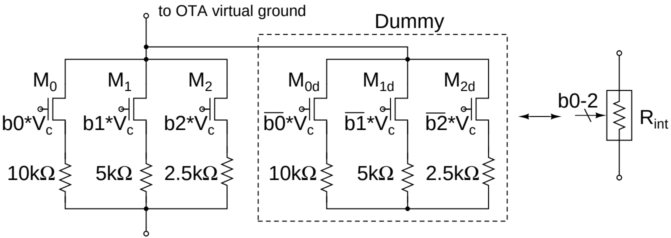
Programmable Integrator



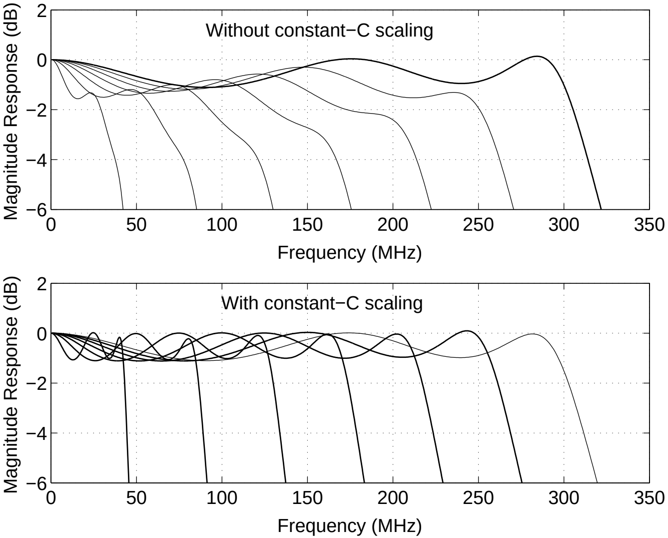
Unit Transconductor



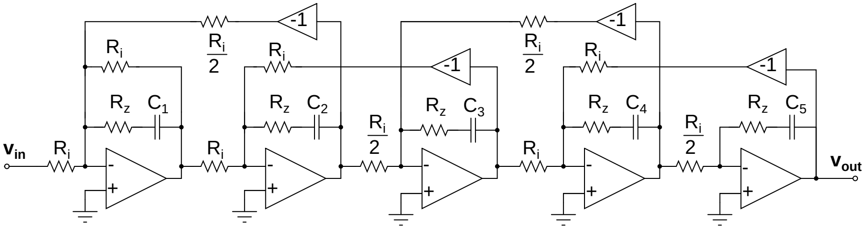
Digitally Programmable Integrating Resistor



Benefits of Constant-C Scaling

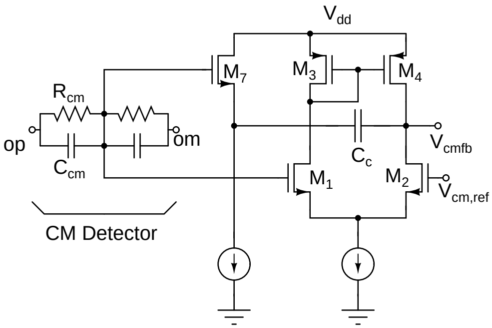


Single-ended Filter Schematic

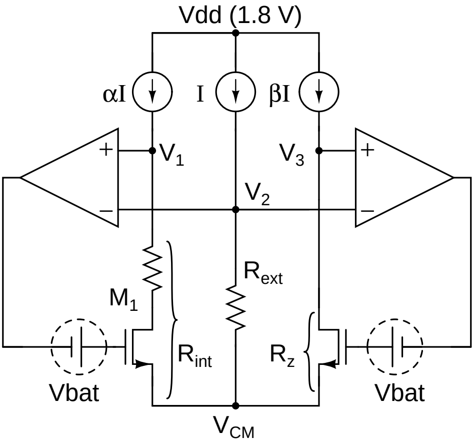


R_i=1666.67 Ω, R_z=145 Ω, C_1=339.76 fF, C_2=919.3 fF, C_3=634.51 fF, C_4=1012.5 fF, C_5=530.05 fF

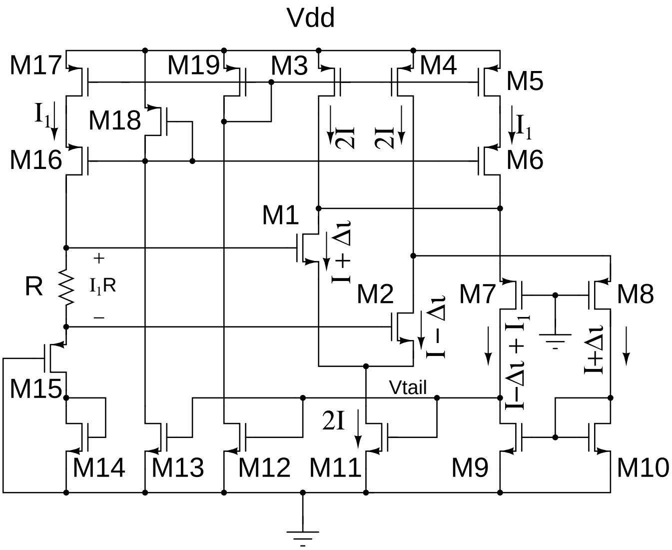
Common-mode Feedback



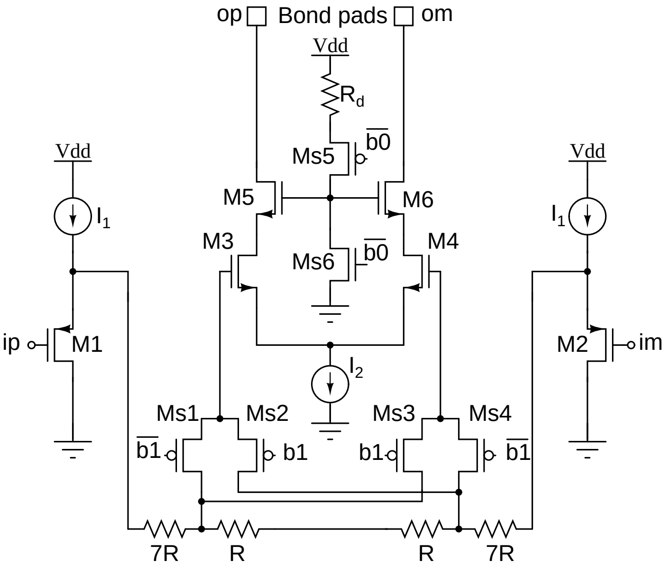
Resistor Servo Loop



Fixed Transconductance Bias

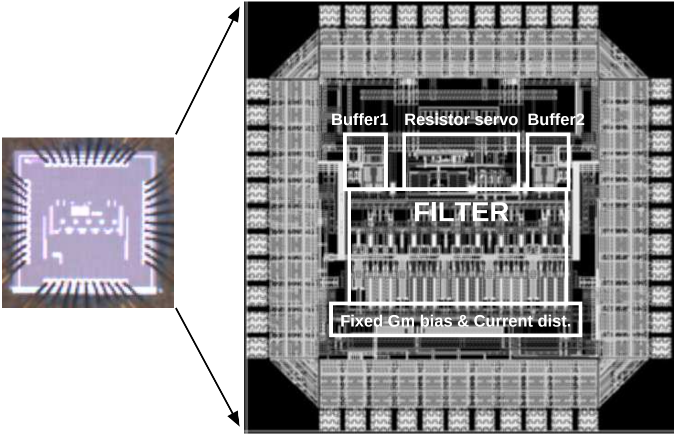


Test Buffer

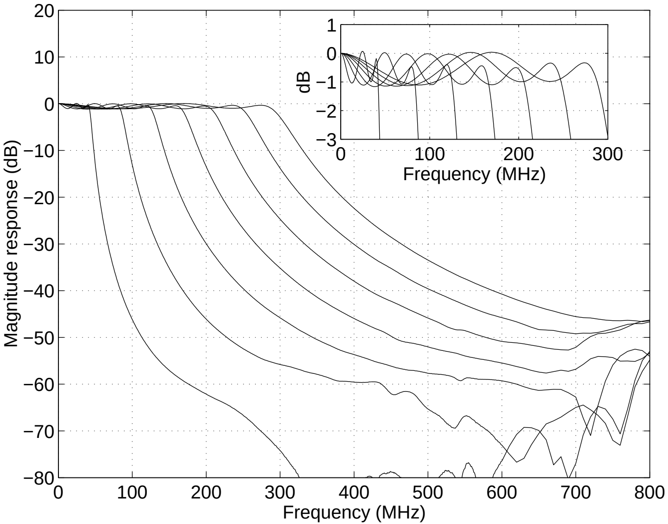


op
Bond pads
om
Vdd
R_d
Ms5
$\overline{b0}$
M5
M6
M3
Ms6
$\overline{b0}$
M4
Vdd
I_1
Vdd
I_1
ip
M1
M2
im
I_2
Ms1
Ms2
Ms3
Ms4
$\overline{b1}$
b1
b1
$\overline{b1}$
7R
R
R
7R

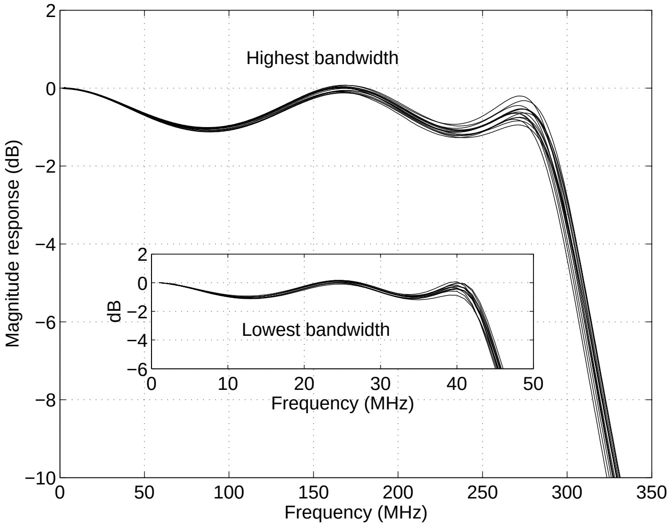
Die Photo & Chip Layout



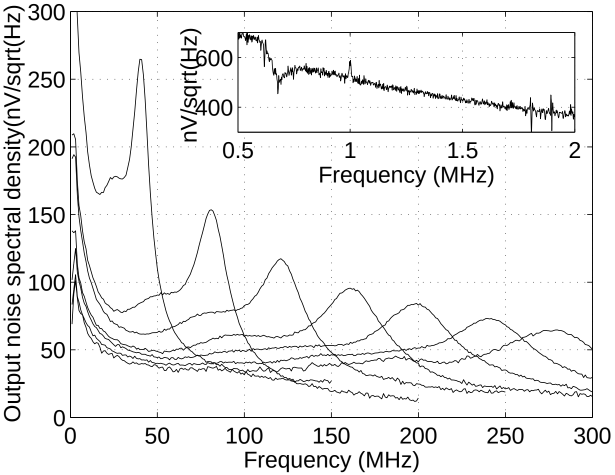
Measured Frequency Response



Response of Ten Chips



Noise Spectral Density with Bandwidth Setting



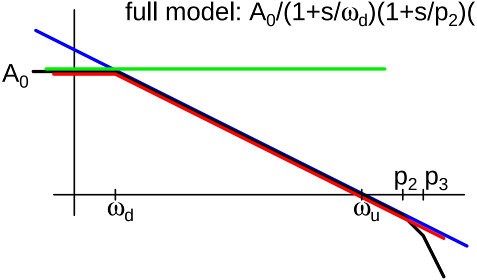
Performance Summary

Table: SUMMARY OF MEASUREMENT RESULTS

Technology	0.18 μm CMOS
Filter type	5^{th} order Chebyshev, Opamp-RC
Supply voltage	1.8 V
3 dB bandwidth	44-300 MHz
Active chip area	0.63 mm^2
Power	54 mW
Integrated output noise	860 μV rms
IIP_3 at band-edge	2.5 V rms
Test tone at $\frac{f_{-1\mathrm{dB}}}{3}$	
$V_{in,pp}$ differential for THD$\leq$-40 dB	2.2 V
Dynamic range for THD$=$-40 dB	56.6 dB

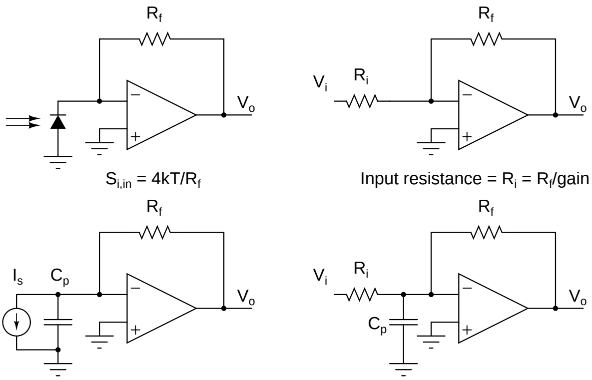
Lead lag compensation

finite dc gain model: A_0
first order model: $A_0/(1+s/\omega_d)$
integrator model: ω_u/s
full model: $A_0/(1+s/\omega_d)(1+s/p_2)(1+s/p_3)$ ...



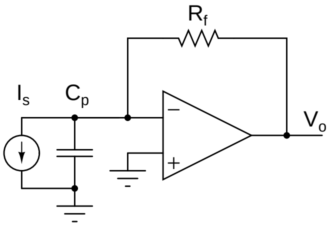
- DC performance: Finite dc gain, constant with frequency
- First order estimate of high frequency effects: Integrator
- More detailed high frequency effects: Integrator+pole (s)
- Simulations: Everything

Negative feedback amplifier design



$$L(s) = A(s)\frac{1}{1 + sC_f R_f} \qquad L(s) = A(s)\frac{R_i}{R_i + R_f}\frac{1}{1 + sC_f(R_f||R_i)}$$

- Extra pole due to the feedback network



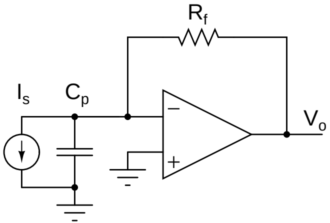
Given R_f and C_d

$$\frac{V_o}{I_s} = \frac{R_f}{s^2\omega_u C_d R_f + s/\omega_u + 1}$$

$$\zeta = \frac{1}{2\sqrt{C_d R_f \omega_u}} = \frac{1}{\sqrt{2}}$$

Set the damping factor to $1/\sqrt{2}$ to obtain a Butterworth response.

Transimpedance amplifier

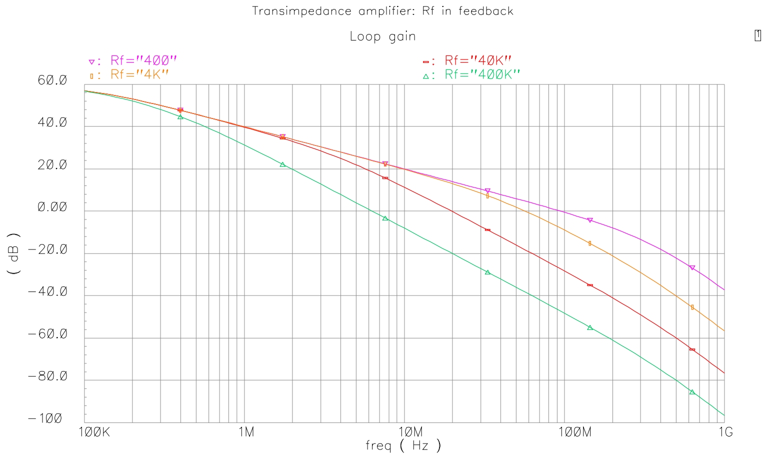


$$\omega_u = \frac{1}{2C_d R_f}$$

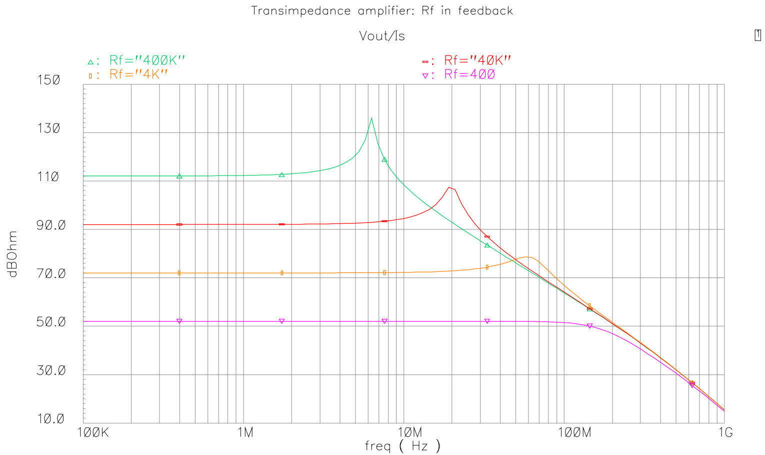
$$\omega_{-3dB} = \frac{1}{2\sqrt{2}\pi C_d R_f}$$

- Bandwidth depends on C_d, R_f, independent of ω_u
- Equivalently, R_f is fixed, given ω_u and C_d; can't be increased

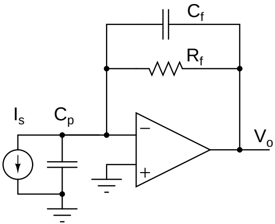
Transimpedance amplifier



Transimpedance amplifier



Transimpedance amplifier-additional zero



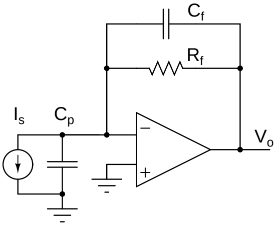
Given R_f and C_d

$$\frac{V_o}{I_s} = \frac{R_f}{s^2 \omega_u C_d R_f + s/\omega_u + sC_f R_f + 1}$$

$$\zeta = \frac{1 + \omega_u C_f R_f}{2\sqrt{\omega_u C_d R_f}}$$

Set the damping factor to $1/\sqrt{2}$ to obtain a Butterworth response.

Transimpedance amplifier-additional zero

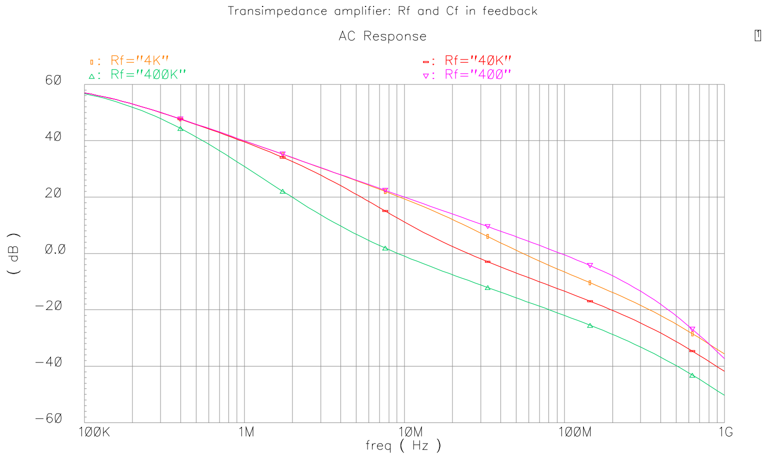


$$C_f = \frac{1}{R_f}\sqrt{2\frac{C_d R_f}{\omega_u} - \frac{1}{\omega_u^2}}$$

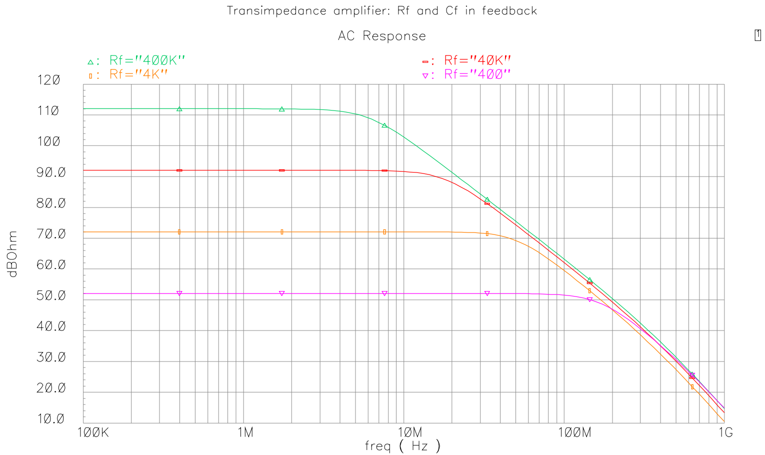
$$\omega_{-3dB} = \frac{1}{2\pi}\sqrt{\frac{\omega_u}{C_d R_f}}\sqrt{\frac{\omega_u C_d R_f}{\omega_u C_d R_f + \sqrt{\omega_u C_d R_f} - 1}} \approx \frac{1}{2\pi}\sqrt{\frac{\omega_u}{C_d R_f}}$$

- C_f can be chosen, given C_d, R_f, and ω_u
- Higher $\omega_u \Rightarrow$ higher bandwidth

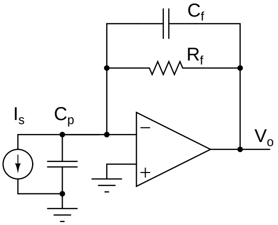
Transimpedance amplifier-additional zero



Transimpedance amplifier-additional zero



Transimpedance amplifier-additional zero



- Zero introduced in the loop gain function
- First order behaviour around unity gain magnitude crossing
- "Lead-lag" compensation
- Minimize virtual ground node parasitics!

References

- H. W. Bode, *Network analysis and feedback amplifier design*, D. Van Nostrand Company, 1945.
- Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw Hill, Aug. 2000.
- K. N. Leung and P. K. Mok, “Analysis of multistage amplifier- frequency compensation,” *IEEE Transactions on Circuits and Systems- I : Fundamental Theory and Applications*, vol. 48, no. 9, pp. 1041-1057, Sep. 2001.
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