A comparison of approaches to carrier generation for Zigbee transceivers

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***Abstract*— Two methods for generating in phase and quadrature local oscillator signals at 2.4 GHz for Zigbee transceivers are investigated. In one method, the output of a 4.8 GHz LC VCO is divided by two to obtain I and Q phases at 2.4 GHz. In another method, outputs of a four stage differential ring VCO at 1.2 GHz are appropriately multiplied to obtain I and Q phases at 2.4 GHz. These circuits are designed and laid out in a 0.18 μm CMOS process and they operate from a 1.8 V power supply. The former architecture occupies 0.052 mm^2, consumes 7.56 mW, and has a phase noise of -117 dBc/Hz at 3.5 MHz. The latter occupies 0.021 mm^2, consumes 9 mW, and has a phase noise of -97 dBc/Hz at 3.5 MHz. Temperature variations of the ring oscillator are minimized using a combination of constant current and constant g_m biasing.**

I. Introduction

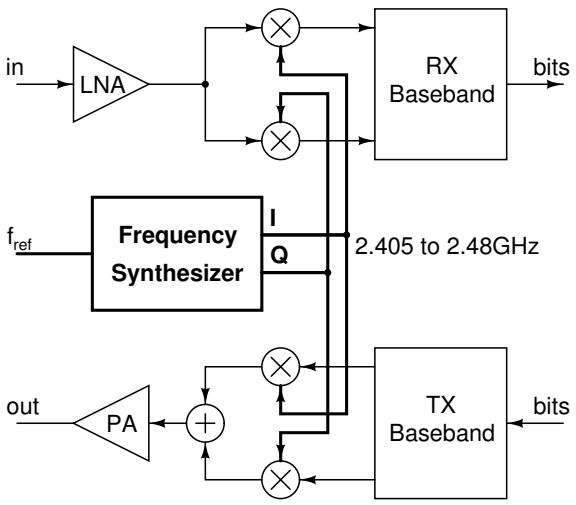

Fig. 1. Zigbee transceiver block diagram

Zigbee (IEEE 802.15.4) standard[1] is intended for low data rate sensor network applications. It specifies 16 channels in the 2.4 GHz band. Fig. 1 shows the block diagram of a possible Zigbee transceiver architecture. The receiver consists of a low noise amplifier followed by downconversion mixers and the baseband circuitry (channel selection filtering and digitization). The transmitter consists of baseband circuitry that does pulse shaping and digital to analog conversion followed by upconversion and power amplification. Both the receiver and the transmitter require a local carrier for frequency conversion. The local carrier will be at the signal frequency in a direct conversion architecture or offset by the intermediate frequency (IF) in a heterodyne architecture. In either case, a frequency synthesizer with in-phase (I) and quadrature (Q) outputs is required. Conventionally, LC oscillators are used in on chip radios due to constraints on phase noise and power dissipation. In this paper, we will investigate the possibility of using a ring oscillator based carrier generator for Zigbee transceivers.

The paper is organized as follows. In section II, we outline the requirements of the local oscillator in a Zigbee transceiver. In section III, we discuss two possible architectures for quadrature carrier generation. Sections IV and V show the design details of these architectures. The design of a frequency synthesizer around these I/Q generators is shown in section VI. In section VII, we compare the two architectures in terms of their performance and chip area.

II. Local oscillator requirements

IEEE 802.15.4 standard specifies 16 channels in the 2.405-2.48 GHz band with a spacing of 5 MHz. The frequency synthesizer (Fig. 1) is required to generate these frequencies offset by the IF. In our case, we have assumed a direct conversion architecture[2] and the frequency synthesizer is designed to generate the channel center frequencies.

To meet the standards, the frequency synthesizer has to have the following requirements: ≤ -92 dBc/Hz phase noise at 3.5 MHz offset and ≤ 200 μs settling time to 40 ppm accuracy. Additionally, it should be able to drive the mixers in the transmitter or the receiver (only one would be operating at any given time). At 3.5 MHz offset, the phase noise of the synthesizer is solely due to the phase noise of the voltage controlled oscillator (VCO). Therefore the VCO must meet this specification. The settling time requirement imposes a lower limit on the bandwidth of the phase locked loop (PLL) used for the frequency synthesizer. The oscillator must drive the mixers and the programmable divider used in the feedback path of the phase locked loop frequency synthesizer.

One of the concerns with a direct conversion architecture is that the transmitted signal can be coupled to the receiver input, and be fed back to the frequency synthesizer through the LNA and mixers, due to finite isolation between different ports of each block (even if the receiver is off). If the oscillator in the frequency synthesizer is at the carrier frequency (2.4 GHz in this case), it will be very sensitive to the modulated transmit signal leaking back into it at the same frequency. This can deteriorate the phase noise of the oscillator significantly. Therefore we have considered only those architectures in which the oscillator is not operating in the transmitted signal band.

III. Architectures for I/Q carrier generation

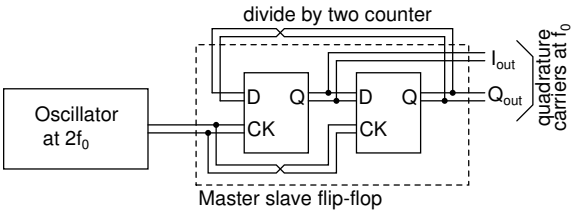

Fig. 2. IQ generation by dividing a double frequency waveform

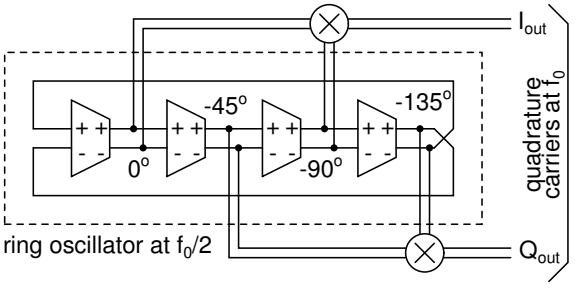

Fig. 3. IQ generation by doubling half frequency waveforms

One of the methods for generating quadrature waveforms is shown in Fig. 2. In this case, an oscillator at twice the desired frequency is used to drive a divide by two counter using a master-slave flip flop. The outputs of the master and the slave latches are separated by half the input period (assuming an input duty cycle of 50%), or equivalently, a quarter of the output period. These can be used as quadrature carriers in the transceiver.

An alternative method for generating quadrature waveforms is shown in Fig. 3. This is based on a four stage differential ring oscillator at half the desired frequency. The waveforms in such an oscillator are 45° apart. Multiplying alternate stage outputs which are separated by 90° results in frequency doubling. From the four waveforms, two such double frequency waveforms can be obtained and they will be 90° apart at the doubled frequency.

When the two schemes are compared, we can observe the following:

- The oscillator in Fig. 2 is at four times the frequency of the oscillator in Fig. 3. This leads to a four times higher power dissipation in the former if ring oscillators are used for both.
- Only one output is required from the oscillator in Fig. 2 whereas Fig. 3 requires a four stage oscillator. Using inductors in each stage of the latter results in a very large chip area.

From the above it appears that an LC oscillator is the only realistic option in Fig. 2 if its power dissipation has to be comparable to that of Fig. 3. Also, a ring oscillator is the only realistic option for the latter if its area of has to be comparable to that of the former. Consequently we can expect to achieve lower phase noise or lower power dissipation with Fig. 2, and a lower area with Fig. 3. However, a definitive comparison can be made only after designing both for a given set of specifications. Since the phase noise specifications for the Zigbee standards are not very stringent[1], the poorer noise performance of Fig. 3 may not be important.

In the rest of the paper, we present the design of quadrature carrier generators using the above schemes and compare the two. The power consumption is minimized while ensuring that the IEEE 802.15.4 requirements are met and that the circuits are capable of driving the load formed by the programmable divider in the feedback path of the frequency synthesizer and the transmit or receive mixers. From the layout of these blocks, the total load on the quadrature outputs was estimated to be 180 fF each.

IV. IQ generation based on dividing a double frequency waveform

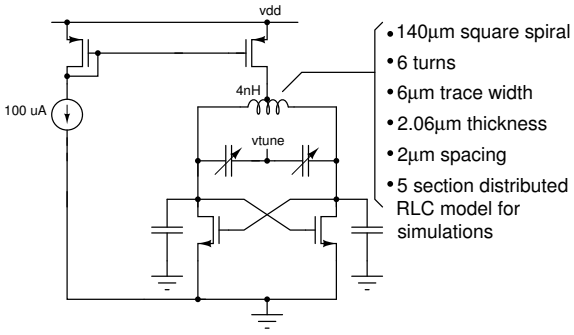

Fig. 4. LC VCO schematic

Fig. 4 shows the schematic of the LC oscillator used in Fig. 2[3]. The negative resistance of the cross coupled nMOS pair cancels the tank circuit's loss to result in sustained oscillations across the LC circuit. The tank circuit is made of a 4 nH differential square spiral inductor, MOS accumulation varactors and some fixed capacitance across the tank. The bias current is adjusted to have a differential swing of 600 mVpp across process and temperature variations. To minimize power consumption, the tank impedance, and hence the inductance must be maximized. But, beyond a certain value of inductance, the required tank capacitance becomes so small that it is dominated by parasitics, and adequate tuning range cannot be obtained. To minimize phase noise with a given tank circuit, the magnitude of the negative conductance must be minimized while ensuring reliable start up. In our design, we have sized the transistors such that, across process and temperature variations, the smallest magnitude of the negative conductance is 1.5 times the equivalent parallel conductance of the tank circuit. The MOS accumulation varactors are laid out in a differential configuration to maximize their quality factor[4].

Fig. 5 shows the schematic of the latch used in the divide by two counter (Fig. 2). The latch uses fully differential current mode logic (CML) with active inductor loads. The active inductors are formed by nMOS load transistors with resistances in series with their gates[5]. The high voltage bias

[1]Compared to cellular phone or wireless LAN standards

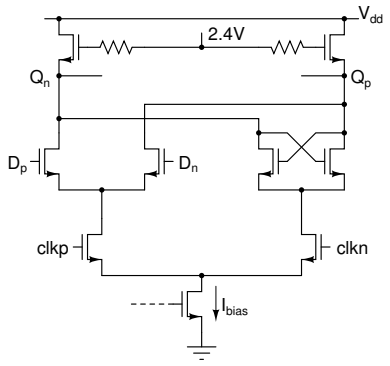

Fig. 5. CML latch used in the divide by two counter

is generated using a charge pump. The resistors are adjusted to obtain sufficiently fast rise times across all process corners. The bias currents are chosen such that the latch can drive the following buffer. Fig. 6 shows the buffer used to drive

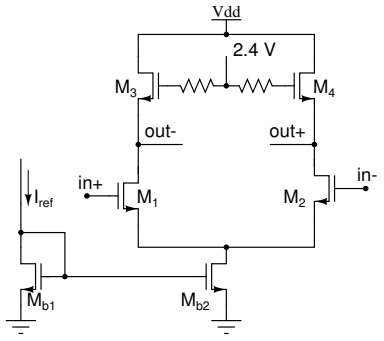

Fig. 6. Buffer to drive the programmable divider and the mixers

the programmable divider and the mixers. It comprises a differential pair with an active inductor load. The bias current is chosen to be sufficient to drive a 180 fF load.

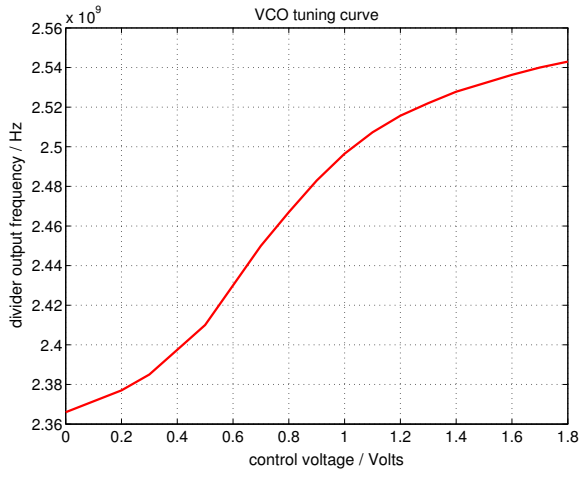

Fig. 7. Frequency (at the divider output) vs. control voltage

Fig. 7 shows the simulated frequency versus control voltage characteristics of the combination of the LC oscillator and the divider. The maximum VCO gain (K_{vco}) is 200 MHz/V. The waveforms at the output of the VCO and

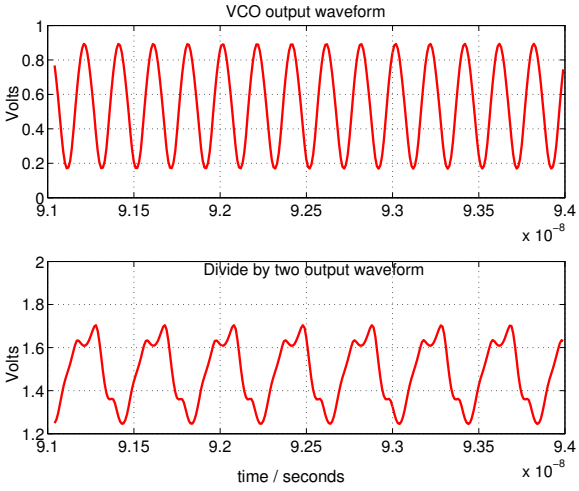

Fig. 8. VCO and divider output waveforms

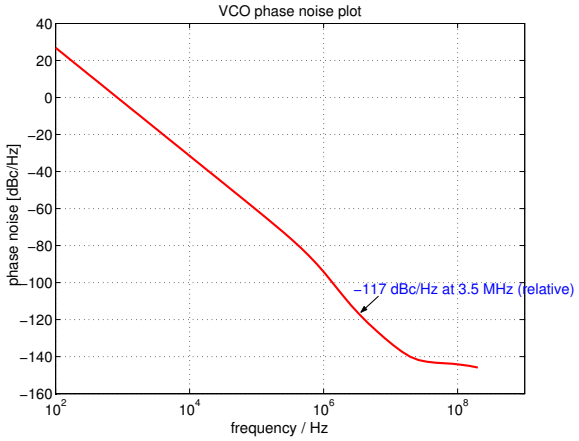

Fig. 9. Phase noise at the divider output

the frequency divider are shown in Fig. 8. Fig. 9 shows the phase noise of the VCO as measured at the divider output[2]. The phase noise is -117 dBc/Hz at 3.5 MHz.

V. IQ Generation Based on Doubling Half Frequency Waveforms

Fig. 10 shows the delay cell used in the architecture in Fig. 3. It consists of a differential pair (M_{3-4}) loaded by pMOS transistors in triode region (M_{1-2}). The oscillation frequency is varied by varying the transconductance of the differential pair through the tail current. The gate bias of the pMOS transistors is adjusted using a replica bias circuit (M_{7-10}) which maintains the drain voltage at 1.3 V. This ensures a constant swing as the VCO is tuned, and also across process and temperature variations. The replica circuit is common to the four stages of the oscillator. The tail current is derived such that the variations of the VCO characteristics across temperature are minimized. This is explained in more detail later. For sustained oscillations in a four stage oscillator, the delay cell needs to have a dc gain of at least $\sqrt{2}$. The

[2]Relative phase noise above 0 dB at very low frequencies is a an artifact of simulation in SpectreRF.

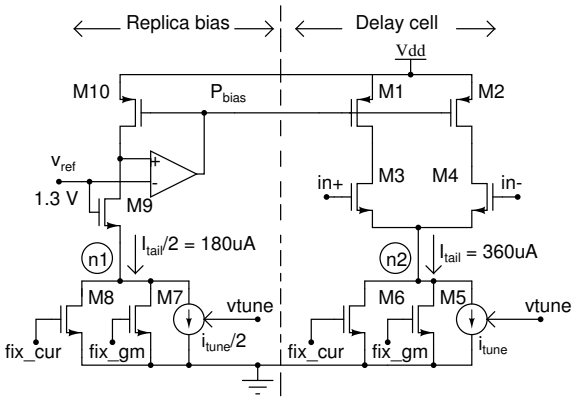

Fig. 10. Schematic of the delay cell with replica bias. "fix_cur" and "fix_gm" are derived from a constant current bias and a constant g_m bias respectively.

transistor sizes are chosen such that the lowest dc gain across process and temperature corners is greater than this limit.

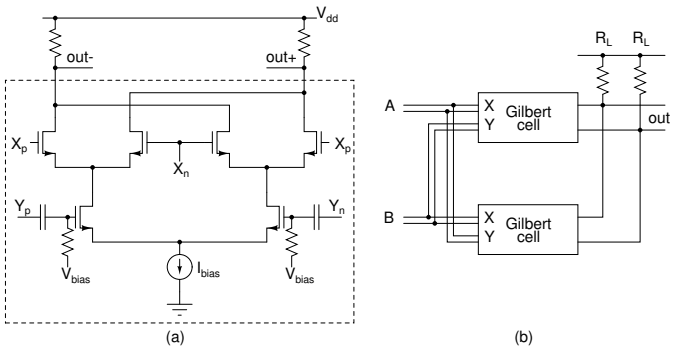

Fig. 11. (a) Gilbert multiplier cell (b) Multiplier with symmetric inputs

The multipliers in Fig. 3 are realized using the well known Gilbert cell (Fig. 11(a)). The disadvantage of this circuit is that the two inputs present different input impedances. If used as is in Fig. 3, the symmetry of the ring oscillator will be destroyed by unequal loading at its nodes. To overcome this problem, two Gilbert cells are used in parallel with each input driving the upper input of one cell and lower input of the other as shown in Fig. 11(b). This results in identical impedances at the two input ports A and B. The lower inputs (Y) are ac coupled and biased at the appropriate common mode level. The multipliers are followed by buffers (Fig. 6) to drive the mixers and the programmable divider.

Fig. 12 shows the frequency variation with temperature of the carrier generator (Fig. 3) using the delay cell in Fig. 10 and the doubler in Fig. 11(b) when the tail current is constant with temperature. A negative temperature coefficient of frequency is observed. Fig. 12 shows the frequency variation with temperature when the tail current is derived from a fixed g_m bias circuit[6]. In this case, as the temperature increases, the bias current is increased to maintain a constant g_m. A positive temperature coefficient is observed. Therefore, a constant current and a current from a fixed g_m bias circuit are added (using M_5 and M_6 in Fig. 10) in the right proportion to cancel the temperature coefficient. The resulting frequency variation with temperature is shown in Fig. 12 and is seen

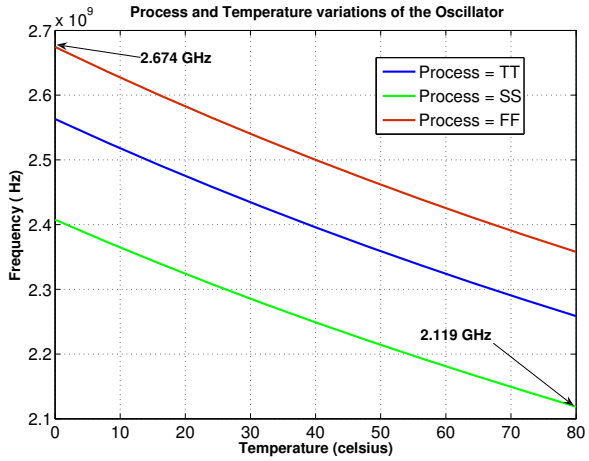

Fig. 12. Process and Temperature variations with fixed current biasing

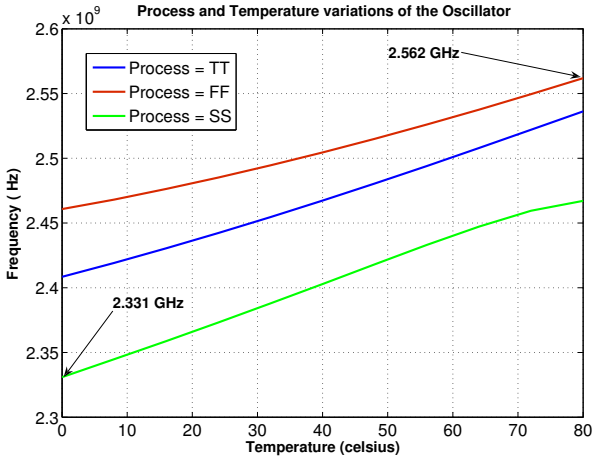

Fig. 13. Process and Temperature variations with fixed g_m biasing

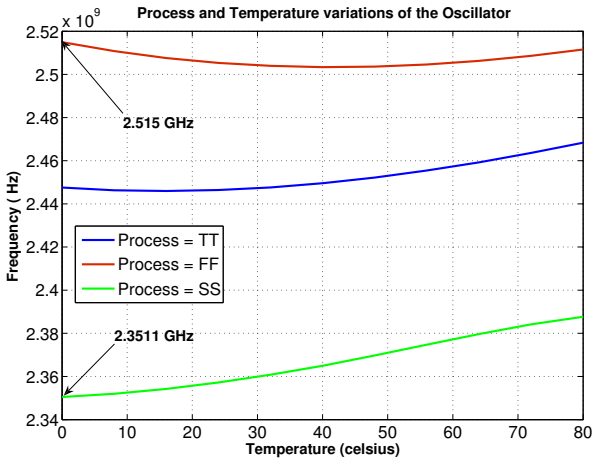

Fig. 14. Process and Temperature variations with mixed biasing

to be significantly smaller than with either constant current or constant g_m biasing. The current consumption of the oscillator increases with "slow" process and high temperatures due to this biasing scheme.

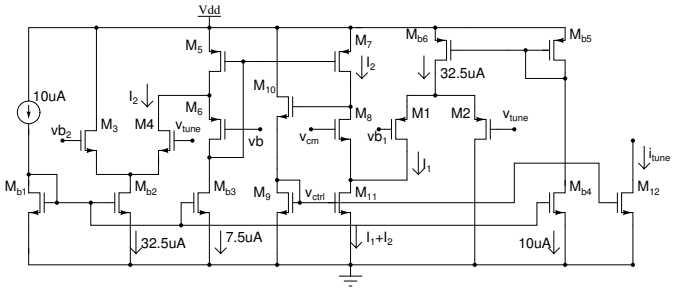

Fig. 15. Voltage to current converter

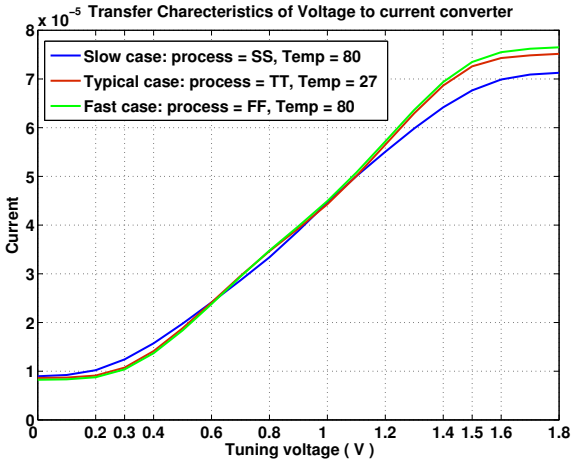

Fig. 16. Transfer characteristics of voltage to current converter

In the ring oscillator above, the frequency is varied using the tail current. In a frequency synthesizer using a charge pump and a passive loop filter, the output is a voltage. To control the ring oscillator using this voltage, a voltage to current converter is used (Fig. 15). To obtain a large range for the control voltage V_{tune}, it is applied to an pMOS differential pair $M_{1,2}$ and a nMOS differential pair $M_{3,4}$ with different reference levels ("vb1" and "vb2"). The currents from the two differential pairs are added to obtain the control current for the ring oscillator. For small values of V_{tune} only M_1 and M_2 are active and for large values of V_{tune}, only M_3 and M_4 are active. The characteristics of the V-I converter are shown in Fig. 16. The usable range of V_{tune} is from 0.3 V to 1.5 V.

Fig. 17 shows the frequency vs. voltage characteristics of the VCO with the doubler. The maximum gain is about 220 MHz/V. Fig. 18 shows the phase noise at the doubler output. Fig. 19 shows the output waveforms.

VI. Frequency Synthesizer Design

Fig. 20 shows the frequency synthesizer designed around the quadrature carrier generators described above. It is a standard type II phase locked loop[7] with $I_{cp} = 10\,\mu$A, $R_1 = 80\,\text{k}\Omega$, $C_1 = 220\,$pF, and $C_2 = 7\,$pF.

The frequency divider in feedback can be programmed to obtain division ratios from 481 to 495. The architecture of the programmable divider is shown in Fig. 21[8]. CML latches are used throughout. The signal frequency reduces as one goes down the divider chain and the bias currents are reduced accordingly. The differential output is converted to single ended output before being fed to the phase frequency detector.

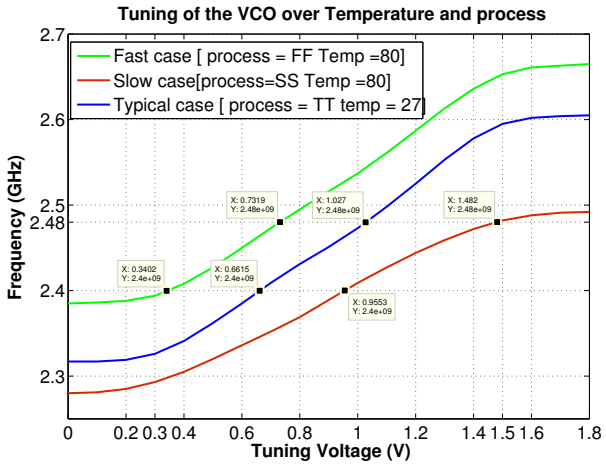

Fig. 17. Frequency vs. voltage at the doubler output

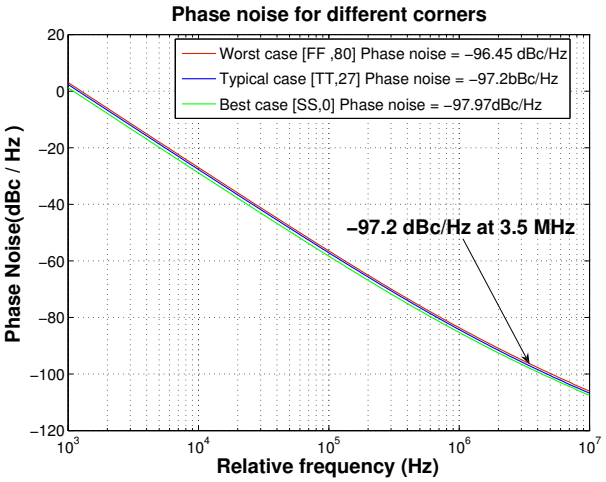

Fig. 18. Phase noise at the doubler output

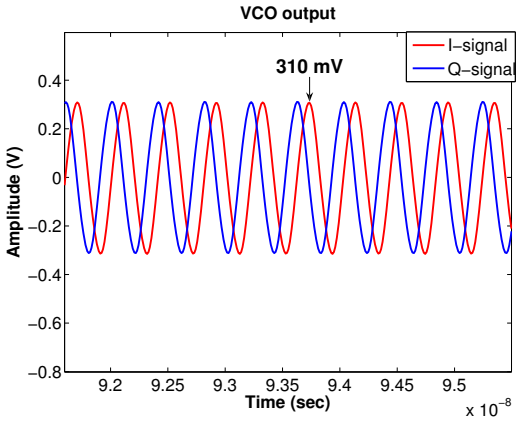

Fig. 19. Quadrature outputs of ring oscillator and doubler combination

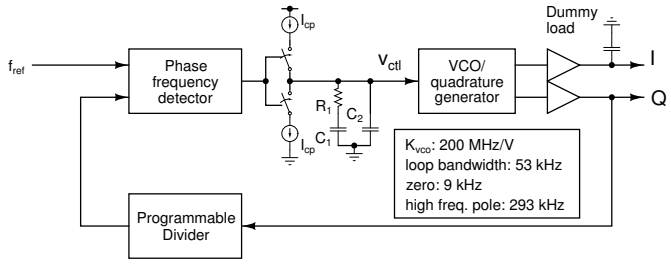

Fig. 20. Frequency synthesizer block diagram

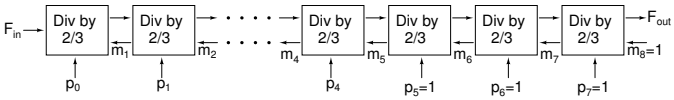

Fig. 21. Programmable frequency divider

VII. Simulation results

Both circuits are designed and laid out in a 0.18 μm CMOS process. Table I shows their salient features. The current consumption of the ring oscillator increases at high temperatures and "slow" processes due to the biasing scheme described earlier. The current consumption of the LC oscillator is independent of process and temperature variations.

The ring oscillator consumes up to 43% higher power than the LC oscillator. The LC oscillator occupies a $2.25\times$ larger area. The phase noise requirements for a Zigbee transceiver can be met with a ring oscillator based architecture. As expected the LC oscillator achieves a much better phase noise.

Table II shows the simulated results of the frequency synthesizer built around the carrier generators described earlier. Since K_{vco} is the same in the two cases, the performance is the same with either architecture.

VIII. Comparison and conclusions

We have presented two approaches to IQ carrier generation for IEEE 802.15.4 Zigbee transceivers. We have designed circuits following both approaches in a 0.18 μm CMOS process and compared them. The comparison is made based on optimizing each design for low power while meeting the requirements of the standard and the load conditions expected in a transceiver. We conclude that it is possible to build a ring oscillator based frequency synthesizer for this standard with a small power penalty and a large area advantage over the LC based approach. Although the phase noise of the LC oscillator is much lower than necessary, the quality factor of the spiral inductor cannot be lowered (while retaining the inductance value) in an attempt to reduce its area, because, doing so reduces the equivalent parallel resistance of the tank circuit and reduces the amplitude of oscillation making it difficult to drive the following stages.

The power consumption of the LC oscillator is constrained by the highest inductance that can be realized while not being overwhelmed by parasitic capacitances. The power consumption of the ring oscillator is limited by the phase noise requirements. Technology scaling does not offer either oscillator significant advantages in terms of power consumption (for the same phase noise specifications). A small reduction in power consumption can be seen due to reduction of parasitic capacitances. The power consumption of the remaining blocks—frequency divider or the multipliers, and the buffers—will be reduced owing to reduction of parasitic capacitances and on chip load capacitances with technology scaling. This reduction will be proportional to the reduction in capacitance and will be the same for either architecture. Therefore we believe that the comparison presented in this paper will remain valid for other CMOS processes.

TABLE I

Performance summary of quadrature generators

	LC osc. + divider (Fig. 2)	Ring osc. + doubler (Fig. 3)
VCO	1 mA	1.44 mA
Bias circuit	—	0.355 mA
V-I converter	—	0.1 mA
Divider	1.8 mA	—
Multipliers	—	0.45 mA each
Buffers	0.7 mA each	0.83 mA each
Total current	**4.2 mA**	**4.455 mA (nom.) 6 mA (max.)**
Phase noise	**-117 dBc/Hz**	**-97 dBc/Hz**
Area	**360 μm x 140 μm**	**160 μm x 140 μm**
K_{vco}	**200 MHz/V**	**220 MHz/V**

TABLE II

Performance summary of the frequency synthesizer

Programmable divider	1.09 mA
Differential to single ended converter	22 μA
Phase frequency detector	23 μA
Charge pump	20 μA
Bias generation circuits	350 μA
Total current	**1.5 mA**
Settling time	**110 μs**
Area	**400 μm x 310 μm**
Reference feedthrough	**-39 dBc (5 MHz) -50 dBc (10 MHz)**

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