A Micropower Log-Domain Filter Using Enhanced Lateral PNPs in a 0.25 μm CMOS Process

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Abstract

A 2^{nd} order low-pass log-domain filter is fabricated in a 0.25 μm CMOS technology using enhanced lateral bipolar transistors. pMOS devices operating in accumulation are used for the integration capacitors. The filter, when tuned to a bandwidth of 22 kHz, consumes 4.1 μW from a 1.5 V supply and has an rms output noise of 0.25 nA. The filter's SNR at 1% THD is 56.1 dB and its maximum $S/(N + THD)$ is 44.9 dB. The chip occupies 0.085 mm^2.

1. Introduction

Log-domain filters [1], which are a form of internally nonlinear circuits that are linear from input to output, have received some attention recently due to their potential for low voltage operation [2]. An exponential nonlinearity is required to implement these filters. They can be realized using bipolar transistors in a bipolar/BiCMOS technology (e.g. [2]) or using MOS transistors operating in weak inversion in a CMOS technology [3, 4].

Another alternative worth exploring for the realization of log-domain filters in CMOS technologies is the use of lateral bipolar transistors. The most common use of lateral transistors in CMOS technologies is in bandgap references. A potential problem with the use of lateral transistors in log-domain filters is their low current gain β. The relatively large base currents can cause significant distortion in a log-domain filter. The enhanced lateral bipolar transistor, originally described in [5] and used in a bandgap reference in [6], is capable of large current gains. This paper describes a log-domain filter using these transistors.

The enhanced lateral bipolar transistor is described briefly in the next section. Sec. 3 presents a second order Butterworth filter using the enhanced lateral PNP transistors. Experimental results are given in Sec. 4.

2. Enhanced lateral bipolar transistors

Fig. 1(a) shows the simplified cross section of a conventional lateral PNP transistor. The "source" and "drain" regions of a pMOS transistor form the collector and emitter and the n-well of the pMOS transistor forms the base. The gate is tied to the most positive voltage in the circuit (commonly done in order to push the carriers below the surface, to avoid imperfections associated with the latter) and has little influence on the operation of the transistor. Fig. 1(b) shows the circuit equivalent of Fig. 1(a). A vertical transistor Q_S whose collector is the (grounded) substrate is inevitably present along with the desired lateral transistor Q_L.

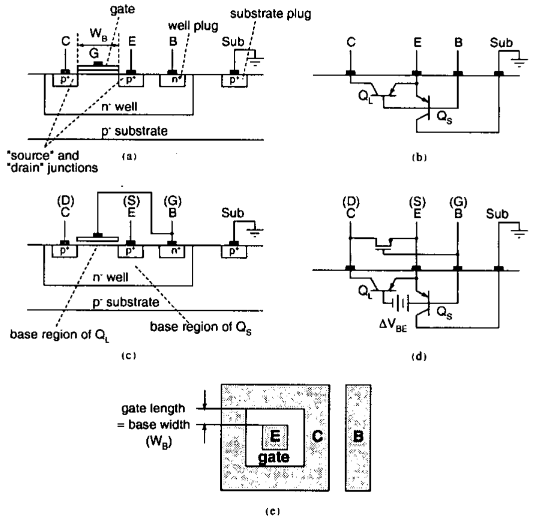

Figure 1. (a) Simplified cross section of a conventional lateral PNP transistor, (b) Electrical equivalent of (a), (c) Simplified cross section of an enhanced lateral PNP transistor, (b) Electrical equivalent of (c), (e) Top view of a practical lateral transistor.

Due to the parallel connection of Q_L and Q_S, only a fraction of the emitter current reaches the collector. This results in a larger bias current (and hence, power consumption) to realize a given transconductance because the collector current of Q_S flows to the substrate and cannot be tapped. Also, the base current of Q_S adds to the base current of Q_L, effectively reducing the current gain β of the lateral transistor.

Fig. 1(c) shows the simplified cross section of the transistor presented in [5]. The gate of the pMOS transistor is connected to the base. In this case, as a negative V_{BE} is applied, the channel tends to invert. The transistor operates as a combination of a subthreshold device and a lateral bipolar device. The result of tying the gate to the base is the realization of a very large dc current gain β, and the suppression of the substrate transistor action to a great extent [5].

A crude explanation for the behavior of this device is as follows [6]. As shown in Fig. 1(c), the base region of the lateral transistor Q_L is near the surface of the device and the base region of the substrate transistor Q_S is deep inside the well underneath the p+ diffusion of the emitter. On applying a negative V_{BE}, an electric field is created underneath the gate of the pMOS transistor. This causes a voltage rise from the surface of the device to the region deep inside the well. This is denoted by ΔV_{BE} in Fig. 1(d). The magnitude of the voltage between the base of Q_L and the emitter is larger than that between the base of Q_S and the emitter by ΔV_{BE}. Comparing Fig. 1(b) to Fig. 1(d), it can be seen that for any given V_{BE}, the contribution of Q_L's collector current to the total collector current is larger in Fig. 1(d). Thus the action of the substrate transistor Q_S is suppressed.

Fig. 1(e) shows the top view of a practical lateral transistor. The emitter is surrounded by the collector to maximize collection efficiency, and hence, the current gain β.

It is reported in [5, 6] that the lateral PNP transistor shown in Fig. 1(c) has a dc current gain in the thousands for small collector currents. These can therefore be used in log-domain filters without the problem of base currents. Compared to an MOS transistor in weak inversion, the bipolar transistor has a larger transconductance for a given current, and therefore, a smaller power consumption to realize a given pole frequency. A disadvantage of lateral bipolar transistors is the large parasitic capacitance from the base (well) to the substrate. But in certain log-domain filter topologies, such as the one given in [2], the base parasitic capacitances do not affect the performance seriously because they appear either across voltage sources or across a desired capacitance. The parasitics at the base do however limit the largest cutoff frequency that can be achieved.

3. Filter design

Fig. 2(a) shows the block diagram of the filter. A second-order Butterworth filter is formed by placing two lossy integrators in a unity gain feedback loop. The transfer function is given by

$$\frac{Y(s)}{U(s)} = \frac{1/2}{1 + (s/\omega_p) + (s/\sqrt{2}\omega_p)^2} \tag{1}$$

where ω_p is the pole of the lossy integrator. The resulting Butterworth filter has a -3 dB bandwidth of $\sqrt{2}\omega_p$.

Fig. 2(b) shows a log-domain lossy integrator [2]. The input current-voltage converter comprising Q_A and M_A logarithmically compresses the input current i_A into a voltage v_A. v_A is fed to a log-domain filter formed by Q_B, C, and I_0. The filtered voltage v_C is fed to a level shifter (Q_C, M_C, and I_0). An exponential voltage-current converter Q_D produces the output current i_D from the level shifted voltage v_D. It can be shown that this log-domain integrator is large-signal linear from the input to the output as long as i_A is positive. The large signal currents i_A and i_D are related in the time domain by

$$\frac{di_D}{dt} = -\frac{I_0}{CV_t} i_D + \frac{I_0}{CV_t} i_A \tag{2}$$

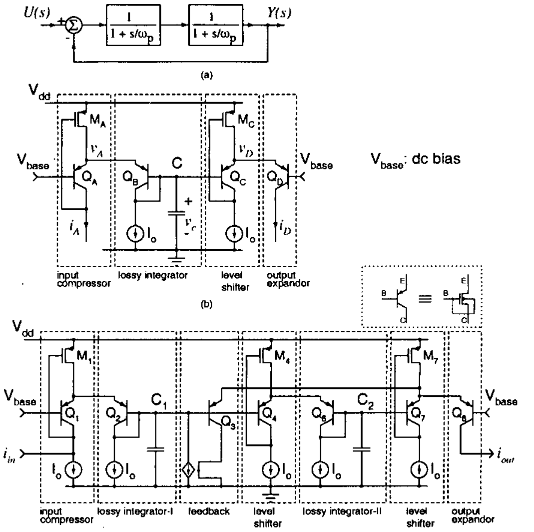

Figure 2. (a) Block diagram of a 2nd-order Butterworth filter, (b) Log-domain lossy integrator, (c) Log-domain 2nd-order Butterworth filter.

where V_t is the thermal voltage. The relation can be expressed in the frequency domain as

$$\frac{I_D(s)}{I_A(s)} = \frac{1}{1 + sCV_t/I_0} \tag{3}$$

Two of these lossy integrators can be combined as shown in Fig. 2(c) to form a Butterworth filter. The input signal i_{in} is added to a bias I_0 and fed to the input transistor Q_1. The PNP transistors (Q_{1-8}) are realized using pMOS transistors whose gates and wells are tied together (Fig. 1, inset in Fig. 2(c)). Owing to the logarithmic compression, the internal voltage swings of a log-domain filter are no larger than a few V_t. Consequently, pMOS accumulation capacitors can be used without introducing additional distortion. C_1 and C_2 in Fig. 2(c) are pMOS accumulation capacitors, each of value 180 pF. The current sources and the current mirror in Fig. 2(c) are realized using cascoded transistors. The supply voltage has to be larger than the sum of the gate-source voltage of the pMOS transistors ($M_{1,4,7}$) and the voltage required to keep the cascode current sources I_0 in the saturation region. With $V_{TP} = 0.9$ V, a 1.5 V supply is sufficient for the operation of this filter.

4. Measured results

Fig. 3 shows the measured I_C vs. V_{EB} variation for transistors of base widths (W_B in Fig. 1) 0.32 μm and 0.36 μm and two values of emitter-collector voltage. The transistor with a narrower base has a higher saturation current and a lower Early voltage (greater separation between the curves for the same change in collector-emitter voltage). Log conformity is good up to a collector current of about 0.5 μA for both transistors. The transistor with the wider base (0.36 μm) was used in

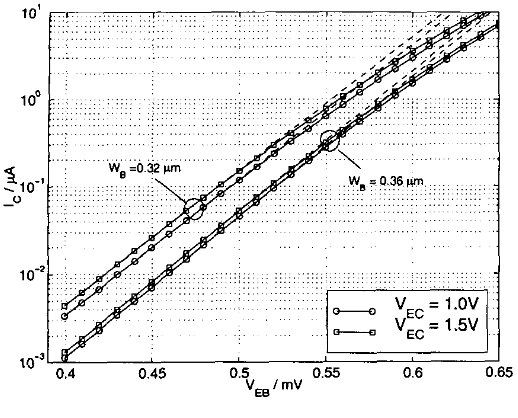

Figure 3. Measured characteristics of the enhanced lateral pnp transistor.

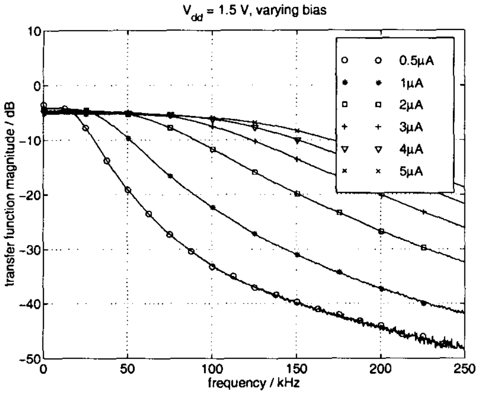

Figure 4. Frequency response of the second-order filter with a supply voltage of 1.5 V for various values of I_0 shown in the insert.

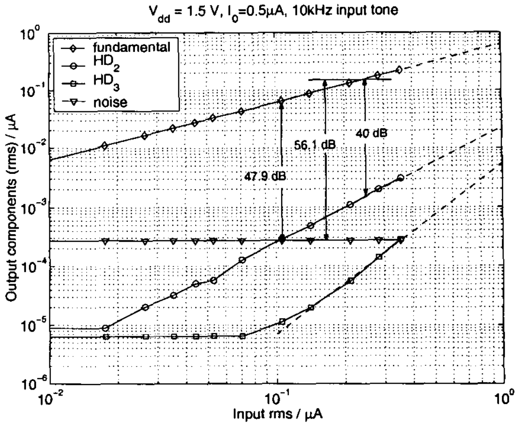

Figure 5. Signal, noise and distortion with $I_0 = 0.5\mu A$.

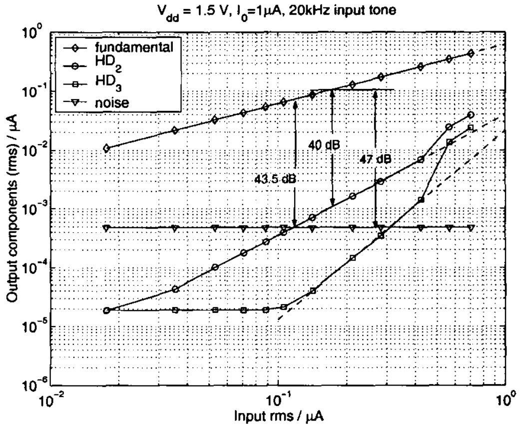

Figure 6. Signal, noise and distortion with $I_0 = 1\mu A$.

the filter described in the previous section. Its measured Early voltage[1] V_A is 2.3 V and the slope factor[2] is 1.04.

Fig. 4 shows the magnitude response of the filter with various bias currents. At larger values of bias currents, the proportionality of bandwidth to the bias current is not seen. This is due to the transistors deviating from the exponential behavior. With $I_0 = 0.5\,\mu$A, the bandwidth is about 22 kHz. The dc gain is more than the expected −6 dB (Eq. (1)) because of the Early effect in the output transistor Q_8 (Fig. 2(c)). The collector of the output transistor is at 0 V due to the measurement setup and its V_{CE} is larger than that of the other transistors in Fig. 2(c) by about 500 mV. Due to the low Early voltage of the transistors, this difference is enough to change the gain by about 1.3 dB.

The output fundamental component, noise and harmonic distortion products when $I_0 = 0.5\,\mu$A are plotted vs. the rms value of the input in Fig. 5. The rms output noise integrated from dc to 50 kHz is 0.25 nA. The distortion at the output of the filter increases with increasing frequency. The 2nd harmonic (HD_2) is much larger than the 3rd harmonic (HD_3) over the usable range of input currents. An input frequency of 10 kHz, which is about half the filter's bandwidth and therefore results in a large 2nd harmonic distortion, is used in the measurements. The maximum value of $S/(N + HD_2)$ is 44.9 dB. When the total harmonic distortion (THD) is 1 % (−40 dB), the filter has a signal to noise ratio (SNR) of 56.1 dB. The filter draws 2.7 μA from a 1.5 V supply.

When I_0 is increased to 1 μA, the filter has a bandwidth of 41 kHz and a current consumption of 5.5 μA. The output signal, noise and distortion products (measured with a 20 kHz input tone) of the filter for $I_0 = 1\,\mu$A are shown in Fig. 6. The output noise (in the 0-100 kHz band) is 0.46 nA. The maximum value of $S/(N + HD_2)$ is 40.5 dB and SNR with 1 % THD is 47 dB. Ideally, a log-domain filter should maintain a constant dynamic-range as it is tuned. The smaller dynamic range with $I_0 = 1\,\mu$A reflects the increased deviation from the exponential characteristic of the lateral bipolar transistor.

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[1] The small signal output conductance of a bipolar transistor is given by $I_c/(V_A + V_{CE})$ in the active region.

[2] The collector current of a bipolar transistor is given by $I_c = I_s \exp(V_{BE}/\eta V_t)$ where η is the slope factor.

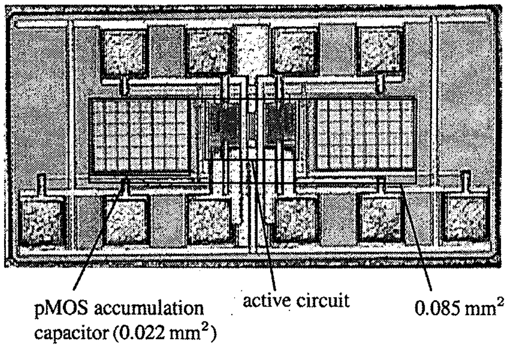

Figure 7. Chip photograph.

Simulations of log-domain filters indicate that the Early effect in bipolar transistors is the dominant cause of distortion. The Early voltage of the lateral transistors is quite small (2.3 V) and can be increased by using a larger base-width (see Fig. 3). This should result in a reduced distortion. It can be seen in Figs. 5 & 6 that THD is dominated by HD_2. Therefore, pseudo-differential operation can be beneficially used to cancel some of the distortion and improve the filter's performance.

Fig. 7 shows the chip photograph. The two pMOS accumulation capacitors occupy $0.022\,mm^2$ each and the entire chip, excluding pads, occupies $0.085\,mm^2$. Table 1 summarizes the performance of the chip.

5. Conclusions

The feasibility of log-domain filters in a standard CMOS process is investigated in this paper. The measured performance of a prototype 2^{nd} order Butterworth filter using enhanced lateral bipolar transistors available in a standard CMOS process is comparable to that of log-domain filters fabricated in bipolar/BiCMOS processes. The results point to the viability of log-domain filters as an alternative for low-frequency filtering in standard CMOS processes.

Table 1. Performance summary

Technology	0.25 μm CMOS	
Chip area	$0.085\,mm^2$ (excl. pads)	
Supply voltage	1.5 V	
Bias current (I_0)	$0.5\mu A$	$1\mu A$
-3 dB BW (kHz)	22	41
Power diss. (μW)	4.1	8.3
o/p noise (rms nA)	0.25	0.46
SNR @ 1 % THD	56.1 dB	47.0 dB
Max. $S/(N + THD)$	44.9 dB	40.5 dB
$\frac{\text{Power dissipation}}{\text{order}\cdot\text{BW}}$	93.2 pJ	101.2 pJ

BW: Bandwidth;

6. Acknowledgments

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