Compensating for Quantizer Delay in Excess of One Clock Cycle in Continuous-Time $\Delta\Sigma$ Modulators

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***Abstract*—The maximum sampling rate of a continuous-time $\Delta\Sigma$ modulator is limited by quantizer delay. Most conventional delay compensation techniques address less than a clock cycle of delay. A technique previously proposed for compensating quantizer delays in excess of a clock cycle in bandpass modulators involves a parallel feedback path that bypasses the quantizer. We analyze this technique for low-pass modulators and show that sampling rates hitherto not possible can be achieved. Design tradeoffs are investigated, and simulation results showing the effectiveness of the technique are given.**

***Index Terms*—Analog-to-digital converter (ADC), compensation, continuous time, delta-sigma, excess loop delay (ELD), oversampling, quantizer, sample and hold (S/H).**

I. Introduction

THE SIGNAL bandwidth that can be achieved in a continuous-time $\Delta\Sigma$ modulator (CTDSM) for a given resolution is limited by the sampling frequency $f_{s,\max}$, which depends on excess loop delay (ELD). The main causes of ELD are the regeneration time of the latch in the flash analog-to-digital converter (ADC) and the delay of the digital logic between the ADC and the feedback digital-to-analog converter (DAC). At higher sampling frequencies, the quantizer delay becomes comparable to the clock period. The $f_{s,\max}$ of several published works ([1]–[3]) was chosen so that the maximum quantizer delay is less than half a clock cycle. This is because most compensation techniques published to date ([3]–[6]) can compensate for a maximum of one clock cycle delay. To make modulators less sensitive to process variations, they are usually compensated for only half a clock cycle of ELD.

A method of compensating more than a clock cycle by using a feedback loop that does not contain the quantizer is given in [7]. In that paper, the authors evaluated the Noise Transfer Function (NTF) and concluded that the in-band quantization noise increases. In this brief, we thoroughly evaluate the technique of placing a local feedback for a low-pass modulator and show that much higher sampling rates can be achieved, leading to a correspondingly higher oversampling ratio (OSR) and a significantly higher resolution. We also show from transistor-level simulations that the sample and hold (S/H), which is used to realize this local feedback can be implemented with a smaller delay than a latch in a multibit quantizer.

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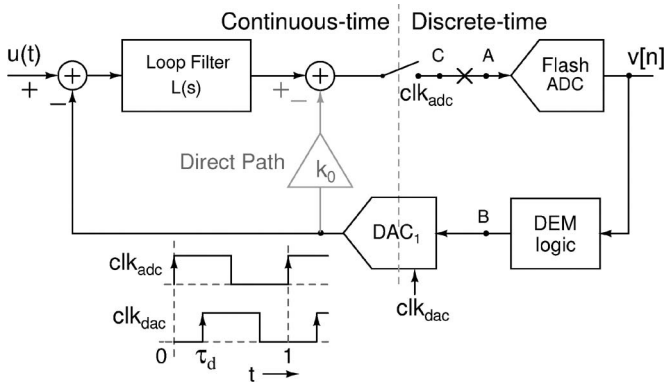

Fig. 1. Block diagram of a Cascaded Integrator with FeedForward summation (CIFF) CTDSM. k_0 is the gain of the direct path required to compensate for ELD.

The rest of this brief is organized as follows: In Section II, we analyze the fundamental limitations of conventional ELD compensation techniques. Section III deals with the analysis of the compensation technique for more than a clock cycle of delay. Section IV demonstrates the superiority of the local feedback S/H ELD compensation technique by comparing its performance with that of conventional methods. Implementation of the idea is shown in Section V. Section VI concludes this brief.

II. Fundamental Limitations of Classical Compensation Techniques

Fig. 1 shows the block diagram of a standard single-loop[1] CTDSM. Here, the logic block includes dynamic element matching (DEM) and the latches used between the flash quantizer and DAC_1. Due to the delay in the flash ADC and the DEM logic, DAC_1 has to be clocked at a time τ_d delayed from the sampling instant of the flash ADC, as shown in Fig. 1. The gain of the direct path (k_0) is zero [8] for a delay-free modulator. A nonreturn-to-zero pulse shape is assumed for DAC_1. Unless otherwise mentioned, the sampling rate is assumed to be 1 Hz. This does not lead to a loss of generality.

Fig. 2 outlines the conventional approach for ELD compensation. k_{1-4} are the gain coefficients of a fourth-order loop filter. The loop is broken, and the discrete-time impulse response of the loop filter from A to C is designed to be the same with ELD [Fig. 2(b)] as that for Fig. 2(a), which is the ideal case ([8], [9]). Therefore, Fig. 2(b) provides the desired

[1] A CIFF architecture is shown here. The proposed technique can also be used for the CIFB architecture.

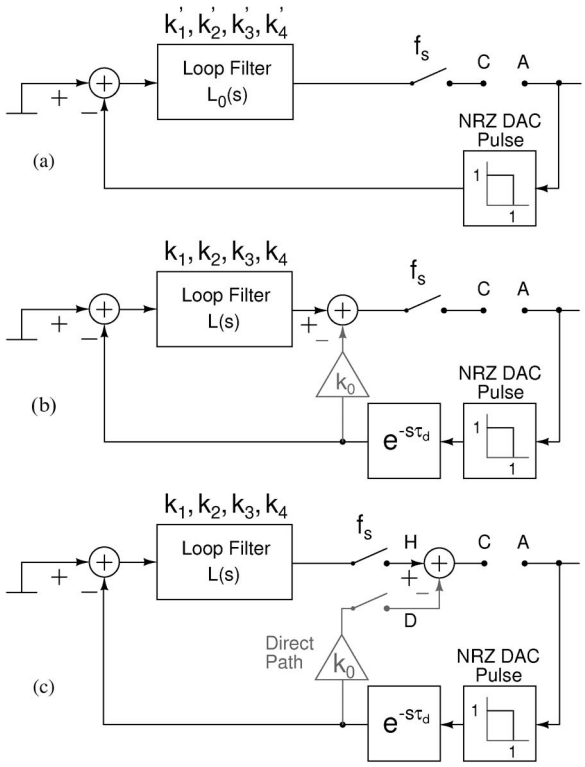

Fig. 2. ΔΣ modulator loop broken at the quantizer. (a) Ideal (no ELD). (b) With ELD, the discrete-time loop filter response from A to C is adjusted to be the same as in the ideal case. (c) Fig. 2(b) modified to show the sampled outputs of the loop filter and the direct path separately.

NTF despite ELD. However, this technique results in a good NTF for a low-pass ΔΣ modulator only for $\tau_d < 1$ [10].

Fig. 2(c) shows the block diagram of Fig. 2(b), with the sampler moved before the summation. Fig. 3 shows the sampled impulse response at the output of the loop filter $L(s)$, the direct path k_0, the resulting NTF impulse response, and the NTF magnitude response for different values of ELD, where a fourth-order modulator with an out-of-band gain (OBG) of 2 and a sampling rate of 1 Hz is used.

The top row of Fig. 3 corresponds to the delay-free case. In this case, the contribution of the direct path is zero to make the ideal sampled impulse response at C in Fig. 2(c). The second row corresponds to half a period delay. The second sample of the output of the loop filter $L(s)$ is reduced, compared with that in the delay-free case. This is compensated by adding an appropriately scaled contribution from the direct path and adjusting coefficients k_{1-4} in the loop filter $L(s)$ to make the sampled impulse response at C in Fig. 2(c) the same as that in the delay-free case [8]. The resulting NTF [Fig. 3.2(c)] is exactly the same as in the ideal case [Fig. 3.1(c)]. As ELD increases, the second sample decreases further, and the k_0 needs to increase.

The third row corresponds to an ELD of one and a half clock cycles. The second sample of the output of the loop filter $L(s)$ is zero. In this case, however, the contribution of the direct path is also zero, and the second sample cannot be restored to its ideal value, regardless of the choice of k_0. Therefore, the second sample of the impulse response at C in Fig. 2(c) is zero. This results in an NTF whose second sample is always zero [Fig. 3.3(c)]. As shown in [10], good NTFs for low-pass modulators cannot be realized with stable minimum-phase transfer functions having a zero-valued second sample in their impulse responses. An example of the magnitude response of a stable NTF optimized for noise suppression at low frequencies, with the second NTF sample being zero, is shown in Fig. 3.3(d). Compared to the ideal case [Fig. 3.1(d)], the quantization noise suppression is worse, and there is greater peaking, indicating that conventional compensation techniques are not effective for ELD exceeding a clock cycle.

A way to obtain a nonzero second sample in the impulse response from A to C in Fig. 2(c) is to have an additional feedback path that does not depend on the quantizer. The delay of this path has to be less than a clock cycle. This is detailed in the next section.

III. Compensation Technique for Delay of More Than One Clock Cycle

Fig. 4 shows the modulator of Fig. 1 with an additional feedback loop around the sampler [7]. A zero-order hold converts the discrete-time signal into a continuous-time signal. In practice, the zero-order hold is realized using a separate S/H circuit [7]. Since the new loop requires only an S/H, its delay is much smaller than that of the quantizer[1] and the digital logic, and can be designed to have a delay of less than a clock cycle from A to C. As before, the loop is broken at the point marked X, and the discrete-time impulse response from A to C is adjusted to be that of the ideal loop filter. Here, the second sample of the original loop filter impulse response from A to C is obtained by adjusting the coefficient a in the fast loop. After getting the second sample accurately from the fast loop, coefficients k_{0-4} are adjusted to match the rest of the samples to their ideal values.

Fig. 5(a) shows the new modulator with additive quantization error e_q. The transfer function before the quantizer consists of the sampled outputs of $L(s)$ and k_0 cascaded with the fast loop, whose transfer function [Fig. 5(b)] is $1/(1+az^{-1})$. The transfer function from the quantization error (e_q) to the output (v) is then calculated as follows:

$$E_q(z) - V(z)\left[L_d(z) + k_0 z^{-2}\right]\frac{1}{1+az^{-1}} = V(z) \tag{1}$$

$$\frac{V(z)}{E_q(z)} = \frac{1+az^{-1}}{1+az^{-1}+k_0z^{-2}+L_d(z)} \tag{2}$$

where $L_d(z)$ corresponds to the sampled output of $L(s)$ when the latter is driven by a pulse of delay $\tau_d (1 < \tau_d < 2)$ mentioned in the previous section, the denominator is adjusted to be the same as that in the ideal NTF. Therefore

$$\text{NTF} = (1+az^{-1})\text{NTF}_{\text{ideal}}(z). \tag{3}$$

[2]High-speed quantizers usually need more than one latching stage to minimize errors due to metastability.

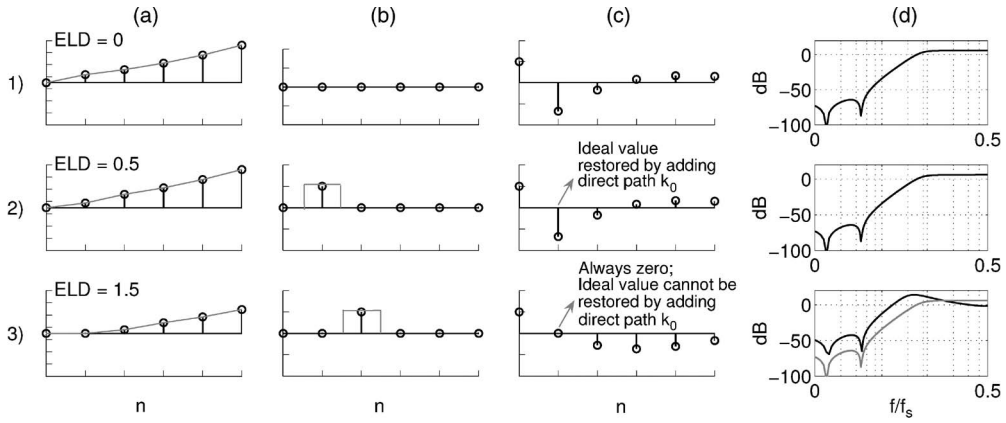

Fig. 3. Limitation of conventional ELD compensation with $\tau_d > 1$. Each row shows the discrete-time equivalent impulse response of the loop filter $L(s)$, the direct path k_0 (with the continuous-time waveforms in gray), and the NTF impulse response that results from the combination. For ELD > 1, the second sample of the NTF is always zero and results in a poor NTF. The sampling rate is 1 Hz. For clarity, columns (a)–(c) are shown to different scales.

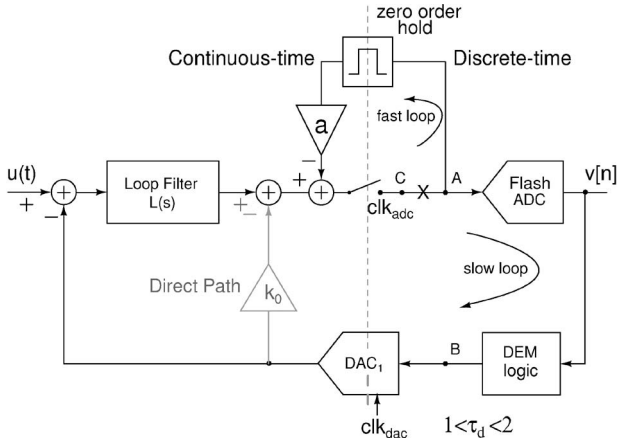

Fig. 4. Block diagram of a $\Delta\Sigma$ ADC with ELD compensation obtained by bypassing the flash ADC using an S/H.

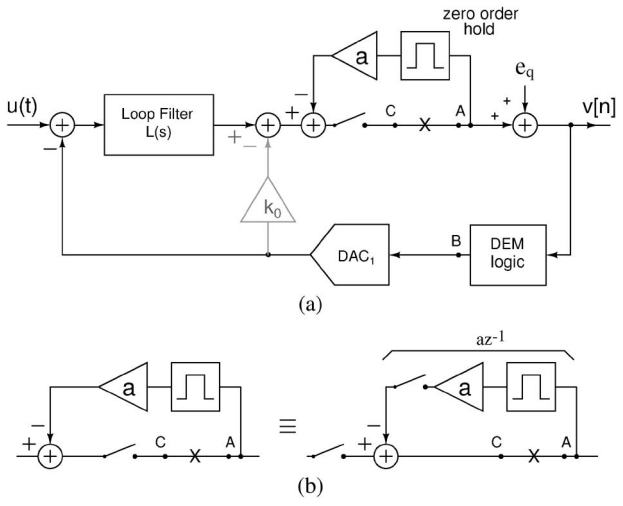

Fig. 5. (a) $\Delta\Sigma$ modulator with additive quantization noise e_q and (b) calculating the transfer function of the fast loop.

An additional zero appears in the NTF, reducing the in-band signal-to-quantization-noise ratio (SQNR) to some extent. These effects are studied in the next section, where a fourth-order NTF is used for illustration.

TABLE I
COEFFICIENTS OF A FOURTH-ORDER BUTTERWORTH NTF WITH OBG = 2 AND OPTIMIZED ZEROS. (OSR = 25)

b_0	b_1	b_2	b_3	b_4	ω_1	ω_2
1	-2.634	2.757	-1.332	0.248	0.0447	0.109

ELD	k_0	k_1	k_2	k_3	k_4	a	NTF
0	0	1.017	0.568	0.209	0.033	N/A	$\text{NTF}_{\text{ideal}}(z)$
0.5	0.588	1.343	0.705	0.225	0.031	N/A	$\text{NTF}_{\text{ideal}}(z)$
1.5	0.966	2.164	0.943	0.255	0.028	1.352	$(1+az^{-1})\text{NTF}_{\text{ideal}}(z)$

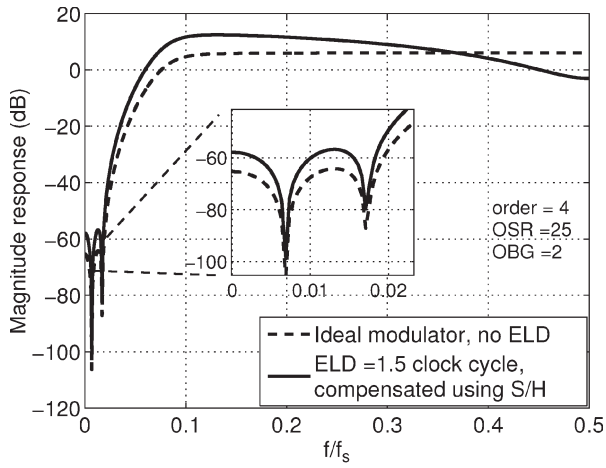

Fig. 6. $|NTF|$ showing the effect of $(1 + az^{-1})$ in the analyzed modulator.

IV. PERFORMANCE OF THE COMPENSATION TECHNIQUE OF MORE THAN ONE CLOCK CYCLE

The NTF of a conventional fourth-order $\Delta\Sigma$ modulator with optimized zeros is of the form

$$\text{NTF}_{\text{ideal}} = \frac{(1-2\cos\omega_1 z^{-1}+z^{-2})(1-2\cos\omega_2 z^{-1}+z^{-2})}{\sum_{m=0}^{4} b_m z^{-m}}.$$

As shown in the previous section, the NTF of the modulator with the new compensation technique is of the form NTF $=$

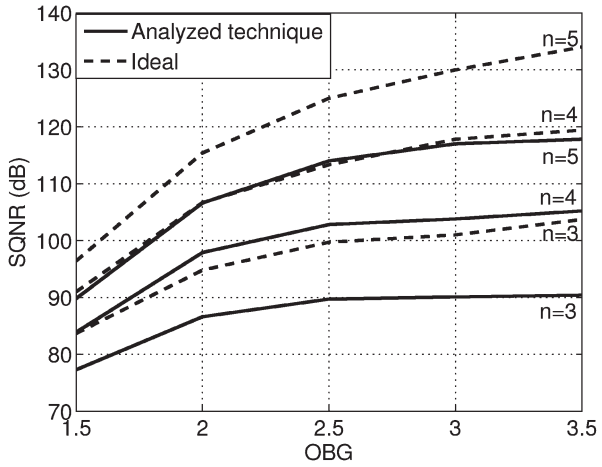

Fig. 7. Peak SQNR versus OBG for various orders. An ELD $= 1.5$ is compensated using the proposed technique. A 4-bit quantizer is assumed (OSR $= 25$).

$(1 + az^{-1})\text{NTF}_{\text{ideal}}$. Here, the ideal NTF is modified[3] due to the zero at $z = -a$.

Table I shows the values of b_m, optimized zeros ω_{1-2}, continuous-time loop filter coefficients k_{0-4}, and fast loop coefficient a for ELD $= 0$, ELD $= 0.5$ (conventionally compensated), and ELD $= 1.5$ (compensated using an S/H).

Fig. 6 shows the NTF magnitudes of the ideal and analyzed modulator structures. There is an increase of 7.5 in the in-band quantization noise *for a given OSR*. The maximum stable amplitude (normalized to the quantizer range) with a 4-bit quantizer is 0.87 for the conventional case and 0.75 for the modulator with an S/H. However, an ELD $= 1.5$ represents a $3\times$ increase in sampling rate for a given quantizer in a given process technology, compared with the conventional case (where the ELD is usually limited to 0.5). The resulting increase in OSR for a given signal bandwidth results in a much higher SQNR.

Fig. 7 shows the effect of the zero at $z = -a$ on the performance of the $\Delta\Sigma$ modulator. As the OBG increases, it is seen that the difference in the peak SQNR of an ideal modulator and one compensated using the S/H increases. However, the performance is better than that of a third-order modulator. Similarly, the fifth-order compensated modulator approaches the behavior of an ideal fourth-order modulator. Thus, the compensation technique demands an increase in order by one to get the same peak SQNR as from the ideal modulator for a given OSR.

Fig. 8 shows that, for the same sampling frequency (f_s), a higher SQNR is obtained from a conventionally compensated modulator, compared with the modulator with an S/H. Since $f_{s,\max}$ is limited by ELD $= 2$ in the proposed technique, the sampling rate of the CTDSM can be increased by a factor of 2. In practice, as the ELD increases, the coefficient k_0 increases. This reduces the feedback fraction around the final opamp, consequently increasing its gain bandwidth requirements. These considerations usually limit the ELD that can be compensated without an additional loop to 0.5. Similarly, in this technique,

[3]In this case, $\int_0^{\pi} \log|\text{NTF}(e^{j\omega})|d\omega \neq 0$, because the zero at $z = -a$ is outside the unit circle.

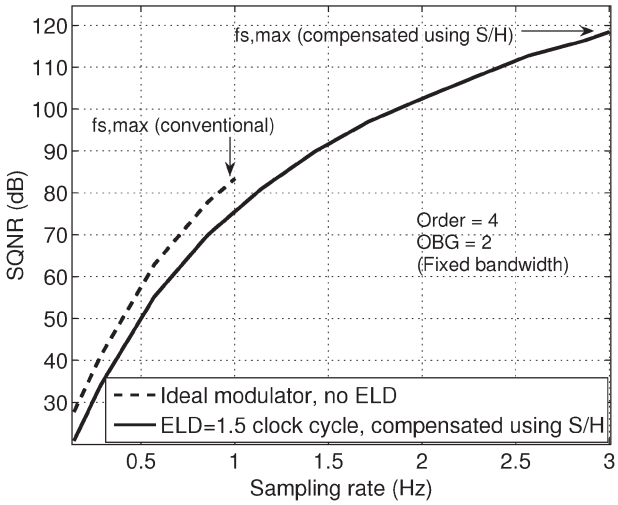

Fig. 8. Variation of SQNR with sampling frequency (f_s). f_s is normalized to the $f_{s,\max}$ of the conventionally compensated modulator. The signal bandwidth is 1/50.

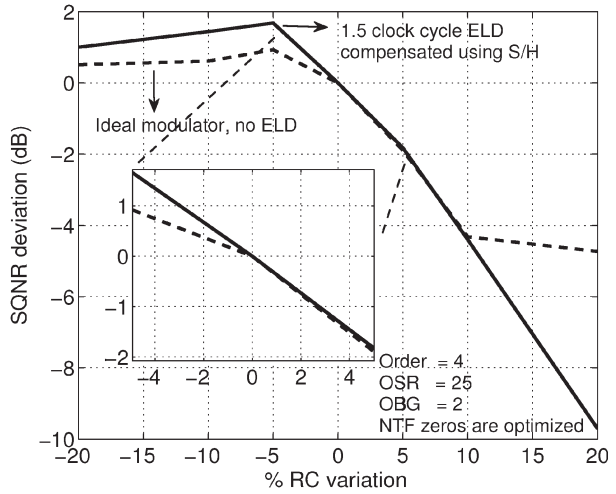

Fig. 9. Peak SQNR deviation from its ideal value versus time constant variations of the loop filter.

it will be limited to 1.5. Thus, the increase in sampling rate is seen to be more than a factor of 2. Hence, as shown in Fig. 8, higher SQNR (or bandwidth) can be obtained with the modulator having a fast loop.

From the simulation results shown in Fig. 9, it is seen that the sensitivity of the conventional and analyzed architecture is virtually the same for $\pm 5\%$ variation in filter time constants. The sensitivity of the NTF magnitude response with respect to the coefficient a of the S/H is shown in Fig. 10. The in-band SNR changes by ± 0.5 dB for a $\pm 10\%$ variation in the coefficient a, attesting to the robustness of the technique.

V. Implementation Details

The fast feedback loop can be realized using an S/H driving a g_m cell around the summing amplifier [Fig. 11(a)] or an S/H driving a capacitor around the last integrator [Fig. 11(b)]. In Fig. 11(a), resistors R_{1-4} are chosen to get the coefficients k_{1-4} [5]. Here, V_{1-4} are the outputs of each integrator. In Fig. 11(b),

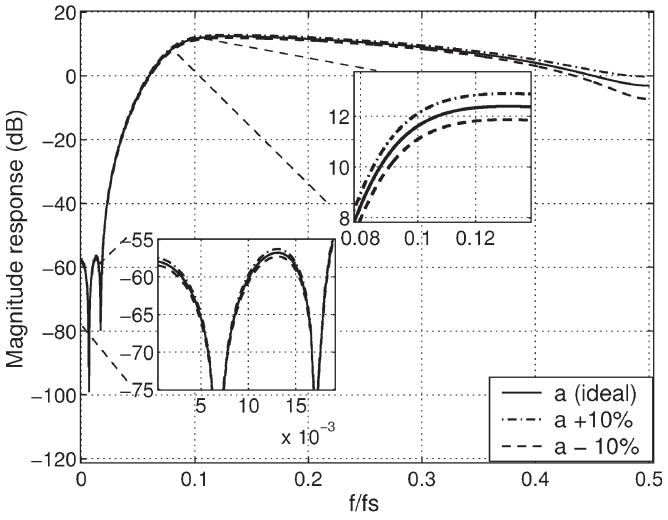

Fig. 10. Magnitude response of NTF for different values of gain coefficient a.

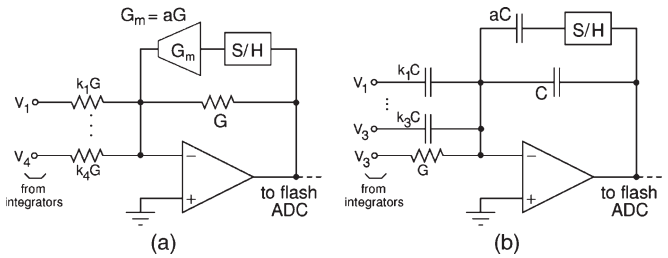

Fig. 11. Implementation of the fast loop with (a) a loop filter with a separate summing amplifier and (b) a loop filter with the last integrator used for summation.

capacitors C_{1-3} are chosen to get the coefficients k_{1-3}, and k_4 is the gain of the last integrator. k_0 can be realized using any of a number of published techniques [3]–[6].

A fourth-order modulator having a four-bit quantizer and a sampling rate of 800 MHz was implemented in a 0.18-μm CMOS process. It was compensated for 1.5 clock cycles of ELD using the fast loop [implemented using Fig. 11(a)]. Fig. 12 shows the eye diagram at the output of the S/H and the quantizer. As can be seen, the delay from the fast loop (0.3 ns) is much smaller than that from the quantizer loop (1 ns).

VI. Conclusion

We have analyzed a technique previously proposed in [7] for compensating high ELD in bandpass $\Delta\Sigma$ modulators for its performance in low-pass $\Delta\Sigma$ modulators. With this technique, ELD of more than one clock cycle can be compensated with a small loss in resolution. Since the ELD due to the quantizer limits the sampling rate in a given process, this technique enables significantly higher sampling rates. This can be used to achieve much higher resolutions by increasing the OSR or to achieve higher signal bandwidths. Transistor-level simulations in a 0.18-μm CMOS process indicate that a sampling frequency of 800 MHz is possible, compared with previously reported highs of about 300 MHz (e.g., [2]).

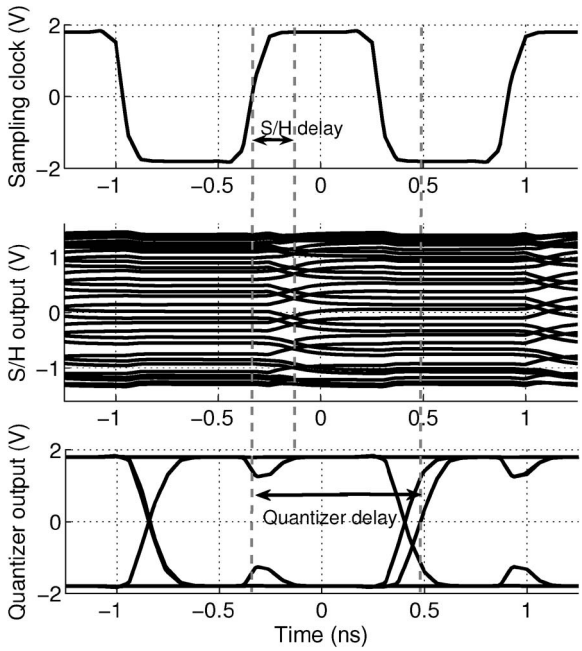

Fig. 12. Eye diagram of the S/H and the quantizer output. Time period = 1.25 ns.

Since the technique presented here can tolerate quantizer delays of more than a clock cycle, it enables the use of multistep ADCs, such as subranging or pipelined A/D converters, in $\Delta\Sigma$ loops. This can reduce the complexity and the power dissipation in the quantizer and its clock drivers.

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