

Micropower Low-Voltage Analog Filter in a Digital CMOS Process

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Abstract—Techniques for implementing micropower analog filters using digital CMOS process technology are described. PMOS devices operating in accumulation are used for the integration capacitors, and the voltage swing across them is limited by employing current-mode operation using the log domain approach. The latter is implemented using enhanced lateral bipolar transistors. A second-order low-pass filter with a cutoff frequency of 22 kHz, fabricated in a 0.25- μm digital CMOS technology, consumes 4.1 μW from a 1.5-V supply and has an rms output noise of 0.25 nA. The filter's signal-to-noise ratio at 1% total harmonic distortion (THD) is 56 dB and its maximum $S/(N + \text{THD})$ is 45 dB. The chip occupies 0.085 mm^2 .

Index Terms—Continuous-time filter, lateral bipolar, log domain, micropower.

I. INTRODUCTION

THE implementation of analog filters in digital CMOS processes is made difficult because of the lack of availability of high-density linear capacitors. Although this problem can be addressed using MOS transistors as capacitors (e.g., [1]), the voltage swing on such capacitors must be kept small in order not to exercise their nonlinearity to a significant extent. The restriction on the voltage swing means that a low supply voltage must be used for power efficient operation. Traditional topologies which operate with a large supply voltage and large internal swings, when used with MOS capacitors, will be forced to reduce their signal swings, but may not tolerate a proportionate reduction of the supply voltage due to biasing constraints. This results in a reduced power efficiency. Filters which have an inherently low internal voltage swing and operate with a low supply voltage are well suited for realization in digital CMOS processes with accumulation capacitors. Log-domain filters [2], which are a form of internally nonlinear circuits that are linear from input to output, have received some attention recently due to their potential for low-voltage operation [3]. An exponential nonlinearity is required to implement these filters, and is best implemented using bipolar transistors in bipolar or BiCMOS technologies (e.g., [3]). In CMOS technology, log-domain filters using MOS transistors operating in weak inversion have been reported [4], [5]. In this brief, we explore instead the use of enhanced lateral bipolar transistors, which are available in CMOS technology. The enhanced lateral bipolar transistor is described briefly in the next section. Section III presents a second-order

Butterworth filter using the enhanced lateral p-n-p transistors. Experimental results are given in Section IV.

II. ENHANCED LATERAL BIPOLAR TRANSISTORS

Fig. 1(a) shows the simplified cross section of a conventional lateral p-n-p transistor. The source and drain regions of a pMOS transistor form the collector and emitter and the n-well of the pMOS transistor forms the base. The gate is tied to the most positive voltage in the circuit (commonly done in order to push the carriers below the surface, thus avoiding imperfections associated with the latter) and has little influence on the operation of the transistor. The most common use of lateral bipolar transistors in CMOS technologies is in bandgap references. However, a problem with the use of such transistors in log-domain filters is their low current gain β . The relatively large base currents can cause significant distortion in such filters. Additionally, a part of the emitter current is shunted to the substrate through the parasitic vertical transistor, resulting in unnecessary current consumption.

The enhanced lateral bipolar transistor, originally described in [6] and used in a bandgap reference in [7], is capable of large current gains. Fig. 1(b) shows the simplified cross section of the transistor presented in [6]. The gate of the pMOS transistor is connected to the base. The transistor operates as a combination of a subthreshold device and a lateral bipolar device; the reader is referred to the literature for a description of the operation of this transistor [6], [7]. The result of tying the gate to the base is the suppression of parasitic substrate transistor action to a great extent, and the realization of a very large dc current gain β [6], and the elimination of the shunting of a part of the emitter current into the substrate. Fig. 1(c) shows the top view of a practical enhanced lateral transistor. The emitter is surrounded by the collector to maximize collection efficiency, and hence, the current gain β .

It is reported in [6] and [7] that the lateral p-n-p transistor shown in Fig. 1 has a dc current gain in the thousands for small collector currents. Such transistors can, therefore, be used in log-domain filters without the problem of base currents. Compared with an MOS transistor in weak inversion, the bipolar transistor has a larger transconductance for a given current and, therefore, a smaller power consumption to realize a given pole frequency.

III. FILTER DESIGN

Fig. 2(a) shows the block diagram of a filter designed to test the aforementioned approach. A second-order Butterworth filter

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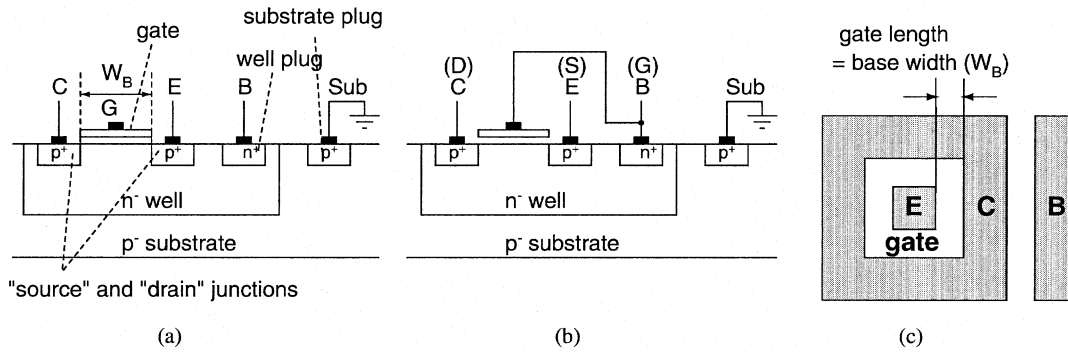


Fig. 1. (a) Simplified cross section of a conventional lateral p-n-p transistor. (b) Simplified cross section of an enhanced lateral p-n-p transistor. (c) Top view of a practical lateral transistor.

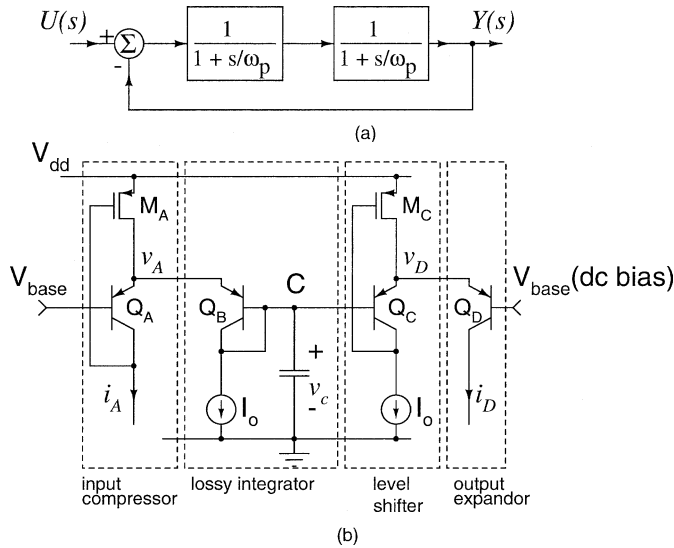


Fig. 2. (a) Block diagram of a second-order Butterworth filter. (b) Log-domain lossy integrator.

is formed by placing two lossy integrators in a unity gain feedback loop. The transfer function is given by

$$\frac{Y(s)}{U(s)} = \frac{1/2}{1 + (s/\omega_p) + (s/\sqrt{2}\omega_p)^2} \quad (1)$$

where ω_p is the pole of the lossy integrator. The resulting Butterworth filter has a -3 -dB bandwidth of $\sqrt{2}\omega_p$.

Fig. 2(b) shows a log-domain lossy integrator [3]. The input current-voltage converter comprising Q_A and M_A logarithmically compresses the input current i_A into a voltage v_A . v_A is fed to a log-domain filter formed by Q_B , C , and I_0 . The filtered voltage v_C is fed to a level shifter (Q_C , M_C , and I_0). An exponential voltage-current converter Q_D produces the output current i_D from the level shifted voltage v_D . It can be shown that this log-domain integrator is large-signal linear from the input to the output as long as i_A is positive. The time and frequency domain relationships between the large signal currents i_A and i_D are

$$\frac{di_D}{dt} = -\frac{I_0}{CV_t} i_D + \frac{I_0}{CV_t} i_A, \quad \frac{I_D(s)}{I_A(s)} = \frac{1}{1 + sCV_t/I_0} \quad (2)$$

where V_t is the thermal voltage.

A disadvantage of lateral bipolar transistors is the large parasitic capacitance from the base (well) to the substrate. But in the topology of Fig. 2, the base parasitic capacitance does not affect the performance seriously because it appears across the desired integrator capacitance. However, this parasitic limits the largest frequency of operation that can be achieved.

Two of the earlier lossy integrators can be combined as shown in Fig. 3 to form a Butterworth filter. The input signal i_{in} is added to a bias I_0 and fed to the input transistor Q_1 . The p-n-p transistors (Q_{1-8}) are realized using pMOS transistors whose gates and wells are tied together (Fig. 1, inset in Fig. 3). Owing to the logarithmic compression, the internal voltage swings of a log-domain filter are no larger than a few V_t . Consequently, pMOS accumulation capacitors can be used without introducing additional distortion. C_1 and C_2 in Fig. 3 are pMOS accumulation capacitors, each of value 180 pF. The supply voltage has to be larger than the sum of the gate-source voltage of the pMOS transistors ($M_{1,4,7}$) and the voltage required to keep the cascode current sources I_0 in the saturation region. With $V_{TP} = 0.9$ V, a 1.5-V supply is sufficient for the operation of this filter.

The main parasitic effect in the frequency response is introduced by the extra pole in the current mirror in the feedback path (Fig. 3). The result is a third-order filter with a high-frequency zero instead of the intended second-order filter. Its effect is to reduce the bandwidth, enhance the quality factor, and to increase the stopband attenuation in the frequency range between the bandwidth of the filter and the parasitic pole.

IV. MEASURED RESULTS

Fig. 4 shows the chip photograph. The two pMOS accumulation capacitors occupy 0.022 mm^2 each and the entire chip, excluding pads, occupies 0.085 mm^2 .

Fig. 5 shows the measured I_C versus V_{EB} variation for transistors of base widths [W_B in Fig. 1(c)] 0.32 and $0.36 \mu\text{m}$ and two values of emitter-collector voltage. The transistor with a narrower base has a higher saturation current and a lower Early voltage (greater separation between the curves for the same change in collector-emitter voltage). Log conformity is good up to a collector current of about $0.5 \mu\text{A}$ for both transistors. The transistor with the wider base ($0.36 \mu\text{m}$) was

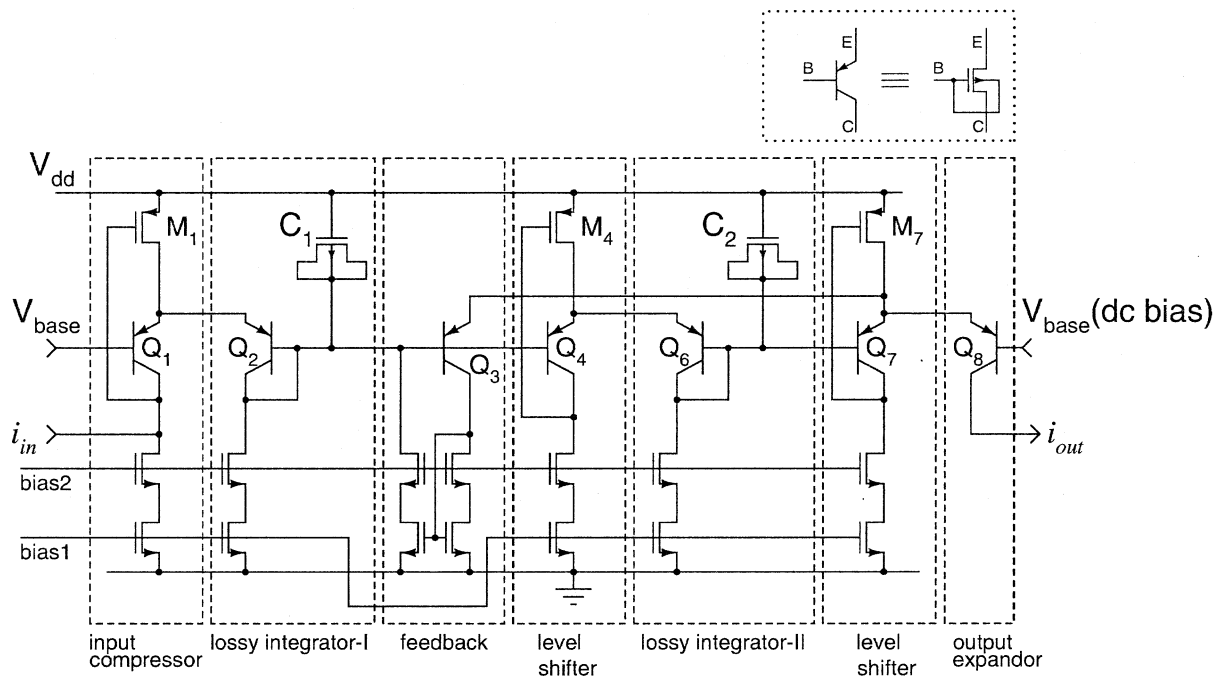


Fig. 3. Log-domain second-order Butterworth filter.

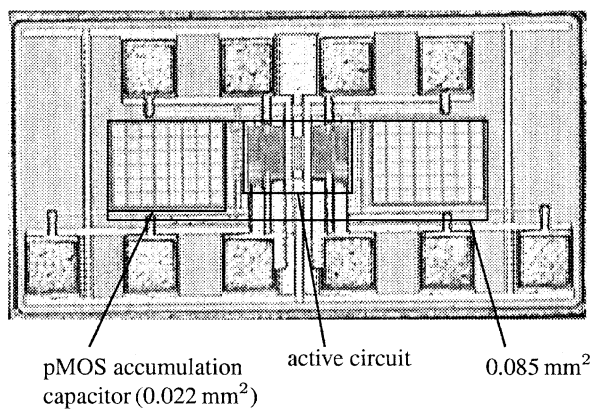


Fig. 4. Chip photograph.

used in the filter described in the previous section. Its measured Early voltage¹ V_A is 2.3 V and the slope factor² is 1.04.

Fig. 6 shows the magnitude response of the filter with various bias currents. At larger values of bias currents, the proportionality of bandwidth to the bias current is not seen. This is due to the transistors deviating from the exponential behavior. With $I_0 = 0.5 \mu A$, the bandwidth is about 22 kHz. The dc gain is more than the expected -6 dB [see (1)] because of the Early effect in the output transistor Q_8 (Fig. 3). The collector of the output transistor is at 0 V due to the measurement setup and its V_{CE} is larger than that of the other transistors in Fig. 3 by about 500 mV. Due to the low Early voltage of the transistors, this difference is enough to change the gain by about 1.3 dB.

¹The small signal output conductance of a bipolar transistor is given by $I_c / (V_A + V_{CE})$ in the active region.

²The collector current of a bipolar transistor is given by $I_c = I_s \exp(V_{BE} / \eta V_t)$ where η is the slope factor.

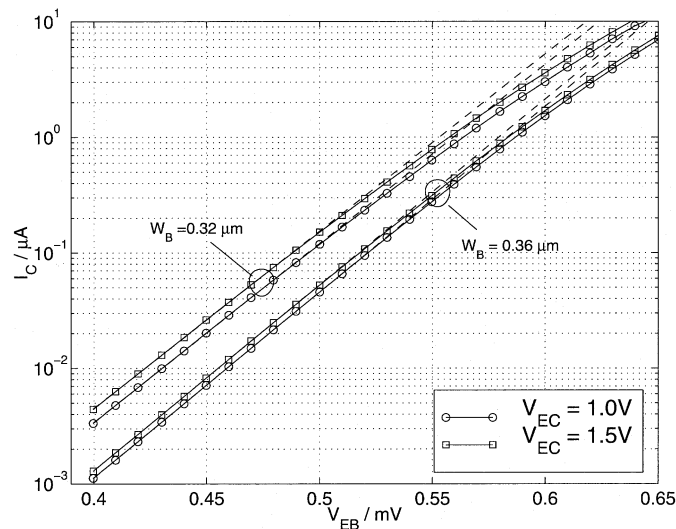


Fig. 5. Measured characteristics of the enhanced lateral p-n-p transistor.

With a 2.5-V supply, the bandwidths for a given bias current are 5%–6% larger.

The measured frequency response for $I_0 = 0.5 \mu A$ and $I_0 = 1 \mu A$ and the ideal second-order Butterworth response are overlaid in Fig. 7. The two measured responses are coincident. The measured attenuation at 1.5 times the bandwidth is about 0.5 dB larger than ideal due to the parasitic pole.

Measurements showed that the second harmonic was larger than the third harmonic, even for input frequencies such that the latter was well within the bandwidth of the filter. The distortion increased with increasing input frequency. Therefore, an input frequency of 10 kHz, about half the filter's bandwidth, was used to obtain a large second harmonic, and hence, a worst case estimate of distortion. The output fundamental component, noise and harmonic distortion products when $I_0 = 0.5 \mu A$ are

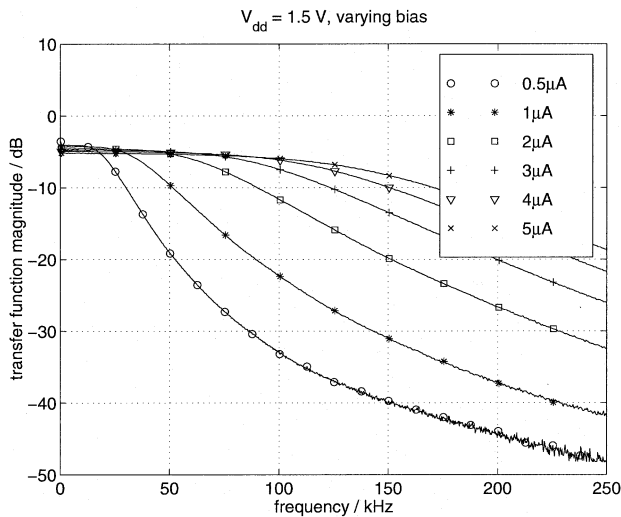


Fig. 6. Frequency response of the second-order filter with a supply voltage of 1.5 V for various values of I_0 shown in the insert.

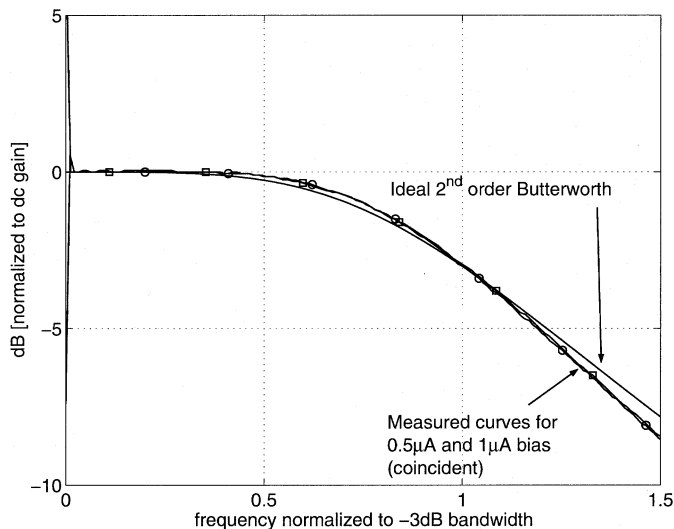


Fig. 7. Compared of the measured frequency response to the ideal Butterworth response.

plotted versus the root-mean-squared (rms) value of the input in Fig. 8. The rms output noise integrated from dc to 50 kHz is 0.25 nA. The maximum value of $S/(N + HD_2)$ is 45 dB. When the total harmonic distortion (THD) is 1% (-40 dB), the filter has a signal-to-noise ratio (S/N) of 56 dB. The filter draws $2.7 \mu\text{A}$ from a 1.5-V supply.

When I_0 is increased to $1 \mu\text{A}$, the filter has a bandwidth of 41 kHz and a current consumption of $5.5 \mu\text{A}$. The output signal, noise, and distortion products (measured with a 20-kHz input tone) of the filter for $I_0 = 1 \mu\text{A}$ are shown in Fig. 9. The output noise (in the 0–100-kHz band) is 0.46 nA. The maximum value of $S/(N + HD_2)$ is 40 dB and S/N with 1% THD is 47 dB. Ideally, a log-domain filter should maintain a constant dynamic range as it is tuned. The smaller dynamic range with $I_0 = 1 \mu\text{A}$ reflects the increased deviation from the exponential characteristic of the lateral bipolar transistor.

Simulations of log-domain filters indicate that the Early effect in bipolar transistors is the dominant cause of distortion. The Early voltage of the lateral transistors is quite small (2.3 V) and

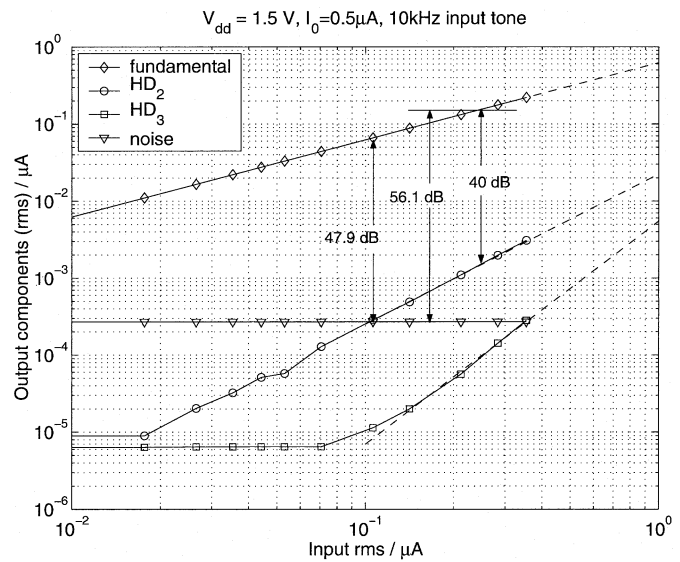


Fig. 8. Signal, noise, and distortion with $I_0 = 0.5 \mu\text{A}$.

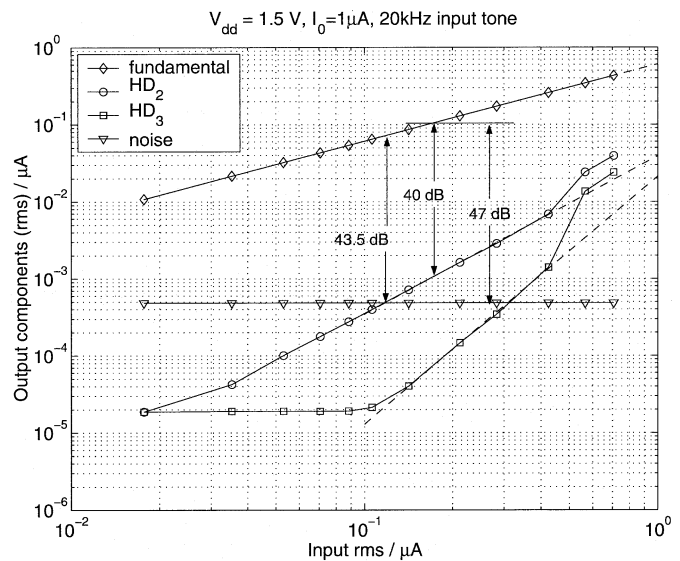


Fig. 9. Signal, noise, and distortion with $I_0 = 1 \mu\text{A}$.

TABLE I
PERFORMANCE SUMMARY

Technology	0.25 μm CMOS	
Chip area	0.085 mm ² (excl. pads)	
Supply voltage	1.5 V	
Bias current (I_0)	0.5 μA	1 μA
-3 dB BW (kHz)	22	41
Power diss. (μW)	4.1	8.3
o/p noise (rms nA)	0.25	0.46
S/N @ 1% THD	56 dB	47 dB
Max. $S/(N + THD)$	45 dB	40 dB
Power dissipation order-bandwidth	93.2 pJ	101.2 pJ

can be increased by using a larger basewidth (see Fig. 5). This should result in a reduced distortion. It can be seen in Figs. 8 and 9 that the THD is dominated by HD_2 . Therefore, pseudo-differential operation can be beneficially used to cancel some of the distortion and improve the filter's performance.

Table I summarizes the performance of the chip.

V. CONCLUSION

The feasibility of micropower low-voltage analog filters in standard digital CMOS process is discussed. It is shown that such filters are possible using MOS transistors in accumulation as capacitors, along with current-mode operation using the log-domain approach with enhanced lateral bipolar transistors. The measured performance of a prototype second-order Butterworth filter in a standard digital CMOS process using these techniques is comparable to that of log-domain filters fabricated in bipolar/BiCMOS processes.

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