COMPANDING SWITCHED CAPACITOR FILTERS

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ABSTRACT

In this paper, two possible switched capacitor implementations of companding filters are discussed. The governing difference equations, an estimate of the increase in the dynamic range for a given power consumption and possible topologies are given.

1. INTRODUCTION

Recently, companding is being investigated as a means of increasing the dynamic range of analog filters, without incurring a proportionate increase in their power consumption. Until now, the focus of research has been on log-domain filters (in bipolar and subthreshold CMOS). We investigate two possible ways of achieving companding with switched capacitor (SC) circuits.

Before proceeding with the analysis, we examine the filters shown in Fig. 1(a). The input block of Filter 2 in Fig. 1(a) is an amplifier of gain $k > 1$. The transfer functions of the two filters are identical. Assume for the moment that the amplifier and the attenuator are noiseless and not limited in their swings, and only the filter embedded between them has a limited dynamic range of DR dB (where dynamic range is defined as the ratio of maximum output signal power P_{max} to the minimum output signal power P_{min}, the latter being assumed to be equal to the output noise power of the filter in absence of any signal). Then, both the filters have a dynamic range of DR dB, but shifted in the absolute level of the signal as shown in Fig. 1(b). It can be seen that with the input amplifier and the output attenuator, the filter performs better at small signal levels, but cannot handle large signals. In a sense, we have one filter suitable for small signals and another for large signals, but neither filter can handle both. *If* it is possible to switch between the two "modes" without distorting the signal, the apparent dynamic range of the resulting filter will be $DR+20\log(k)$ dB (an increase of k^2 in the power ratio P_{max}/P_{min}). Further, if this increase in dynamic range can be achieved without increasing the power consumption or the total capacitance by k^2 (an increase that would be required in a conventional linear filter—see [1]), this approach would have an advantage over a conventional linear filter. We also observe that a scaling of the input or the output by a constant factor does not alter the dynamic range as long as the "scaling blocks" are not excessively noisy.

Continuous time log-domain realizations can be found in [2, 3, 4]. The "analog floating point technique" is described in [5]. The general design of discrete-time companding processors is given in [6].

The following sections deal with the equations and the circuit realizations for companding in a switched capacitor filter, and the increase in the dynamic range over a linear filter for a fixed power consumption. A first order filter is taken as an example and two different approaches are discussed.

2. TIME VARYING TRANSFORMATION OF A DISCRETE TIME ACCUMULATOR

Consider the prototype lossy accumulator shown in Fig. 2. This circuit can be described in terms of its state variable x as:

$$x[n+1] = \frac{B}{B+F}x[n] - \frac{A}{B+F}u[n+1] \quad (1)$$

$$y[n] = Cx[n] \quad (2)$$

where u is the input voltage and y is the output charge (dumped on the next accumulator). In a practical circuit, large inputs cause x to exceed a maximum allowable value V_{max}, saturating the circuit. We seek to derive a modified circuit whose state variable, which we denote by w, does not suffer from this problem, but still maintains the same input-output characteristic as the prototype in Fig. 2. Let the mapping from x to w be of the form $w[n] = g[n]x[n]$, where $g[n]$ is an appropriate sequence[6] to be defined below. Using this in (1)–(2) we obtain:

$$w[n+1] = \frac{B}{B+F}w[n] - \frac{A}{B+F}g[n+1]u[n+1] + \frac{g[n+1]-g[n]}{g[n]}\frac{B}{B+F}w[n] \quad (3)$$

$$y[n] = \frac{C}{g[n]}w[n] \quad (4)$$

The first two terms on the right hand side (RHS) of (3) and the RHS of (4) "resemble" (1) and (2), with extra terms indicating an input scaling factor of $g[n+1]$ and an output scaling factor of $1/g[n]$. The last term of (3) compensates for the distortion when g changes, so that the input-output behavior of (3)–(4) is the same as that of (1)–(2).

A possible x to w mapping is shown in Fig. 3. It can be seen that, for inputs that would have caused x in the prototype to exceed V_{max}, w remains properly bounded. The resultant circuit operates according to the "analog floating point" principle described in [5].

Let us consider an example where x in the prototype increases monotonically, starting from zero. In the companding filter g is initially unity and w follows x. However, when w tries to exceed V_{max}, its value is reset to $0.5V_{max}$, by decreasing the value of g by a factor of 2. This happens again and again as x increases further, as seen in Fig. 3. The values of the slopes that would be encountered in this case would be 1, 1/2, 1/4 etc. If now x

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is imagined to decrease starting from large values, the opposite behavior is observed. When w reduces to $0.5V_{max}$, the gain at the input g is increased by a factor of 2, raising w to V_{max}, as can be deduced from Fig. 3. The example in Fig. 3 uses four values of g ($\{1, 1/2, 1/4, 1/8\}$).

A circuit realizing the companding lossy accumulator described above is shown in Fig. 4. In order to detect the crossings of the preset levels V_{max} and $V_{max}/2$, comparators are employed. Their outputs drive logic circuitry used to set the value of g. In Fig. 4, the output of the op-amp changes in ϕ_2 and is held constant in ϕ_1. Therefore, the comparison is done in ϕ_1 and the circuit prepared appropriately for the next ϕ_2. The scaling of the input and the output is achieved by changing the values of the input capacitor or the output capacitor (input capacitance of the next stage). An array of capacitors is used and the appropriate one switched in.

The last term in (3) vanishes when $g[n+1] = g[n]$. Under that condition, the circuit behaves as a linear accumulator shown in Fig. 2, with an input capacitance of $g[n+1]A$ and and output capacitance of $C/g[n]$.

When g is unchanged, the coefficient of $w[n]$ on the RHS of (3) is $B/(B+F)$. When g changes, the coefficient of $w[n]$ is either $2B/(B+F)$ or $0.5B/(B+F)$ depending on whether $g[n+1] = 2g[n]$ or $g[n+1] = 0.5g[n]$. The former implies a doubling of the state variable (the voltage on the capacitor B) and the latter implies reduction by a factor of two.

The state variable can be doubled by having another capacitor of value B which is charged to w in every cycle and dumping its charge on the feedback capacitor B in the integration phase when a doubling is required [5].

The state variable can be halved as follows: The integrating capacitor B is split into two capacitors $B/2$ each (B_1, B_2 in Fig. 4). For normal operation, the two are placed in parallel and function as the integrating capacitor. Another capacitor B_3 of value $B/2$ is discharged in every cycle. When w needs to be halved, B_2 is disconnected and B_3 is connected across B_1. This halves the voltage across B_1, and leaves a total feedback capacitor of value B, as required by the left hand side of (3). Each time w is halved, B_2 and B_3 interchange their roles in order to ensure uninterrupted operation.

Fig. 4 shows the circuit schematically along with the relevant logic signals. "Inc" and "Dec" denote logic signals indicating an increase or decrease of g respectively. "b_0" is a bit that toggles each time g is halved, so that B_2 and B_3 alternate their roles.

For small signals, the circuit operates with $g = 1$ and the circuit is identical to the prototype without companding (Fig. 2). Therefore, the noise floor is the same as that of the prototype filter. From the arguments presented earlier in this section, and from Fig. 3, it can be seen that the maximum input voltage that can be applied to the companding filter without saturating the op-amp is 8 times larger than the maximum signal that can be applied to the filter in Fig. 2. Consequently, the companding filter has a dynamic range which is $20\log(8)$ dB (a factor of 64) larger than that of the prototype filter. However, the input voltage cannot be allowed to exceed V_{max}; to maintain the advantages mentioned in view of this, one can use smaller input voltages and larger input capacitance (see below).

The effective load on the op-amp in Fig. 2 is

$$C_{load1} = \frac{(B+F)A}{B+F+A} + C \tag{5}$$

and that in Fig. 4 is

$$C_{load2} = \frac{(B+F)Ag[n+1]}{B+F+Ag[n+1]} + C/g[n] \tag{6}$$

Assuming that C dominates A, B and F, the worst case increase in the capacitive loading from the filter in Fig. 2 to that in Fig. 4 is $\max(1/g[n]) = 8$. To drive this increased load, the op-amp needs to be biased at a current which is 8 times larger, and hence, the power consumption increases by a factor of 8 ($10\log(8)$ dB). The worst case increase in the capacitance used is $(C+2C+4C+8C)/C = 15$. Since the dynamic range went up by a factor of 64 ($20\log(8)$ dB), the companding filter has a significantly larger dynamic range for a given power consumption than a conventional linear filter. In practical SC circuits, C does not quite dominate A, B & F. A more precise calculation for a 6^{th} order 0.5 dB Chebyshev filter with a cutoff frequency of $f_s/10$ and four values of g as implied in Fig. 3 shows an increase in the total capacitance by a factor of 7.7. This is 8.3 times smaller than the increase in total capacitance (a factor of 64) that would be demanded by a conventional linear filter[1] for the same increase in the dynamic range. Similarly, the increase in the power consumption is 8 times smaller than in a conventional linear filter.

The above estimates do not include the power consumed by the control circuitry and the comparators, or the increased slew-rate requirements on the op-amp due to the "jumps" in the characteristic of Fig. 3, which in practice, will reduce the "advantage" estimated above. By generalizing the method followed in the previous paragraphs, it can be found that the improvement in the dynamic range per unit power consumption of a companding filter increases with the number of g values used (number of different slopes in Fig. 3). But, the spread in capacitance values increases exponentially with the number of g values used, and the use of a very large number of g values is impractical.

A higher order filter can be built using the companding accumulators described above. The capacitor array at the output of one stage can be combined with the array at the input of the following stage to form a bigger array, which is controlled using the logic signals derived from both the stages. The voltage levels at the output of each op-amp will be a compressed version of the voltages present in a conventional linear filter. After the final accumulator, an expander must be used to recover the "linear" output (which is related to the input through the relevant linear time invariant difference equations). This consists of a SC amplifier with a switchable input capacitor array.

Fig. 6 shows the time response of a 6^{th} order 0.5 dB Chebyshev filter (cutoff = $f_s/10$) to a sinusoidal input at $f_s/64$ obtained from SWITCAP simulation. The output of the last op-amp and the expanded outputs are shown for input amplitudes of 0.9V, 3V and 8V. The compressed version (the voltage at the op-amp output) has nearly the same swing for an input which varies by as much as 1:9. Thus, by preventing the op-amp outputs from overloading in presence of large inputs, companding achieves a larger dynamic range than a conventional filter.

By compressing the outputs of the op-amps, input voltages larger than those allowable in a conventional linear filter can be applied. However, breakdown constraints can preclude large input voltages. This situation can be rectified by increasing the size of the input capacitance and reducing the magnitude of the input voltage—a 1 V input sampled by a 1 pF capacitor is the same as a 0.25 V signal sampled by a 4 pF capacitor as far as the signal is concerned.

3. COMPANDING ACCUMULATOR USING A NONLINEAR BLOCK AT THE OUTPUT

Another approach to realize companding switched capacitor filters would be to imitate log-domain filters by using a piecewise linear exponential expander at the output in place of the bipolar transistor in a log-domain filter. Fig. 5 shows such a curve having four segments with successive slopes increasing by a factor of two. As in section 2., we seek to modify the state variable description of the prototype lossy accumulator given by (1)–(2) to obtain the companding accumulator. The output charge y is related to the new state variable w through $y = C(a_n w[n] + b_n)$ where $a_n = a(w[n])$ and $b_n = b(w[n])$ are the slope and the intercept of the characteristic shown in Fig. 5. Using this in (1)–(2) and rearranging, we get:

$$w[n+1] = \frac{B}{B+F} w[n] - \frac{A}{B+F} \frac{u[n+1]}{a_{n+1}} \frac{B}{B+F} \frac{(a_n - a_{n+1}) w[n] + b_n - b_{n+1}}{a_{n+1}} \quad (7)$$

$$y[n] = C(a_n w[n] + b_n) \quad (8)$$

(7) describes a lossy accumulator with gain switching $(u[n+1]/a_{n+1})$ along with a term which compensates for changes in a_n, b_n. This circuit can be implemented along lines similar to that described in section 2. The details are not given due to lack of space.

For very small signals, the circuit operates in the first segment of Fig. 5 (slope=1). Therefore, the output noise is the same as that in a conventional linear filter. From Fig. 5, it can be seen that the maximum output charge is 3.75 $((2^4 - 1)/4)$ times the maximum output charge in a conventional linear filter. Therefore, the dynamic range increases by 20 log(3.75) dB.

By following steps similar to those in section 2., it can be found that the worst case capacitive loading increases by a factor of 8 (when the circuit is operating on the last segment of Fig. 5). The maximum output charge increases by a factor of 3.75. Therefore, the op-amp needs to be biased at a correspondingly larger current, leading to a 3.75 times increase in the power dissipation. The increase in the dynamic range is more than the increase in the power consumption and hence, the circuit is advantageous over a linear filter.

The increase in the dynamic range for a fixed power consumption is smaller for this circuit than for that described in section 2. So, the latter is better in terms of improvement in the dynamic range.

From Fig. 3 and the description in section 2., it is clear that the output voltage of the op-amp in Fig. 4 jumps by $V_{max}/2$ each time g changes, whereas the characteristic described by Fig. 5 is continuous and the jumps at the output of the op-amp are generally smaller. This implies that the circuit described in this section has less stringent slew-rate requirements than that in section 2.

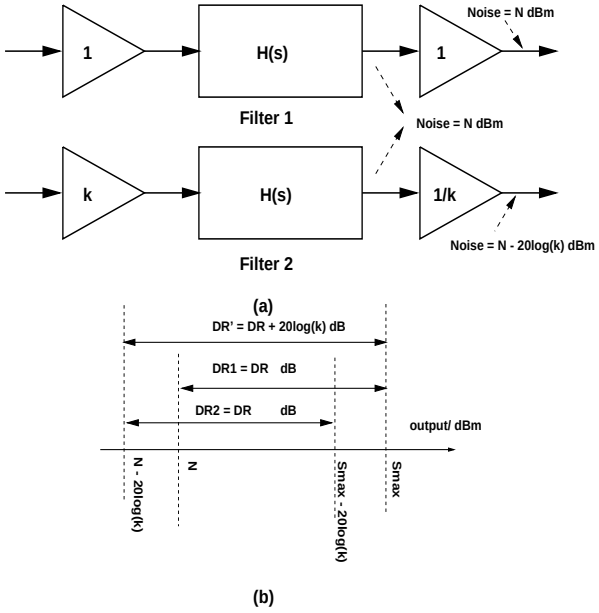

Figure 1. Two filters with skewed operating ranges.

4. CONCLUSION

This article discusses two possible methods for realizing switched capacitor companding circuits and their advantages over conventional linear filters.

5. ACKNOWLEDGMENTS

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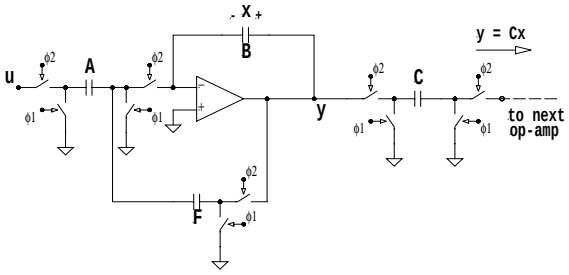

Figure 2. Lossy accumulator without companding.

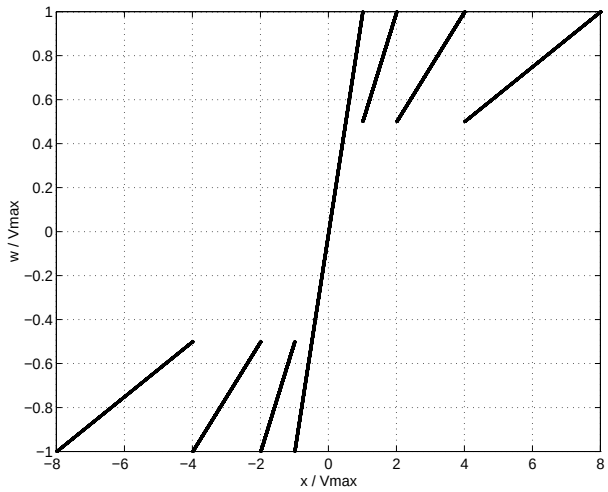

Figure 3. Mapping from x to w.

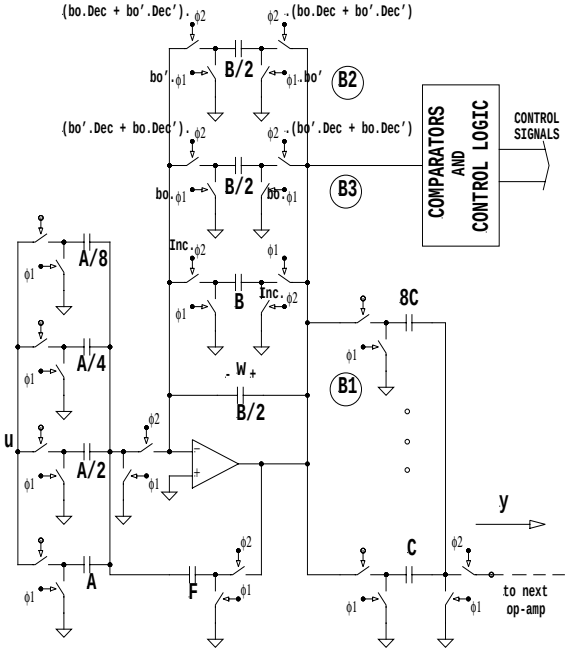

Figure 4. Lossy accumulator with companding.

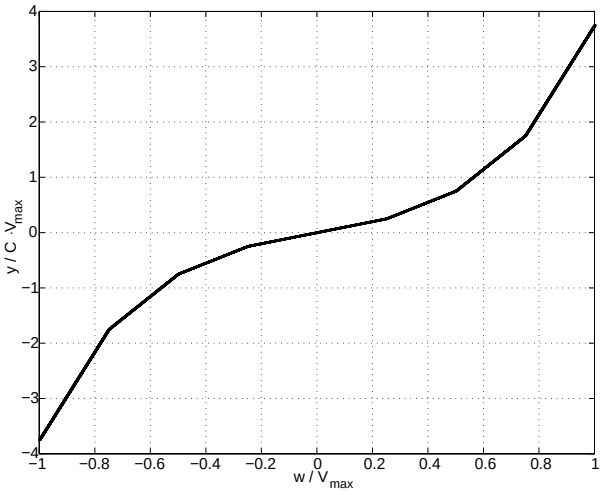

Figure 5. Piecewise linear exponential.

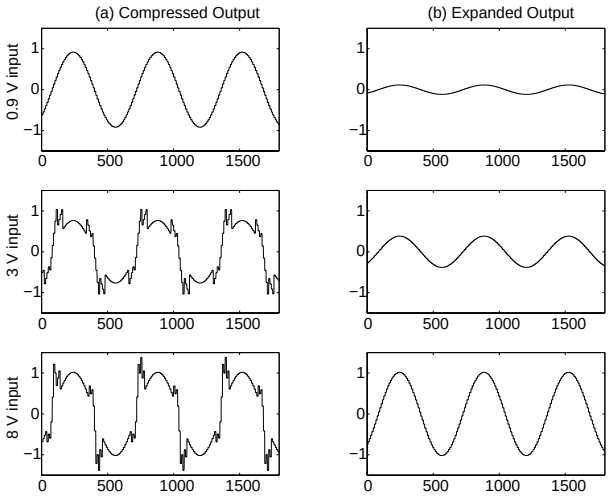

Figure 6. Waveforms in a SC Chebyshev filter with companding. Top trace: 0.9 V input, middle trace: 3 V input, bottom trace: 8 V input.