Synthesis Based Introduction to Opamps and Phase Locked Loops

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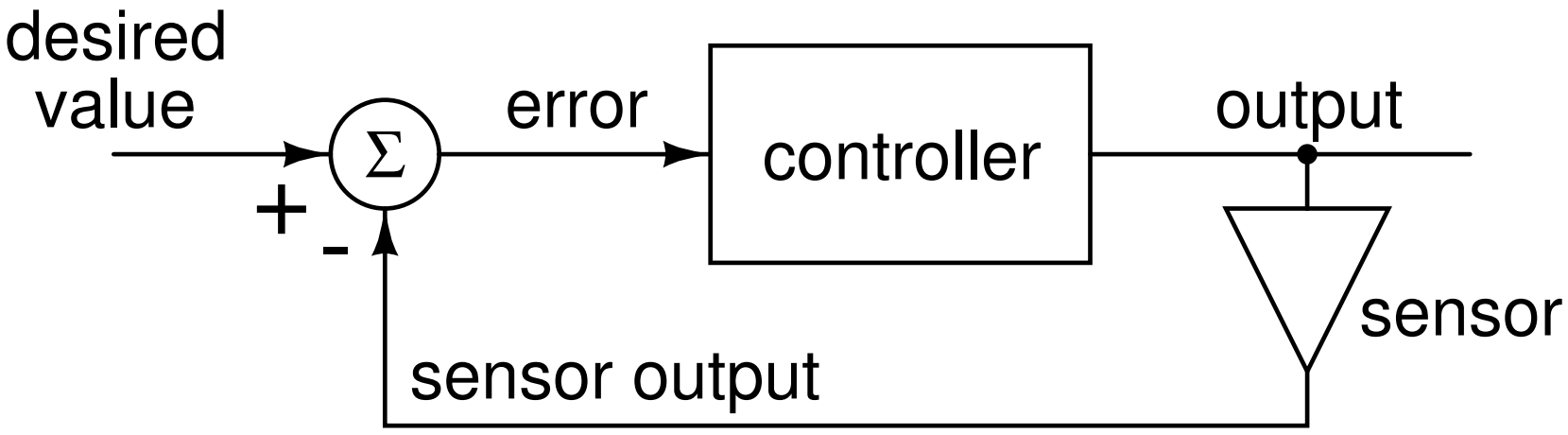
Outline

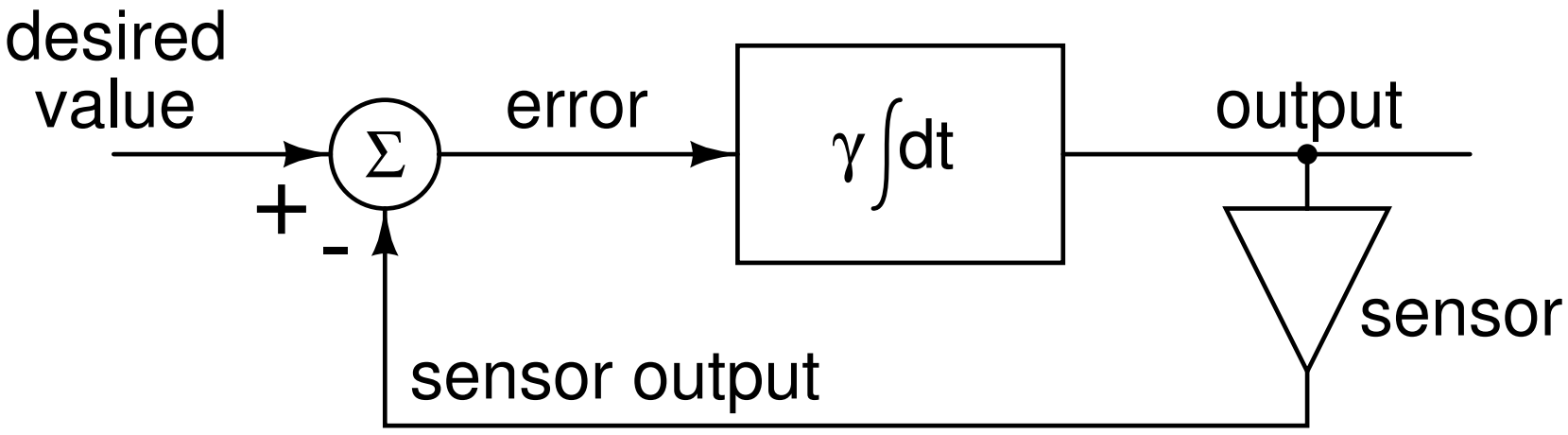
- Negative feedback amplifier
  - Integrate the error to drive the output
- Opamp to compute and integrate the error
  - G_m loaded by a capacitor—Single stage opamp
  - Better I-V conversion—Two stage opamp
  - Further refinement—Three stage opamp
- PLL as negative feedback frequency multiplier
  - Integrate frequency error to drive the output—Type I PLL
  - Static phase error causes reference spurs
  - Additional integrator to null phase error—Type II PLL
- Conclusions

Negative feedback system



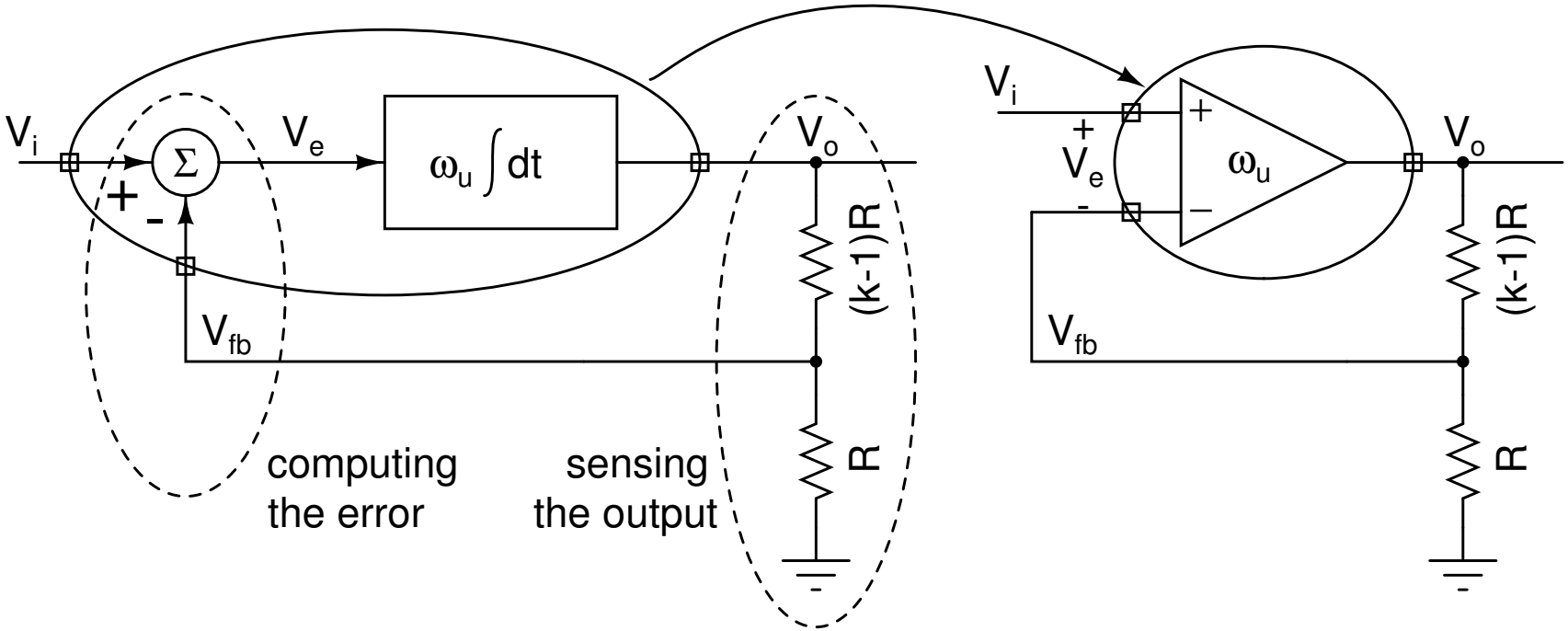
- Controller: Continuously changes the input until error goes to zero

Negative feedback system



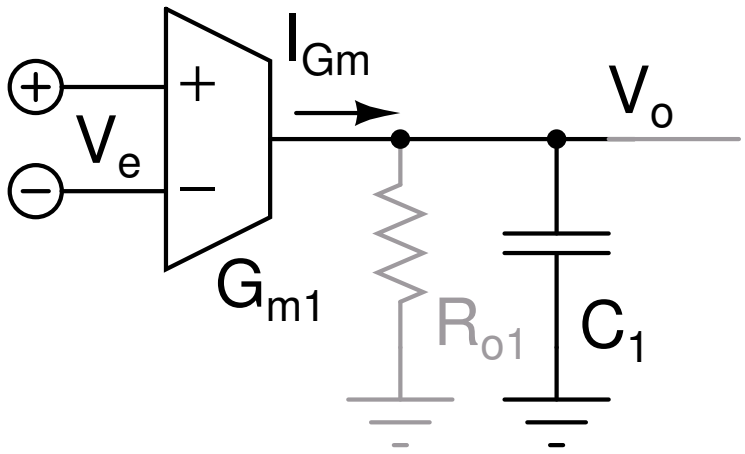
- Controller: Continuously changes the input until error goes to zero

Negative feedback amplifier



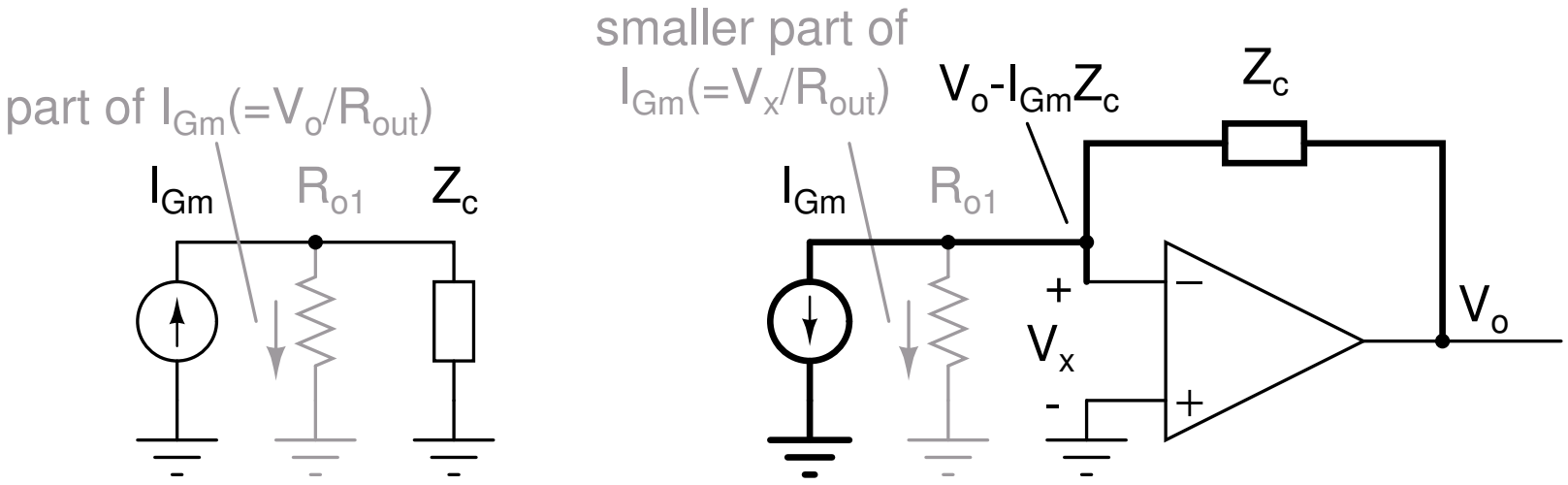
- Integrate the error $V_i - V_o/k$ to drive the output
- Opamp computes the error and integrates it

Opamp (integrator) realization



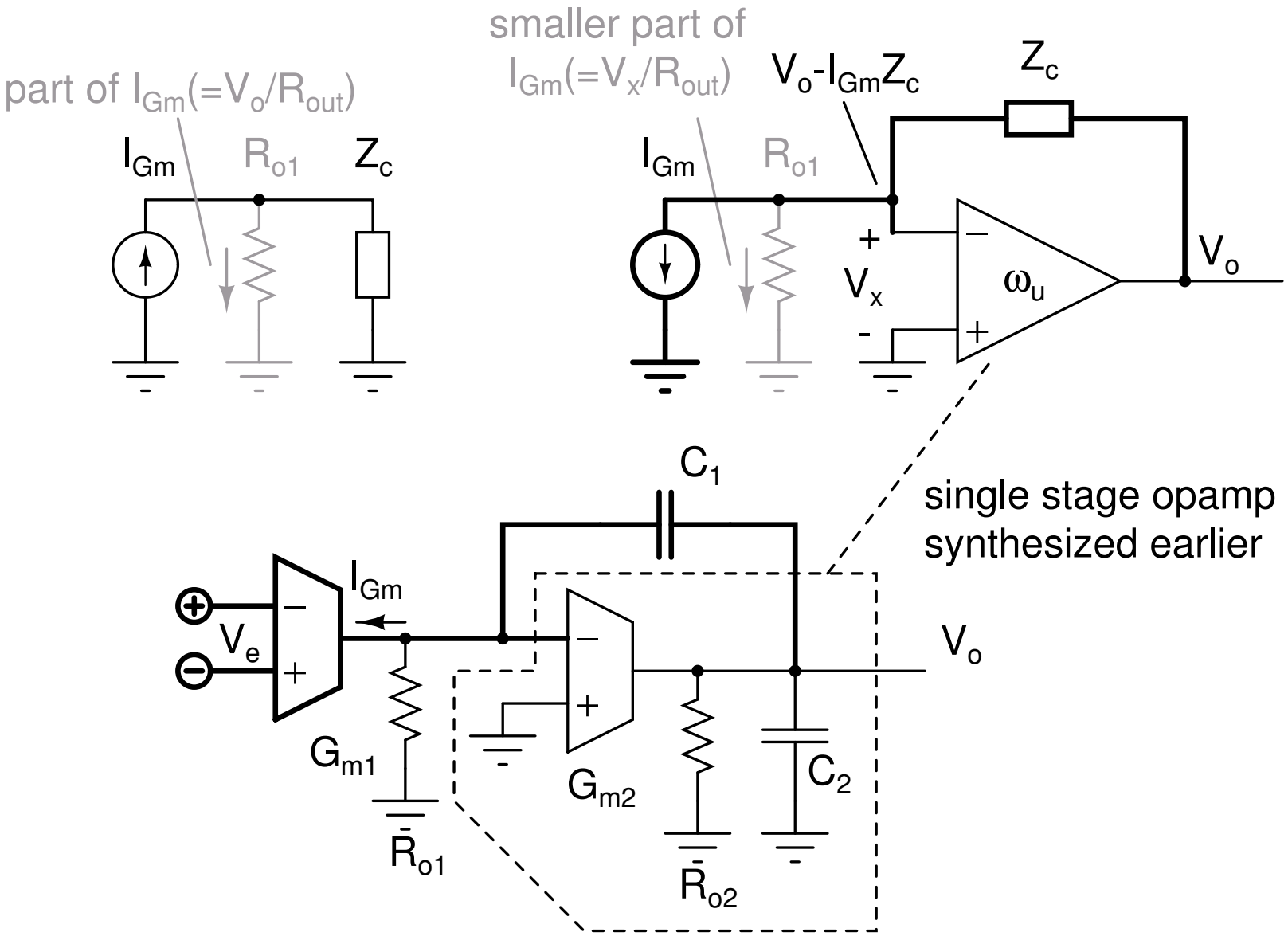
- $G_m - C$ integrator
- Finite $R_{o1} \Rightarrow$ Finite dc gain $\Rightarrow$ Steady state error

Transimpedance amplifier for better I-V conversion



- Use negative feedback to realize a CCVS
- $V_o \approx I_{Gm}Z_c$ within the unity loop gain frequency

Improved I-V conversion—Two stage opamp



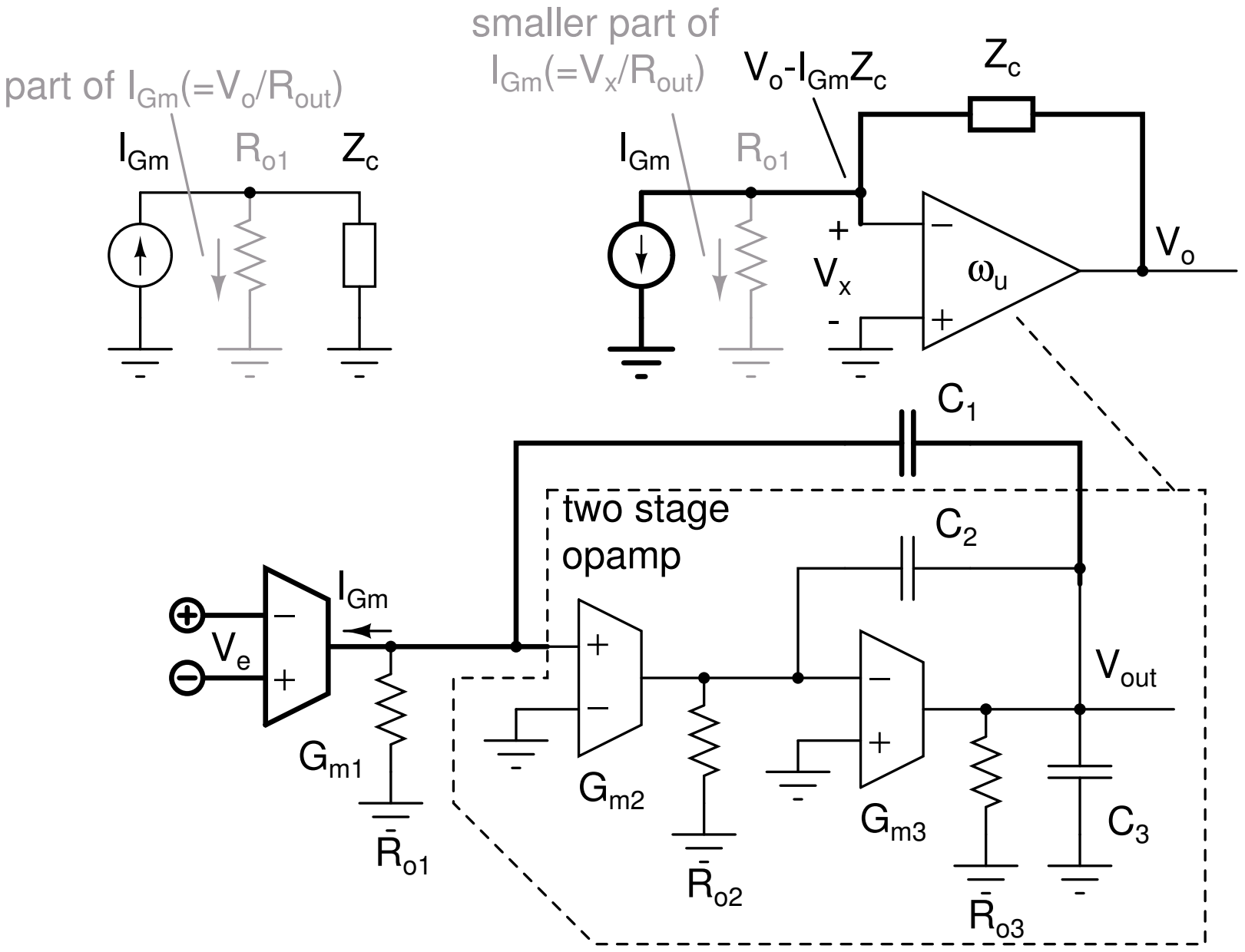
Intuition about two stage opamp

I-V conversion bandwidth $\approx$ unity loop gain frequency

$$\omega_{u,desired} < \omega_{u,inner}$$

$$\frac{G_{m1}}{C} < \frac{G_{m2}}{C_2}$$

Further improvement—Three stage opamp



Intuition about three stage opamp

I-V conversion bandwidth $\approx$ unity loop gain frequency

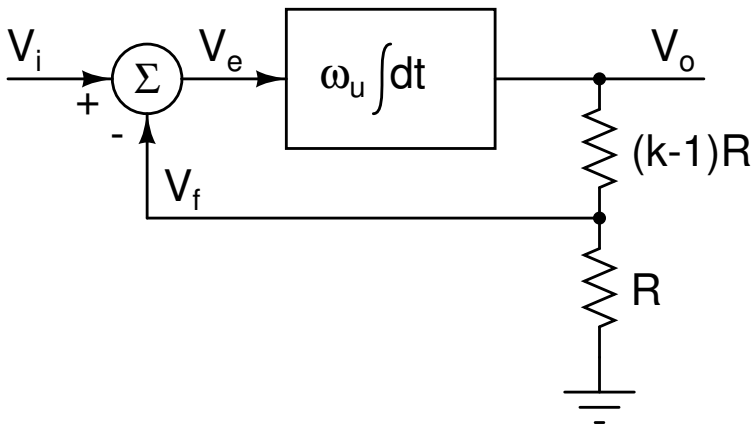
$$\omega_{u,desired} < \omega_{u,inner}$$

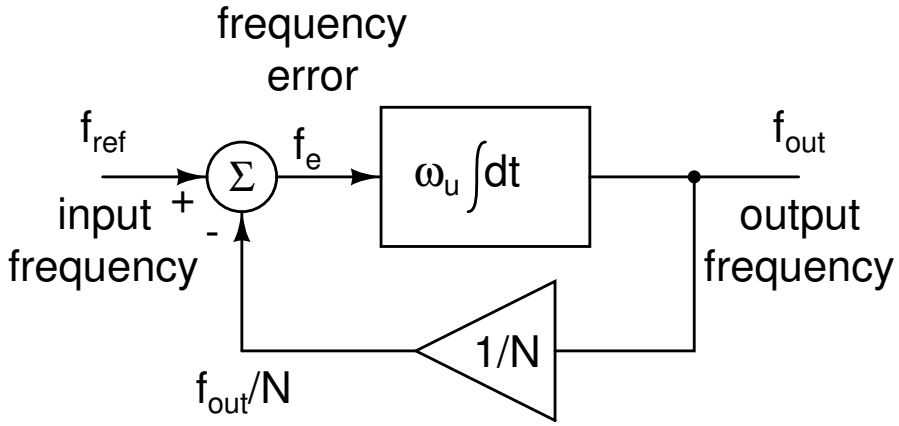
$$\frac{G_{m1}}{C} < \frac{G_{m2}}{C_2} < \frac{G_{m3}}{C_3}$$

Analysis of two and three stage opamps

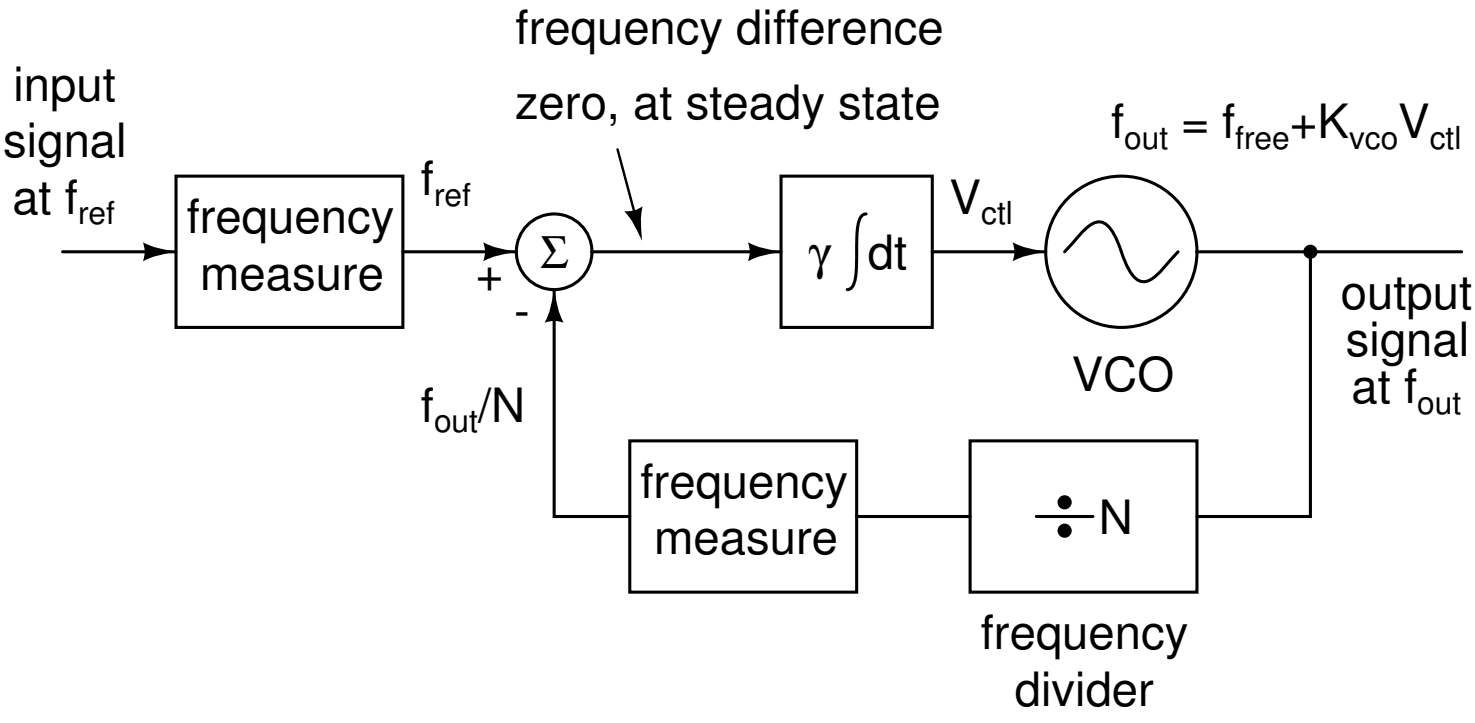
- Two stage opamp
  - DC gain
  - Pole locations, pole splitting
  - Stability constraints
  - RHP zero and its cancellation
- Three stage opamp
  - DC gain
  - Pole locations
  - Stability constraints
  - Zero pair and their optimization

Frequency multiplication analogous to voltage amplification

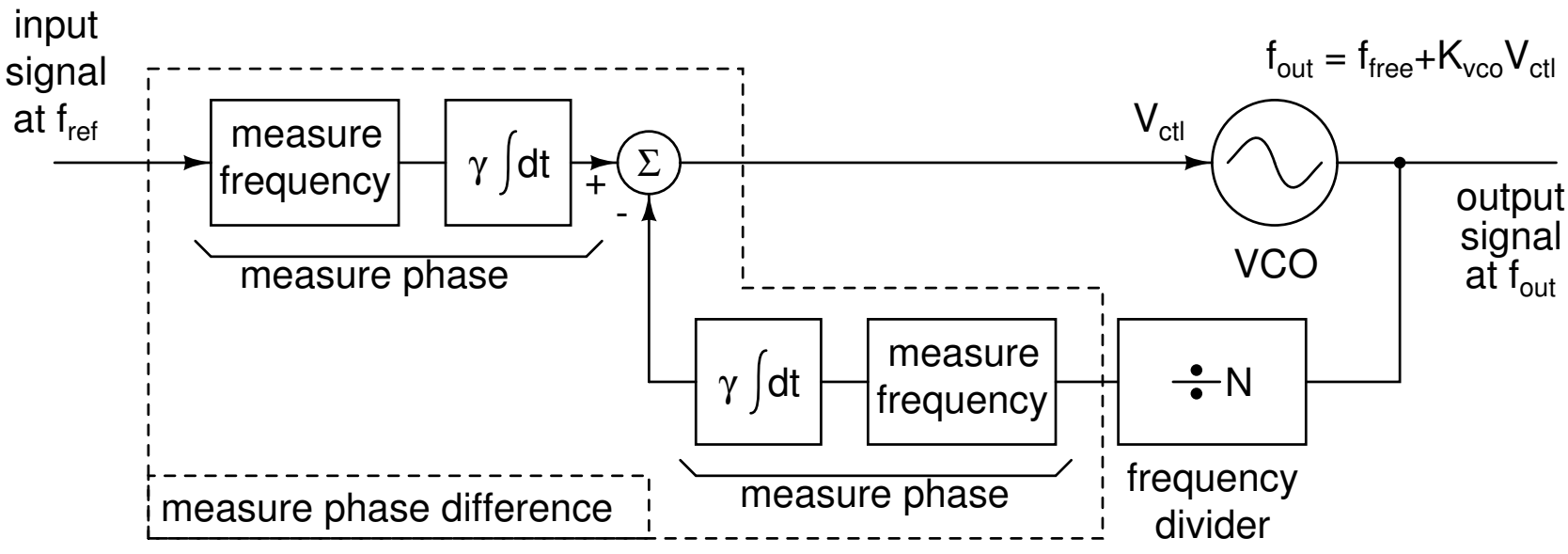




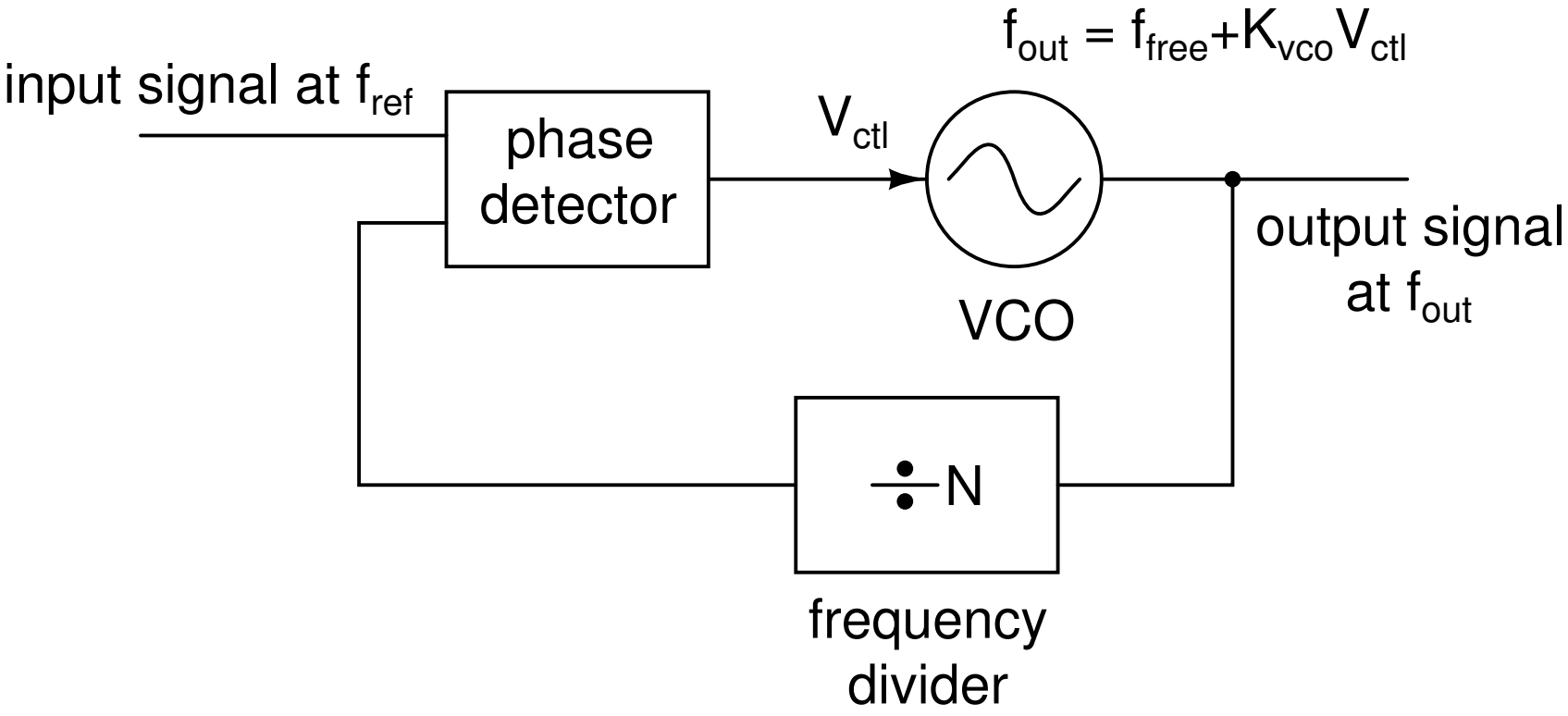
Frequency multiplication



Integrate frequency difference ⇒ Phase difference

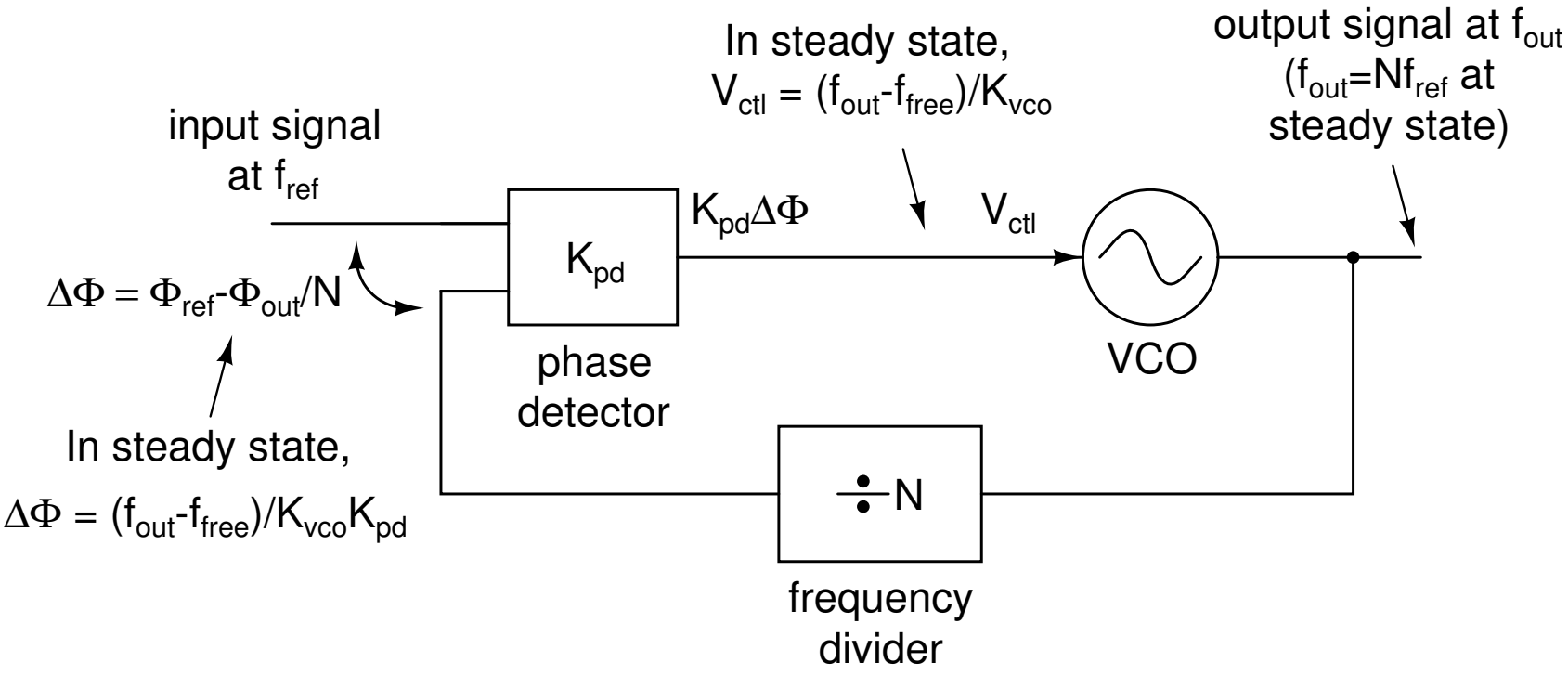


Type I phase locked loop



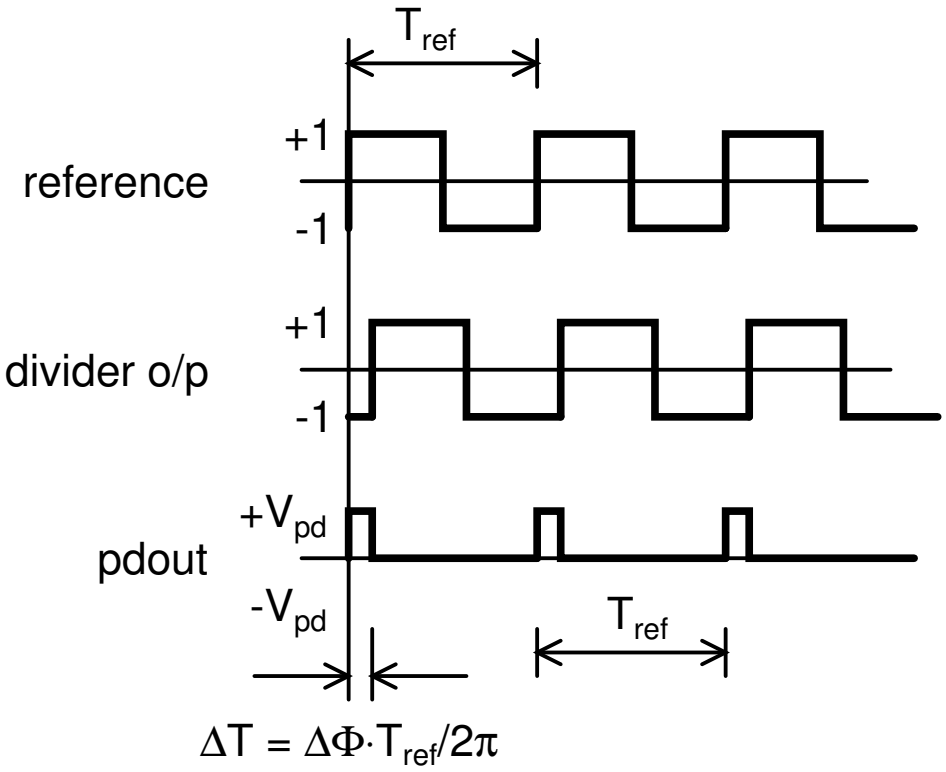
- Phase detector and VCO in a loop

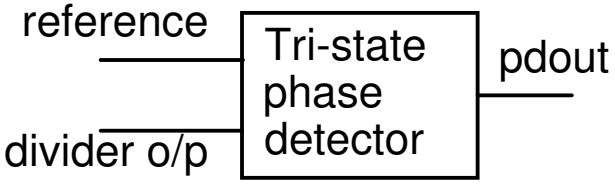
Type I phase locked loop



- Phase offset $\Delta\Phi = (f_{out} - f_{free})/K_{vco}K_{pd}$ between input and feedback signals
- $|\Delta\Phi|$ limited to $\pm n\pi$ due to periodic nature of phase
- Limited lock range $|f_{out} - f_{free}|$

Tri state phase detector example





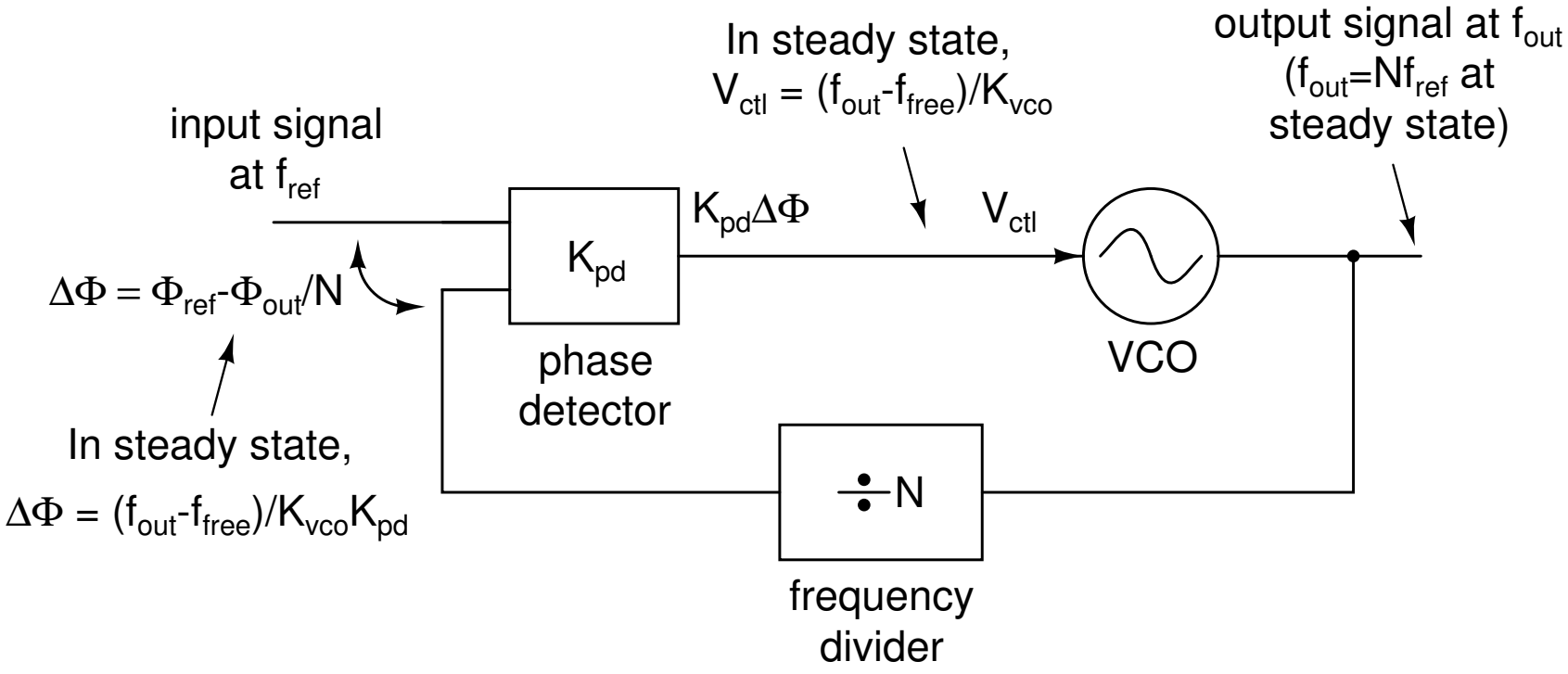
$$\frac{V_{out}(t)}{V_{pd}} = \underbrace{\frac{\Delta\Phi}{2\pi}}_{\text{Average}} + \underbrace{\frac{\Delta\Phi}{\pi}\sum_{n=1}^{\infty}\text{sinc}\left(\frac{n\Delta\Phi}{\pi}\right)\cos(2\pi n f_{ref}t - n\Delta\Phi/2)}_{\text{Periodic error at } f_{ref} \propto \Delta\Phi}$$

Type I PLL with a practical phase detector

- Output average value $\propto \Delta\Phi$
- Periodic signal at f_{ref}
- Periodic signal magnitude proportional to $\Delta\Phi$
- VCO modulated at f_{ref} and its harmonics
- PLL output has sidebands at integer multiples of f_{ref}

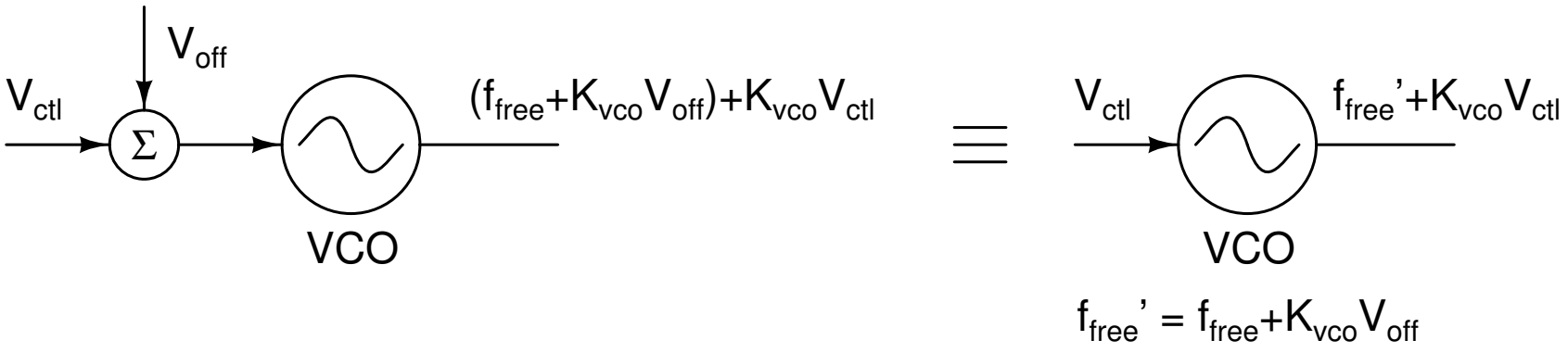
For a modest sideband level of -40 dB, PLL lock range $\approx 10^{-4} f_{ref}$. Cannot change N at all!

Type I phase locked loop



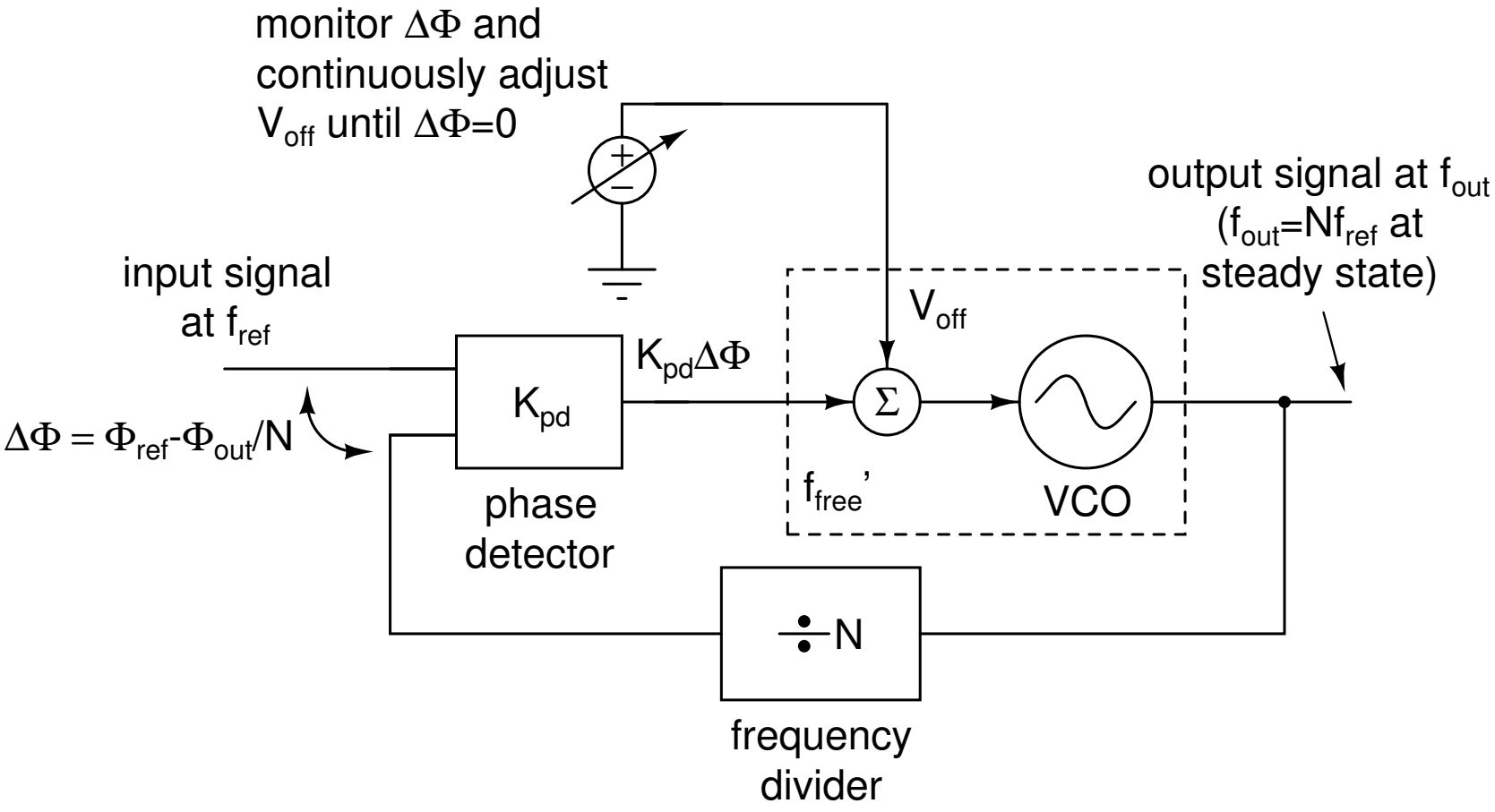
$\Delta\Phi = 0$ if f_{out} happens to be equal to f_{ref}. Zero spurs!

Changing the free running frequency of a VCO



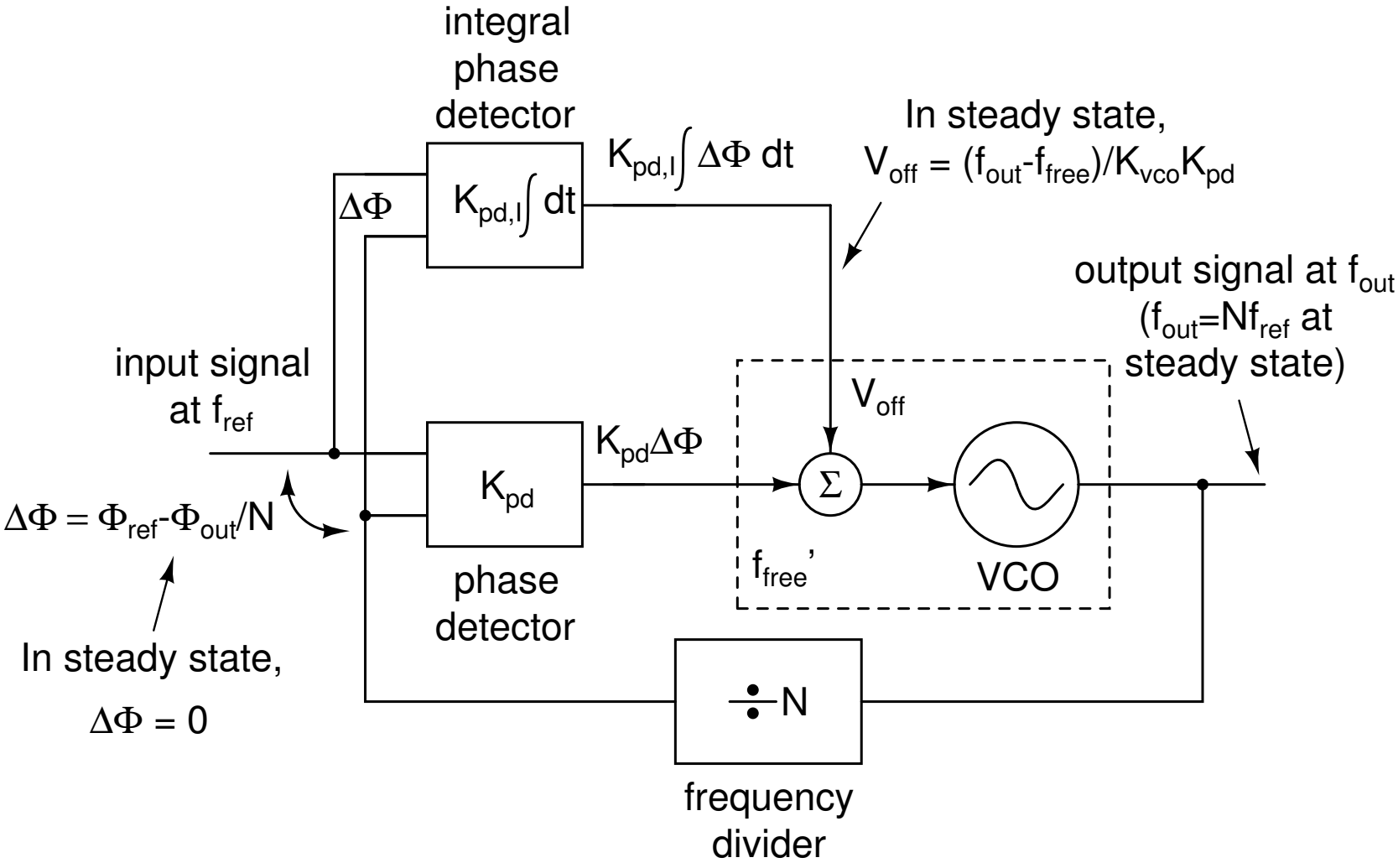
- Add a bias to the input to change the free running frequency

Slowly change the bias until $\Delta\phi = 0$



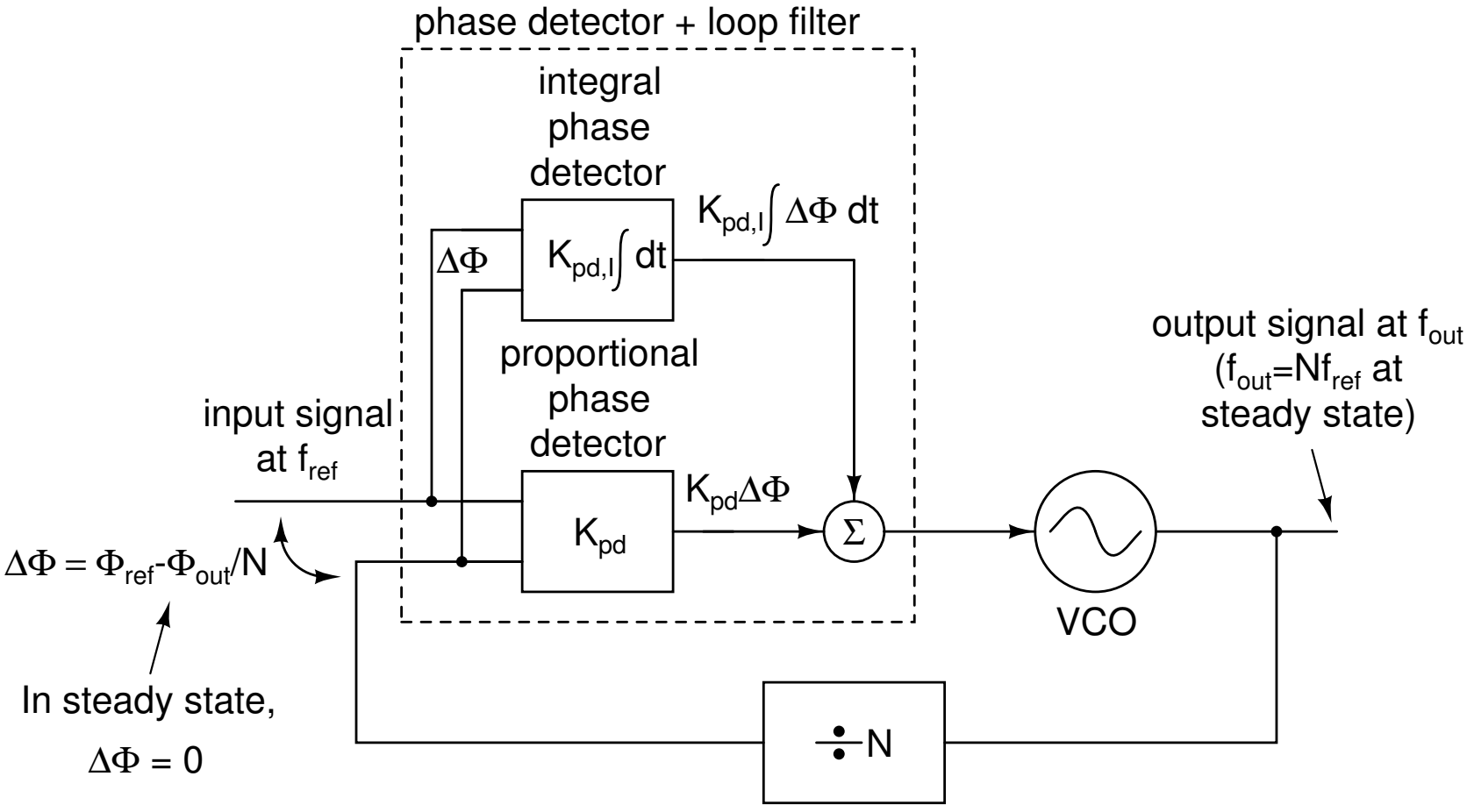
- Slowly change the bias V_{off} until $\Delta\phi = 0$

Slowly change the bias until $\Delta\phi = 0$



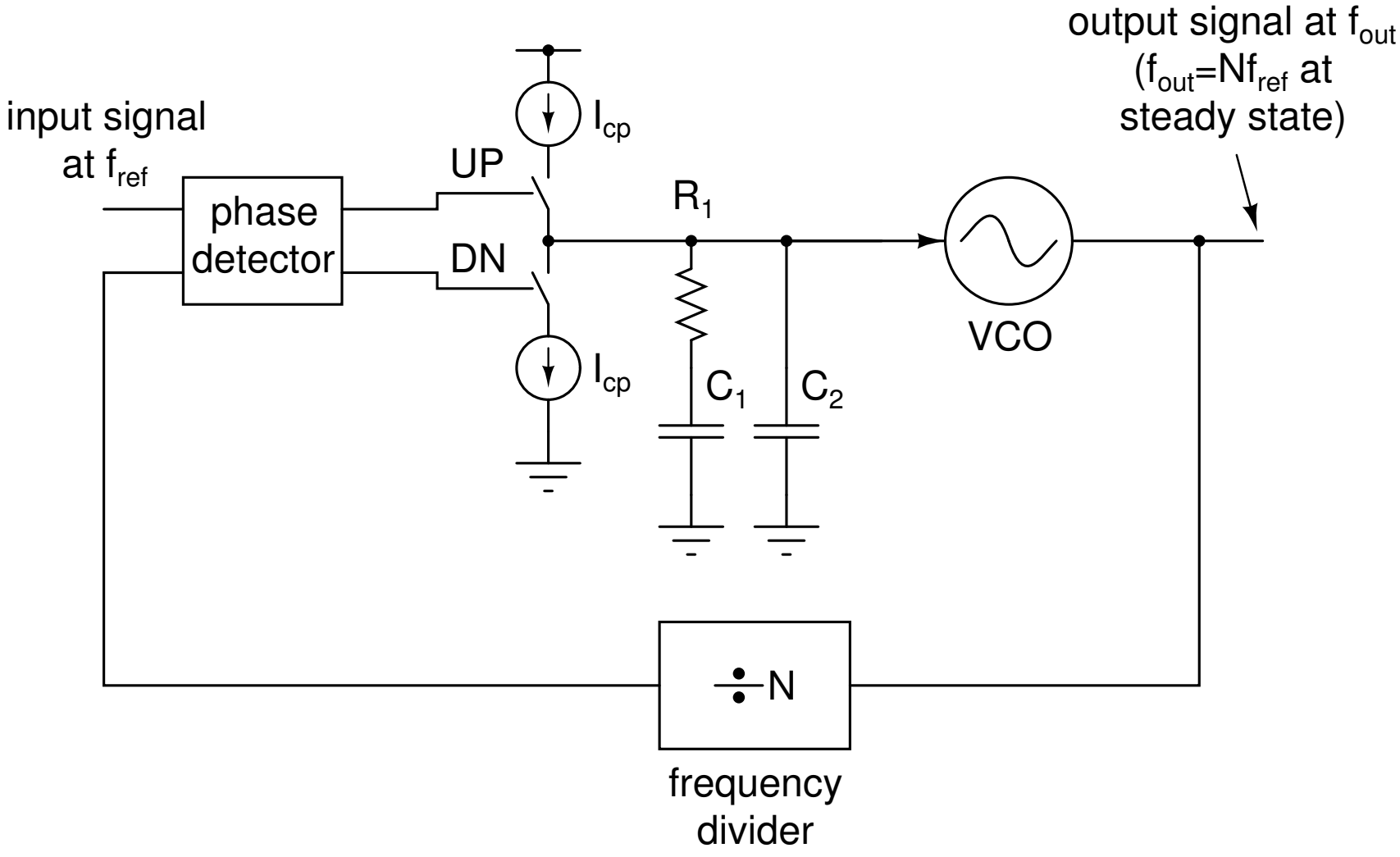
- Measure $\Delta\phi$ and integrate it to control V_{off}

Type II Phase locked loop



- Proportional + integral loop filter

Type II Phase locked loop implementation



Intuition about the Phase locked loop

- Reason for using a phase detector for frequency synthesis
- Reason for an additional integrator in the loop filter
- Integral path for adjusting V_{off} slower than the main path (type I)
  - PLL bandwidth (unity loop gain frequency) is the same as in the type I loop
  - Presence of a zero before the PLL bandwidth (unity loop gain frequency)
  - Integral path influences the phase transfer functions only well below the PLL bandwidth

Analysis of type II Phase locked loop

- Pole zero locations
- Phase (jitter) transfer functions
- Higher order loop filter for higher spur suppression

Suggested course outline

- Negative feedback circuits
- Stability analysis
- **Opamp topologies using controlled sources (G_m)**
- Opamp topologies at the transistor level
- **Phase locked loop at the system level**

Conclusions

- Negative feedback: *Continuous* adjustment to reduce error
- Integrator is the key element of the negative feedback loop
- Implementing a voltage integrator and seeking to improve its performance leads to commonly used opamp topologies
- Implementing a negative feedback frequency multiplier and seeking to improve its performance leads to type I and II phase locked loops
- Valuable intuition gained before embarking on analysis

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