Synthesis Based Introduction to Opamps and Phase Locked Loops

Nagendra Krishnapura
Department of Electrical Engineering, Indian Institute of Technology, Madras, Chennai 600 036, India

***Abstract*— The opamp and the phase locked loop can be synthesized from the prototype negative feedback system which uses an integrator to continuously drive the output until the error between the desired and actual outputs becomes zero. Different opamp topologies are shown to be logical outcomes of synthesizing such a system and progressively improving its performance. The phase locked loop is synthesized as a frequency multiplier, analogous to a voltage amplifier. The synthetic approach from a common foundation helps students to easily make connections between different negative feedback circuits.**

I. Motivation

A graduate course in analog integrated circuit design necessarily includes a discussion of negative feedback systems and stability, design of opamps and their frequency compensation schemes. Frequently, the phase locked loop is also introduced in such a course. Traditionally, the topologies have been taken for granted and the focus has been on analysis[1]. This paper outlines a synthesis based introduction to these circuits. The author believes that this approach gives students some intuition about their behavior before diving into analysis. Integrating synthesis with analysis is also necessary to make it easier for students to apply what they have learned[2]. The synthesis presented here is based on a negative feedback system which continuously drives the output until the error between desired and actual values is reduced to zero. Opamp topologies are developed as progressively better realizations of an integrator which is used as the controller in the negative feedback system. The phase locked loop is developed analogous to an amplifier as a negative feedback circuit that can be used to multiply (amplify) the input frequency. None of the circuits in this paper is new. What is presented is a synthesis based introduction which the author believes is more intuitive than traditional approaches.

The following section briefly introduces the negative feedback amplifier with an integrator at its core. The opamp is defined as the building block which measures the error between desired and sensed values and integrates it[3]. Section III shows the synthesis of the opamp starting with the simplest way to implement such an integrator. Two- and three-stage opamp topologies are derived in an attempt to make the opamp behave closer to an ideal integrator. Section IV introduces the type-I phase locked loop as a frequency multiplier which is analogous to a voltage amplifier. Section V briefly outlines a method for developing the type-II PLL along similar lines. Section VI suggests a possible flow of topics in a course incorporating the ideas in this paper. Section VII concludes the paper.

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II. Negative feedback system using an integrator

In [3], The intuitive notion of negative feedback as a system which senses the output, compares it to the desired value, and *continuously drives the output until it reaches the desired value* (Fig. 1(a)) is shown to lead to a controller which integrates the error and drives the output (Fig. 1(b)). Using this principle to realize an amplifier with gain k and input and output voltages of V_i and V_o respectively leads to the system in Fig. 2(a). The error $V_e = V_i - V_o/k$ is integrated to drive the output V_o. By inspection, it is clear that the output settles to kV_i when the input V_i is a constant. As shown in Fig. 2(b), The opamp is then defined as a block that takes the difference between desired and sensed values and integrates the difference[3].

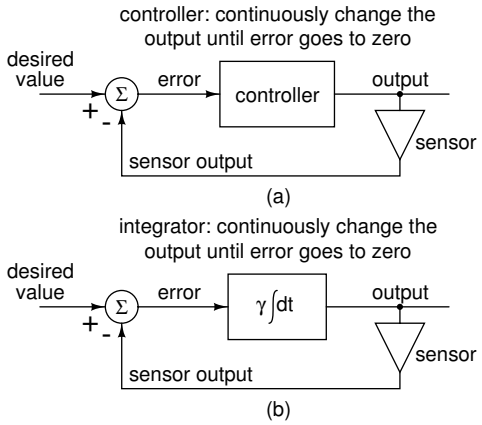

Fig. 1. (a) Conceptual diagram of a negative feedback system, (b) Negative feedback system using an integrator as controller (γ is a constant with the appropriate dimensions)[3].

III. Synthesis of opamp topologies

A. Single stage opamp; DC gain limitation

The simplest way of implementing the opamp's function, i.e. integrating the input difference voltage, is to generate a current proportional to the input difference voltage V_e using a transconductor G_{m1} and passing the output current into a capacitor C_1 as shown in Fig. 3. If $R_{o1} = \infty$, the circuit realizes

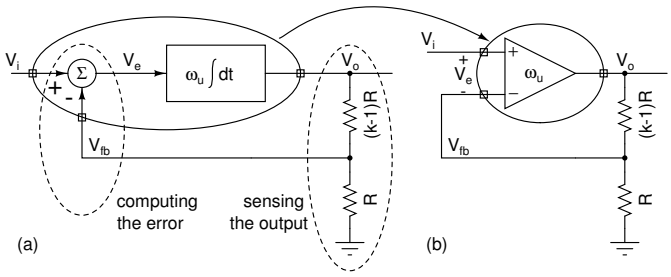

Fig. 2. (a) Negative feedback amplifier using an integrator (ω_u is a constant with dimensions of frequency), (b) Opamp as a combination of error computation and integration[3]. The resulting amplifier is the classic non-inverting amplifier.

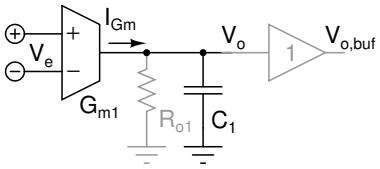

Fig. 3. Realizing an integrator using a transconductor and capacitor. R_{o1} is the output resistance of the transconductor. The buffer shown in gray may be used for isolating heavy loads.

an opamp with a unity gain frequency $\omega_u = G_{m1}/C_1$. The output may be buffered if driving a resistive load.

It is well known that one cannot realize a (controlled) current source with an infinite output resistance. The transfer function including R_{o1} is

$$\frac{V_o(s)}{V_e(s)} = \frac{G_{m1}R_{o1}}{1+sC_1R_{o1}} = \frac{1}{1/G_{m1}R_{o1}+sC_1/G_{m1}} \qquad (1)$$

The first form above makes the dc gain $A_o = G_{m1}R_{o1}$ explicit, and the second one makes it clear that a small non-ideal term $1/G_{m1}R_{o1}$ is added to the term that represents integration in the denominator. Analyzing the prototype amplifier (Fig. 2(b)) with the opamp model in Eq. 1, it becomes clear that the amplifier's gain is reduced to $k/(1+k/A_o)$. The value of A_o that can be realized with a single transconductor limits the accuracy of this amplifier. Attempts to overcome this problem result in more sophisticated opamp topologies as discussed below.

B. Cascode opamp

The dc gain can be improved by improving R_{o1}, i.e. making a better controlled current source. This can be done by adding cascode transistors (common gate amplifiers or current buffers) to the transconductor implementation. Choosing to use cascode transistors of the same polarity or opposite polarity of the transistors in the transconductor G_{m1} results in telescopic and folded cascode topologies respectively. This is not further discussed here.

C. Two stage miller compensated opamp

In Fig. 3, the current from the transconductor is passed through an impedance $Z_c = 1/sC_1$ by connecting the latter across the transconductor's output. The voltage V_o equals

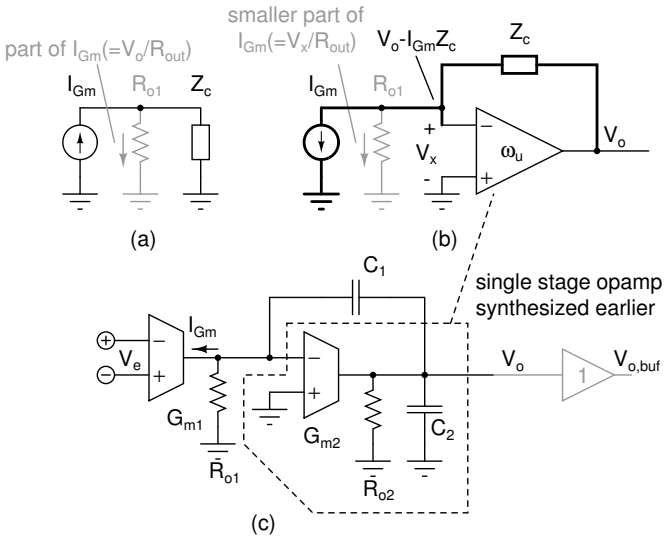

Fig. 4. (a) Crude I-V conversion, (b) Better I-V conversion using negative feedback, (c) A better opamp using the idea in (b).

I_{Gm}/Z_c. When the transconductor has a finite output resistance R_{o1}, some of the current that should have flown into Z_c flows into R_{o1} instead. This is shown in Fig. 4(a). This is what causes a finite dc gain. A better way of converting the output current of G_{m1} into voltage is to realize a current controlled voltage source (CCVS) using negative feedback. The desired relationship between the output voltage and the transconductor's output current is given by

$$V_o - I_{Gm}Z_c \quad = \quad 0 \qquad (2)$$

The equation above is written in the form of an error voltage which should equal zero[4]. Negative feedback can be used to drive the output voltage such that the error becomes zero by integrating this error with appropriate polarity and driving the output. The part shown in thick lines in Fig. 4(b) generates the error voltage $V_x = V_o - I_{Gm}Z_c$ computed in Eq. 2. This can be integrated to drive the output using an opamp as shown in Fig. 4(b), similar to the way it is done in Fig. 2. Since the voltage across R_{o1} in Fig. 4(b) is the error voltage V_x (which is zero in an ideal negative feedback system) instead of V_o as was in Fig. 4(a), the part of I_{Gm} that flows through R_{o1} is much smaller than in the latter, and the output voltage V_o is much closer to I_{Gm}/Z_c. The opamp is then substituted with the only opamp that is known so far—the one in Fig. 3.

Fig. 4(c) shows the resulting topology (G_{m2}, C_2, R_{o2} form the opamp used to realize the current controlled voltage source). The dc gain is the product of dc gains of the two stages, confirming that this opamp is better (closer to an ideal integrator) than the single stage opamp in Fig. 3. This is the classic two-stage miller compensated opamp. This approach makes several aspects immediately clear

- The unity gain frequency of the Miller compensated opamp is G_{m1}/C_1, same as that for the single stage opamp in Fig. 3 from which it was derived.

- The opamp used to realize the current controlled voltage source has a unity gain frequency of G_{m2}/C_2. This is also the unity loop gain frequency of the feedback loop used to realize the CCVS. The closed loop transfer function has a pole at this frequency. This will be the non-dominant pole of the miller-compensated opamp and there is a constraint on the minimum value this can take depending on the unity loop gain frequency of the feedback loop realized around the complete opamp. With unity gain feedback around the two-stage opamp, G_{m2}/C_2 has to be sufficiently larger than G_{m1}/C_1.

Analysis can then be used to rigorously demonstrate these aspects, the presence of the right half plane zero, the change in the location of the non-dominant pole when there is a parasitic capacitance at the first stage output.

D. Three stage miller compensated opamp

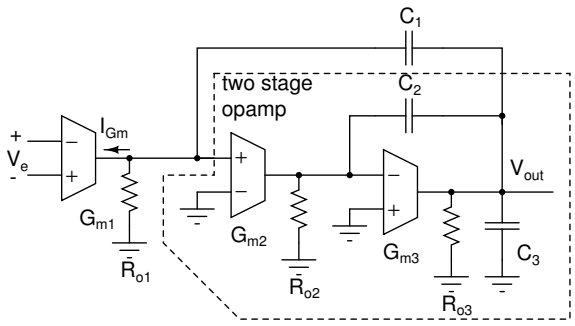

Fig. 5. Three stage opamp: This uses the two stage opamp (G_{m2}, G_{m3}, C_2, C_3) in Fig. 4(c) to realize the CCVS.

Using the single stage opamp in Fig. 3 in the current controlled voltage source in Fig. 4(b) resulted in the two stage opamp in Fig. 4(c). Since the two-stage opamp is better than the single stage opamp, it could be used to improve the CCVS in Fig. 4(b). The motivation to do so is that, the error voltage, i.e., the voltage at the output of G_{m1} will be even smaller, reducing the effect of the output resistance of the first stage even further. The resulting topology is shown in Fig. 5. The two stages of the miller compensated opamp used to implement the CCVS are given subscripts of 2 and 3 respectively. The dc gain is the product of dc gains of the three stages, confirming that this opamp is better than the two stage opamp. As before, the key features are immediately obvious

- The unity gain frequency of the Miller compensated opamp is G_{m1}/C_1, same as that for the single stage opamp in Fig. 3.
- From arguments made in the previous section, G_{m2}/C_2 (the unity gain frequency of the internal two stage opamp) appears as the non-dominant pole of the complete opamp. This has to be sufficiently larger than G_{m1}/C_1 assuming that the complete opamp is in unity feedback. G_{m3}/C_3 in turn has to be sufficiently larger than G_{m2}/C_2.

As before, rigorous analysis can confirm these aspects and reveal the location of the zeros, and pole locations in presence of parasitic capacitances at the first and second stage outputs.

IV. Phase locked loops

Phase locked loops (PLL) are widely used for frequency synthesis, clock generation, and clock and data recovery. Usually ([1], [5], [6], [7]) they are introduced by putting down the block diagram of the analog PLL using a multiplier as the phase detector. Alternatives such as the three state phase detector are then introduced and analyzed in the phase domain. A different approach is taken in [8, Chapter 15] where the PLL is arrived at by attempting to align the phase of two signals of the same frequency. In this paper, we start with the goal of multiplying a frequency, draw the analogy with multiplying (amplifying) a voltage, use the same negative feedback loop with an integrator as the controller (Fig. 1, 2) and arrive at the basic PLL topology.

Just as voltage amplifiers multiply the input voltage, we could try and make frequency amplifiers which "amplify" the input frequency. Fig. 6(a) shows a voltage amplifier in which the output voltage is divided, compared to the input, and driven by an integrator until the error between the two reduces to zero. Fig. 6(b) shows an analogous system in which the output frequency is divided, compared to the input frequency, and driven by an integrator until the error reduces to zero.

The frequency divider in the feedback path can be implemented using digital state machines as long as the division is by an integer. The controller must integrate the frequency error f_e to produce the output frequency f_{out}. A voltage controlled oscillator (VCO) can be used as a source whose frequency can be controlled. Since the control signal of a VCO is a voltage, we need a block which produces a voltage which is proportional to the integral of the frequency error. Fig. 6(c) shows these details.

Fig. 7(a) shows the same block diagram as Fig. 6(c) with the integration moved before error computation. Since the integral of frequency is phase, the combination of integration and computing the error is replaced by a block that computes the phase difference between the input and the feedback signals. This leads us to Fig. 7(b) which has a phase detector, a VCO, and a frequency divider in a negative feedback loop.

Fig. 7(b) is nothing but the classic type-I phase locked loop ([5], [6]). As with opamps, the topology is deduced logically from the desired goal—that of realizing a frequency multiplier using a negative feedback loop.

V. Type-II phase locked loop

The phase locked loop topology that is most popular[5] is the type-II PLL which includes another integrator in order to reduce the phase difference between input and feedback signals to zero. Analysis of the type-I PLL in Fig. 7(b) with practical phase detector implementations and their limitation on phase detection range reveals a (usually unacceptable) trade-off between the lock range and the extent of periodic

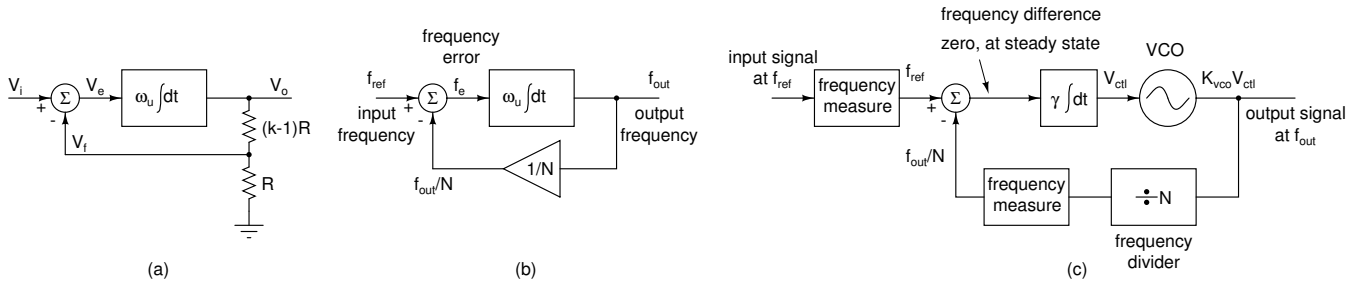

Fig. 6. (a) Voltage amplifier (gain k), (b) Frequency multiplier ("gain" N) analogous to a voltage amplifier, (c) Frequency multiplier showing the essential blocks.

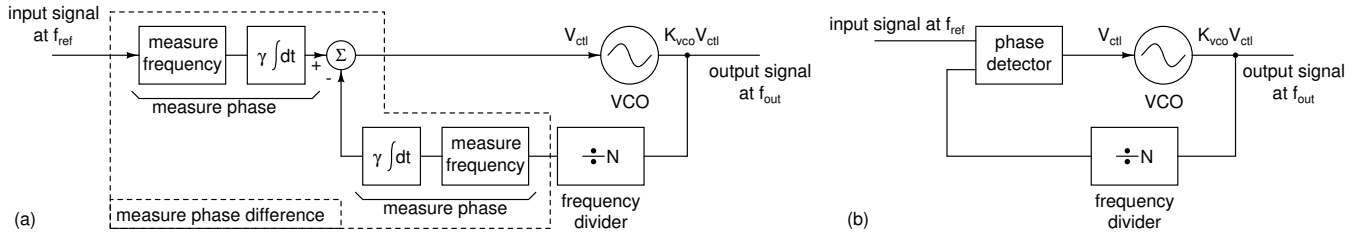

Fig. 7. (a) Integration moved before error computation—the block within dashed lines detects the phase difference between the input and the frequency divided output, (b) Final form of the frequency multiplier—Type I phase locked loop.

phase modulation of the output. An attempt to break this trade-off leads to the conclusion that the phase error between the input and feedback must also be driven to zero, forcing one to use another integrator in the loop to continuously make this adjustment. The topology is derived along the lines of Fig. 1. When stability considerations are added, one arrives at the type-II PLL with a pole-zero loop filter. Owing to lack of space, those details are not presented here.

VI. Suggested Outline of the Course

The development of the opamp topologies can immediately follow the introduction of negative feedback circuits and their stability analysis[3]. All of the opamp topologies in Section III can be synthesized at the level of the controlled sources and their stability can be analyzed. Transistor implementations of those opamps can be taken up afterwards (It is assumed that students have been previously exposed to single transistor amplifiers, the differential pair, and the current mirror). Such an approach separates the somewhat unrelated details of stability of the opamp and biasing details of the transistors. It also makes clear that there can be alternative transistor topologies for the same type of opamp, even if only the most popular alternative is discussed in class. PLLs can be introduced after opamps and opamp circuits. This approach has been successfully used by the author in [9].

VII. Conclusions

The commonly used opamp topologies and the phase locked loop neatly fit into the view that a negative feedback loop drives the error to zero by integrating the error to drive the output. Since all opamps behave as integrators in a certain range of frequencies, it seems natural to start with a perfect integrator and add on other non-ideal features such as the finite dc gain and extra poles and remedies for them. In contrast to this, when one starts with a memoryless opamp, concepts of frequency dependence and compensation are introduced in a rather ad-hoc fashion. Treating the unity (loop) gain frequency as the primary quantity and the dc gain as a secondary one also meshes better with reality. The former is fundamentally related to the power consumption of the circuit whereas the latter can be tailored over a wide range without a direct influence on the power consumption. The phase locked loop can be synthesized in an analogous technique starting with the goal of multiplying the input frequency. In the author's opinion this synthesis based introduction to opamps and PLLs is more intuitive than the traditional approach. The author also feels that students would have a better grasp of the principles of negative feedback since the same concept is repeatedly reinforced while teaching each type of circuit.

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