Introducing Negative Feedback with an Integrator as the Central Element 2012 International Symposium on Circuits and Systems Seoul, Korea

Nagendra Krishnapura

Department of Electrical Engineering Indian Institute of Technology, Madras Chennai, 600036, India

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Motivation

- Intuition before full blown analysis
- Synthesis instead of ad-hoc introduction
- Time domain reasoning/analysis
 - More intuitive
 - Exact analysis difficult for complex systems

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- Frequency domain analysis
 - More abstract
 - Can handle complex systems easily

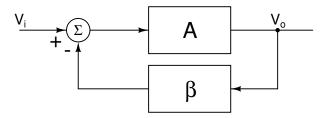
Outline

- Traditional introduction to negative feedback systems
- Integrator as controller in a negative feedback system
- Intuition and analysis in the time domain
- Pedagogical advantages of the proposed introduction

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Conclusions

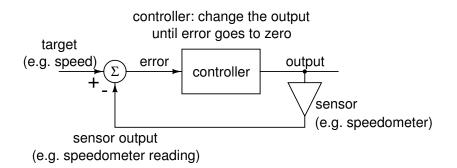
Traditional introduction to negative feedback systems



- Algebraic system—cannot explain evolution over time
- Unstable with arbitrarily small loop delay
 - Ideal delay T_d in the loop \Rightarrow oscillations with a period $2T_d$

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 Real systems have non-zero delay and don't respond instantaneously Intuitive understanding of negative feedback systems

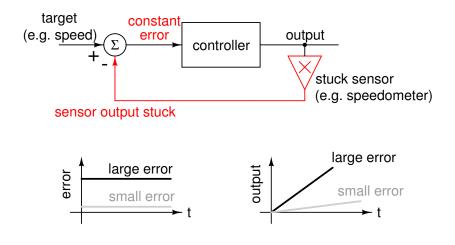


Compare the sensed output to the target (desired output)

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• Continuously change the output until the output approaches the target

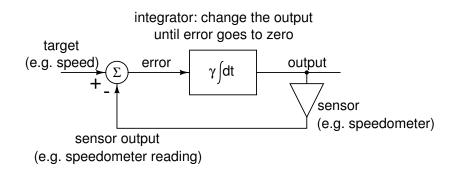
Nature of the controller



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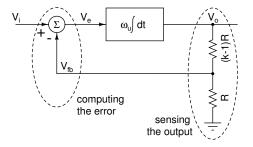
Controller integrates the error

Negative feedback system with an integrator



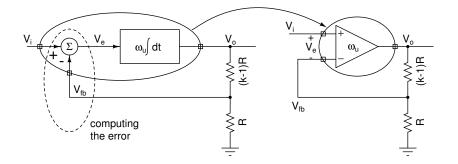
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Negative feedback amplifier

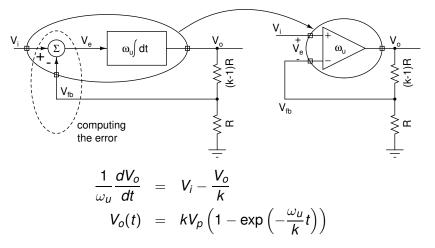


- Need the output V_o to be gain k times the input V_i
- Compare V_o/k to V_i and integrate the error
- Steady state when $V_o = kV_i$ for constant V_i

Opamp for implementing a negative feedback amplifier



Time domain behavior with constant/step inputs



- Time constant k/ω_u
- Asymptotically reaches $V_o = kV_i$ or $V_{fb} = V_i$

Relation to frequency domain analysis

Loop gain
$$L(s) = \frac{\omega_u}{ks} = \frac{\omega_{u,loop}}{s}$$

Frequency domain:

- Unity loop gain frequency ω_{u,loop}
- Significant negative feedback up to ω_{u,loop} ⇒ nearly ideal behavior up to ω_{u,loop} (Closed loop Bandwidth)

$$au_{loop} = rac{1}{\omega_{u,loop}}$$

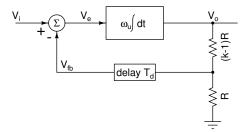
Time domain:

• Unit step response of the loop gain

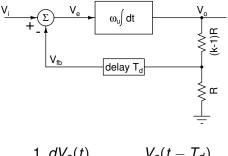
$$= t/(1/\omega_{u,loop}) = t/ au_{loop}$$

• Closed loop response time constant = $1/\omega_{u,loop} = \tau_{loop}$

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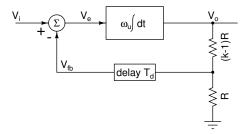


- Reacts to past output \Rightarrow Don't know target has been reached
- Possibility of overshoots or unbounded oscillation
- Unaffected if the integrator's output doesn't change significantly over T_d



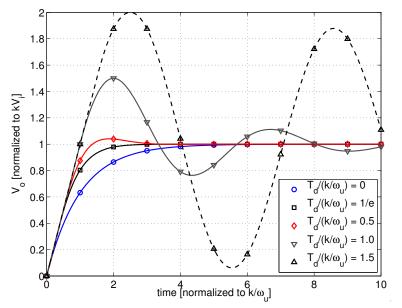
$$\frac{1}{\omega_u}\frac{dV_o(t)}{dt} = V_i - \frac{V_o(t - T_d)}{k}$$

Delay differential equation



- *T_d*/*τ_{loop}* ≤ 1/*e*(= 0.367): No overshoot
- 1/e < T_d/τ_{loop} < π/2: Overshoot + ringing
- $\pi/2 < T_d/\tau_{loop}$: Unstable

In practice we need a "well behaved" response (limited overshoot)



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% Overshoot	0	1	2	4	10	20
T_d/ au_{loop}	,	0.445	0.465	0.5	0.585	0.695
	(0.367)					

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Fixing the stability problem in presence of delay

- Stability governed by the ratio of T_d to τ_{loop}
- Reduce *T_d*: Faster circuit/technology
- Increase $\tau_{loop} \Rightarrow$ Decrease $\omega_{u,loop}$: Slower integration

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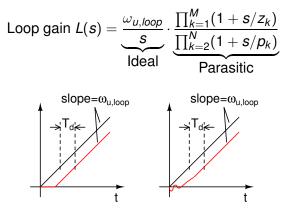
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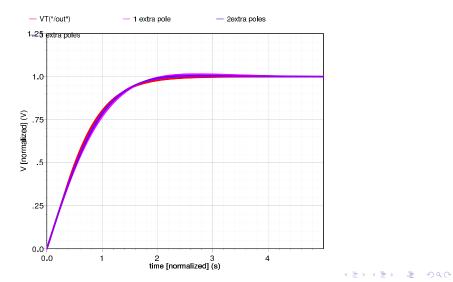
Delays in circuit implementation—parasitic poles and zeros



Unit step response of L(s) is a ramp of slope $\omega_{u,loop}$ (same as ideal) with a delay $T_d = \sum_{k=1}^N 1/p_k - \sum_{k=1}^M 1/z_k$

Closed loop response with eqiuvalent delay

Transient Response



Advantages of this formulation

• Synthesis from common experience of negative feedback based adjustment in the time domain

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- Intuition and key results obtained from time domain reasoning
 - Exponential settling
 - Possibility of ringing, overshoot, and instability

Advantages of this formulation

- Traditional viewpoint
 - Memoryless amplifier (loop gain) in the ideal case
 - Frequency dependence as non-ideal feature
- Proposed viewpoint
 - Integrator in the ideal case (∞ dc gain)
 - Finite dc gain due to non-ideal implementation
- $\omega_{u,loop}$ more fundamental characteristic of the negative feedback loop than dc loop gain
 - Increasing $\omega_{u,loop}$ requires higher power
 - Increasing dc loop gain indirectly influences power
- Loop gain of all feedback systems has integrator-like behavior over some frequency range
 - Nyquist plot should enter the unity circle near the negative imaginary axis
 - Bode plot should have -20 dB/decade slope near the unity gain frequency

Advantages of this formulation

- Clear why fastest negative feedback systems are slower than fastest open loop systems
- Leads to commonly used opamp and phase locked loop topologies

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Suggested course outline

- Negative feedback with integrating controller
- Opamp for computing and integrating error
- Time domain analysis with delay
- Laplace transform stability analysis, Nyquist criteria

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- Relation to time domain analysis results
- Synthesis of opamp, PLL topologies

References

Adel S. Sedra and Kenneth C. Smith, Microelectronic Circuits, 6th ed., Oxford University Press 2009.
Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, <i>Analysis and Design of Analog Integrated Circuits</i> , 5th ed., Wiley 2009.
Nagendra Krishnapura, "Synthesis Based Introduction to Opamps and Phase Locked Loops," <i>Proc. 2012 IEEE ISCAS</i> , May 2012.
Karl J. Astrom and Richard M. Murray, "Feedback Systems: An Introduction for Scientists and Engineers," Available: http://www.cds.caltech.edu/~murray/amwiki/index.php/Main_Page
Barrie Gilbert, "Opamp myths," Available: http://pe2bz.philpem.me.uk/ Parts-Active/IC-Analog/OpAmps/OpAmpMyths/c007-OpAmpMyths.htm
Hal Smith, An Introduction to Delay Differential Equations with Applications to the Life Sciences, 1st ed., Springer 2010.
Nagendra Krishnapura, "EE5390: Analog Integrated Circuit Design," Available: http://www.ee.iitm.ac.in/~nagendra/videolectures