Introducing Negative Feedback with an Integrator as the Central Element

Nagendra Krishnapura
Department of Electrical Engineering, Indian Institute of Technology, Madras, Chennai 600 036, India

***Abstract*— Negative feedback is introduced using an integrator as the central element by making intuitive connections with the way we sense the difference between desired and actual values and continuously adjust the latter so that it reaches the desired value. In contrast to the traditional use of a memoryless high gain amplifier as the central element, this approach makes it clear right from the beginning that negative feedback circuits take time to respond (have a finite bandwidth), that some excess delay can be tolerated, while larger excess delays lead to ringing and eventually instability, and that negative feedback circuits can be stabilized by slowing them down. Time domain intuition and analysis lead to key conclusions regarding the stability margin of negative feedback circuits. This approach complements the conventional frequency domain approach by serving as an introduction that anticipates the results that are derived by the latter. The presented approach also lends itself better to synthesis of key negative feedback blocks such as opamps and the phase locked loop.**

I. Motivation

A graduate course in analog integrated circuit design necessarily includes a discussion of negative feedback circuits and stability, design of opamps, and their frequency compensation schemes. This paper outlines a scheme for development of these topics which differs from the traditional approach taken in classrooms and standard textbooks (e.g. [1], [2]). The reasons for taking this approach are as follows:

- Time domain reasoning is intuitive, though exact analysis with arbitrary signals is usually difficult or even impossible. Frequency domain analysis is easier, but is at a higher level of abstraction. Therefore, it is often best to appeal to students' natural intuition in the time domain in the initial explanations, get them to anticipate the results, and move on to the frequency domain for exact calculations using the Laplace transform.
- Students grasp the topics better if they are told why the system is the way it is, rather than simply showing it to them and analyzing it.

None of the results in this paper is new. They have been known and taught for decades, usually using the traditional frequency domain approach. What is presented here is an alternative viewpoint towards negative feedback circuits which the author believes is more intuitive and more efficient in conveying the key concepts in the classroom. Key results about negative feedback systems can be derived from this time domain approach which can hence serve as an introduction to the subject. As shows later in this paper, this method makes it clear right from the beginning that negative feedback circuits take time to respond (i.e. they have a non-zero time constant or a finite bandwidth), that some delay can be tolerated while larger delays lead to ringing and eventually instability, that negative feedback circuits can be stabilized by slowing them down, and that negative feedback circuits tend to be slower than open loop circuits. Frequency domain approach, which is used for exact analysis of complex circuits can follow this introduction. The results derived from the latter for specific circuits can be connected to the earlier general conclusions drawn from the time domain analysis. The presented approach also lends itself better to synthesis of key negative feedback blocks such as the phase locked loop[3].

The next section outlines the traditional classroom introduction to negative feedback circuits and discusses certain shortcomings in it. Section III deduces the nature of the negative feedback system by drawing analogies with manual adjustment of quantities in everyday life. It is seen that the central element of the negative feedback system is an integrator. The prototype negative feedback amplifier is discussed in Section IV. The opamp is introduced as a convenient building block of negative feedback systems in Section V. Section VI briefly discusses the step response of the amplifier in the ideal case. The behavior of the system with an additional delay in the loop is discussed intuitively in Section VII and results of its analysis are shown in Section VIII. The suggested flow of topics in the classroom and connections between the time domain analysis presented here and the traditional frequency domain viewpoint are given in Section IX. Section X concludes the paper.

II. Traditional Introduction to Negative Feedback Circuits

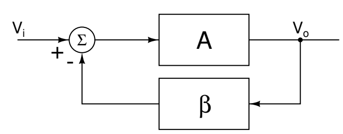

Fig. 1. Block diagram traditionally used to introduce negative feedback circuits.

Traditionally ([1], [2]) negative feedback circuits are introduced by putting showing the classical block diagram in Fig. 1, analyzing it, and showing that the closed loop gain

This work was supported in part by the Special Manpower Development Programme in VLSI, Ministry of Information Technology, Government of India.

V_o/V_i approaches $1/\beta$ when $A\beta \gg 1$. Replacing A by an opamp and β by a resistive divider results in the classic non-inverting amplifier topology.

The author feels that this approach has some shortcomings when used in the classroom—mainly in that it leaves certain questions unanswered until later when complete analysis is carried out including the details of the circuits. No reason is given for why the topology is the way it is in Fig. 1. Many times, the negative feedback action is described by assuming that there is a non zero error voltage V_e and stating that the feedback appears in the opposite polarity that somehow reduces V_e. But, the circuit as it stands is algebraic and does not allow an error voltage V_e that evolves over time (for a constant input). Furthermore, if a delay is added to the loop as shown in Fig. 1, *the system is unstable for arbitrarily small values of delay*. This contradicts our intuition which feels that the system should remain stable for small enough delays. Finally, no real negative feedback system has a frequency independent behavior implied in Fig. 1, whereas a large class of them has a first order $(1/s)$ frequency dependence in some significant range of frequencies[1]. Therefore it seems fair to treat the first order dependence, or an integrator-like behavior as an essential feature and not as a shortcoming to be coped with.

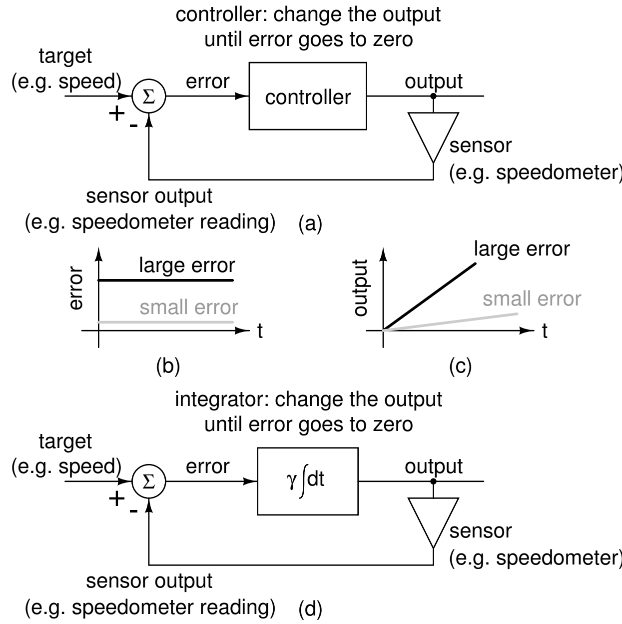

Fig. 2. (a) Conceptual diagram of a negative feedback system, (b) Error when the sensor is stuck, (c) Controller output when the sensor is stuck, (d) Negative feedback system using an integrator as controller (γ is a constant with the appropriate dimensions).

III. Integrator as the Controller in a Negative Feedback System

The intuitive notion of negative feedback as a system which senses the output, compares it to the desired value, and *continuously drives the output until it reaches the desired value* is very easy to explain to students. For example, while driving a car or listening to a radio, one senses the difference between desired and actual speed or volume level and *continuously adjusts* the latter until the desired values are attained. Fig. 2(a) depicts this idea. It is emphasized here that one *does not know* how to set the output instantaneously to the correct value as implied by Fig. 1, but the it is the process of continuous sensing and adjustment that drives the output to the correct value. Also, intuitively, if the sensed output is very close to the desired value, one drives the output gently so that it changes slowly (e.g. the car is gently accelerated) whereas if the sensed output is far from the desired value, it is driven strongly so that output changes more rapidly.

The problem now in hand is to figure out the nature of the controller in Fig. 2(a). This can be done most easily by assuming that the output of the sensor is stuck. In this case the error input to the controller is a constant (Fig. 2(b)) and the output (Fig. 2(c)) ramps up continuously. This is analogous to continuously accelerating and increasing the speed when the speedometer is stuck. For a smaller error, the output would up more slowly. The rate of change of the controller's output is proportional to the error between the sensed and the desired output. From this, it can be deduced that the desired form of the driver in Fig. 2(a) is an integrator. The output of the controller is the integral of its input (error between the desired and actual outputs) over time. Fig. 2(d) shows the feedback system using an integrator as the controller.

Fig. 2(a) is the classical block diagram used in control systems textbooks to introduce the concept of feedback control (e.g [4, Fig. 1.13]). What is being pointed out in this paper is that the idea of *continuous adjustment* leads to the controller being an integrator (Fig. 2(d)) and that the system with an integrator results in a smoother introduction to negative feedback in the classroom than the one with a memoryless amplifier (Fig. 1).

IV. The Negative Feedback Amplifier

In circuit design, we are in particular interested in negative feedback amplifiers. An amplifier of gain k with an output voltage V_o and an input voltage V_i (assumed to be constant with time) follows the relationship $V_o = kV_i$. For this to be implemented with negative feedback, we define the desired value to be V_i and the sensed value to be V_o/k, so that, when the sensed value is driven to be equal to the desired value, the relationship above holds true. Translating Fig. 2(c) with these definitions yields the prototype negative feedback amplifier in Fig. 3(a). The sensor is a resistive voltage divider $1/k$. By inspection, it is clear that, steady state occurs only when $V_o = kV_i$ and any other value of V_o results in a continuous change in the output.

[1] Around the unity gain frequency, the Bode plot of the loop gain of systems with a reasonable phase margin has a -20 dB/decade slope. On the Nyquist plot, this corresponds to the loop gain contour crossing the unit circle in the third quadrant, closer to the negative imaginary axis. Therefore, around the unity gain frequency, the loop gain should show integrator-like behavior, though it may deviate from it at higher or lower frequencies. Frequency compensation for stabilizing negative feedback loops forces this behavior.

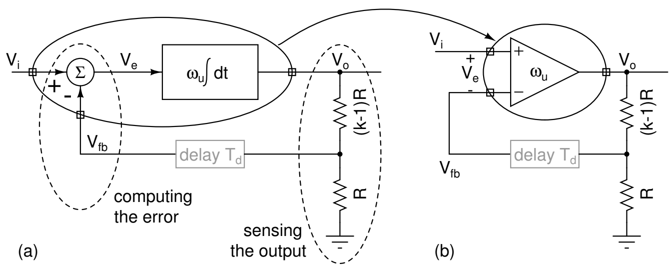

Fig. 3. (a) Negative feedback amplifier using an integrator. ω_u is a constant with dimensions of frequency. Assume that the delay T_d is zero until section VIII. (b) Opamp as a combination of error computation and integration. The resulting amplifier. is the classic non-inverting amplifier.

V. Opamp as Error Integrator

The essential operations in a negative feedback amplifier are: (a) Taking the difference between the desired and the sensed values to compute the error and (b) Integrating the error. A circuit realizing the combination of these functions would be a very useful building block, and is nothing but the ubiquitous opamp (Fig. 3(b)). ω_u is a parameter of the opamp. It is the slope of the output for a unit step input. It is also the *unity gain frequency* of the opamp's magnitude response[2].

VI. Step Response of the Negative Feedback Amplifier

When an step of size V_p is applied as the input V_i to the amplifier in Fig. 3, assuming a zero initial condition, the error voltage V_e equals the input step at $t = 0+$. The output ramps up at a rate $\omega_u V_p$, and the feedback signal V_{fb} ramps up at a rate $(\omega_u/k)V_p$. As V_{fb} increases, V_e reduces, and the rate of increase of the V_o (and V_{fb}) reduces. The system has a time constant (k/ω_u) asymptotically reaches steady state with $V_o = kV_i$ (and $V_{fb} = V_i$). This is the well known behavior is captured by the differential equation and its solution (for a step V_p) given below

$$\frac{1}{\omega_u}\frac{dV_o}{dt} = V_i - \frac{V_o}{k} \quad (1)$$

$$V_o(t) = kV_p\left(1 - e^{-\frac{\omega_u}{k}t}\right) \quad (2)$$

VII. Behavior with Delay in the Loop—Intuition

Thus far, the description of the negative feedback amplifier (Fig. 3) implied that the actual output was sensed instantaneously and the controller reacts instantaneously to the resulting error between the desired and the sensed value. In practice, there are delays in the loop. The qualitative effects are easy enough to imagine. Again, assume a zero initial condition for the integrator and a step input of amplitude V_p. Let there be a non-zero delay T_d in the feedback path. After the step is applied, for a duration of T_d, the feedback signal V_{fb} remains at zero and the error V_e remains at V_p. In the delay-free case, the feedback signal would have started to ramp up from $t = 0+$ at a rate $(\omega_u/k)V_p$. For a small delay ($T_d \ll k/\omega_u$), the delay-free feedback at $t = T_d$ would be approximately $(\omega_u/k)T_d V_p$ and the corresponding error would be $V_p - (\omega_u/k)T_d V_p \approx V_p$. Since the difference in the error signal between the delay-free and delayed feedback cases is small, one would expect that, for $T_d \ll (k/\omega_u)$, the behavior would be similar to the delay-free case.

For larger delays, say $T_d = (k/\omega_u)$, during the period up to T_d, the output builds up to kV_p, the desired steady state output. Since V_e starts to decrease from its initial value of V_p only after $t = T_d$, the output overshoots the desired value and continues to ramp up due to the positive value of V_e. The error voltage V_e becomes negative and causes V_o to decrease only when the delayed feedback V_{fb} crosses V_p at $t = 2T_d$. The output V_o then crosses kV_p in the other direction, but there is a delay of T_d before this reversal is fed back to V_e. The output oscillates around the desired steady state of kV_p.

From this, one can deduce that, if T_d is so large that V_o overshoots to twice the steady state value of kV_p or higher, the system would never recover, since the overshoot in each direction becomes successively higher. Similarly, if the overshoot is only a small fraction of the steady state value of kV_p, the overshoots become successively smaller and eventually die out.

As described earlier, the difference between the feedback signals in the delayed and delay-free cases is $(\omega_u/k)T_d V_p$. To reduce this difference, one must either (a) reduce the delay(if possible), or (b) reduce (ω_u/k) (the rate at which the feedback signal ramps up initially), i.e. "slow down" the integration such that not much change occurs over the duration of the delay. These two points capture the essence of techniques for stabilizing negative feedback systems. The second point above also illustrates that there is a technological limit to speed or bandwidth of a negative feedback system because of the minimum delay that is realizable in the particular technology. As mentioned in the introduction, appreciating these points before diving into the analysis provides a much better motivation to do the latter.

VIII. Behavior with Delay in the Loop—Analysis

With a non-zero delay in Fig. 3(a), the differential equation governing the amplifier is

$$\frac{1}{\omega_u}\frac{dV_o(t)}{dt} = V_i - \frac{V_o(t-T_d)}{k} \quad (3)$$

This is a delay differential equation describing delayed feedback[6]. This equation can be solved in the time domain with a bit of algebra and familiarity with the ordinary differential equation in Eq. 1. Due to lack of space, the analysis is not shown here. The essential features of the solution are (*e* is the natural exponent):

- For $T_d < 1/e \cdot k/\omega_u$ the step response shows no overshoot. This is analogous to overdamped response in a second order system.

[2]That an integrator is better model for an opamp than a memoryless amplifier is pointed out in [5]. The discussions in this paper show that the integrator is not only a model for the opamp, but is the natural outcome of synthesizing a negative feedback system from our intuitive notion of feedback as continuous adjustment of the output in a direction that reduces the error.

- For $T_d = 1/e \cdot k/\omega_u$ the step response shows no overshoot. This is analogous to critically damped response in a second order system. $T_d = 1/e \cdot k/\omega_u$ is the highest delay possible without resulting in overshoots.
- For $1/e \cdot k/\omega_u < T_d < \pi/2 \cdot k/\omega_u$ the step response rings before settling. This is analogous to underdamped response in a second order system.
- For $\pi/2 \cdot k/\omega_u < T_d$ the step response blows up and the amplifier is unstable.

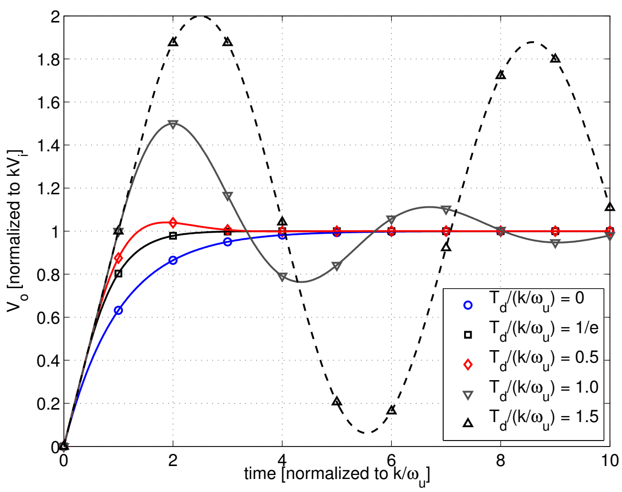

Fig. 4. Transient response of Fig. 3(a) for different values of delay with a step input V_i and zero initial conditions.

The above results confirm the intuitive conclusions in the previous section. Fig. 4 shows the step responses for different values of delay less than the instability limit $\pi/2 \cdot k/\omega_u$. Table I shows the delay T_d normalized to the amplifier time constant k/ω_u for different values of overshoot. The delay that can be tolerated is constrained by the amount of acceptable overshoot.

TABLE I
DELAY FOR A GIVEN OVERSHOOT

% Overshoot	1	2	4	10	20
$T_d/(k/\omega_u)$	0.445	0.465	0.5	0.585	0.695

IX. DEVELOPMENT OF TOPICS IN THE CLASSROOM

The discussion of negative feedback can start with the development of the negative feedback amplifier and its time domain analysis described in Sections III to VIII. The behavior of the system can be visualized intuitively in the time domain before it is mathematically derived. Frequency domain analysis of Fig. 3(a) leads to connections between the unity loop gain frequency and the time constant and bandwidth of the closed loop system.

This can be followed by an attempt to synthesize the integrator using a voltage controlled current source and a capacitor. This leads naturally to the single stage opamp. The effect of finite output resistance of a real current source leads to discussion of finite dc gain and consequent steady state error. Attempting to improve the dc gain in order to reduce the steady state error leads to more complicated opamp topologies such as cascode and multi-stage opamps.

Parasitic effects in the circuit such as the parasitic capacitance C_p at the output of the resistive divider leads to discussion of the effect of parasitic poles in the negative feedback amplifier. The unit step response of the loop gain in Fig. 3(a) is a ramp of slope of ω_u/k. With parasitic poles $p_{2,3,\ldots,N}$ in the loop, the step response of the loop gain is a ramp with a delay $\sum_{m=2}^{N} 1/p_m$ after the transients die out. The constraint on the delay T_d (as a fraction of k/ω_u) for the desired overshoot level can be translated into a constraint on the location of the parasitic poles in relation to ω_u/k. These results can be connected to the ones obtained from conventional frequency domain analysis in terms of phase margin. Salient ideas about stabilizing negative feedback loops and consequent limits (last paragraph about Section VII) can be reinforced during these discussions.

A useful and frequently used concept is that of the ideal opamp which can be discussed soon after Fig. 3(a) is introduced. In the memoryless model of the feedback amplifier in Fig. 1, the forward amplifier turns into the ideal opamp in the limit $A \rightarrow \infty$. When the opamp is modeled as an integrator, it is by definition ideal for dc, owing to the infinite dc gain of the integrator. It can also be made ideal for all frequencies by taking the limit $\omega_u \rightarrow \infty$.

X. CONCLUSIONS

Sensing the error between the desired and actual values and continuous adjustment of the latter to reduce the error leads to the integrator being the central element of a negative feedback amplifier. Time domain analysis of this system provides key general results about the behavior of negative feedback systems. Attempts to realize the integrator naturally lead to opamp topologies. The author has used this approach successfully in [7] and feels that student interest was better maintained due to (a) synthetic development of the negative feedback amplifier and constituent circuits, and (b) the high level overview of key results provided by time domain analysis before rigorous analysis of the same for specific cases in the frequency domain.

REFERENCES

[1] Adel S. Sedra and Kenneth C. Smith, *Microelectronic Circuits*, 6th ed., Oxford University Press 2009.
[2] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed., Wiley 2009.
[3] Nagendra Krishnapura, "Synthesis Based Introduction to Opamps and Phase Locked Loops," *Proc. 2012 IEEE ISCAS*, May 2012.
[4] Karl J. Astrom and Richard M. Murray, "Feedback Systems: An Introduction for Scientists and Engineers," Available: http://www.cds.caltech.edu/~murray/amwiki/index.php/Main_Page
[5] Barrie Gilbert, "Opamp myths," Available: http://pe2bz.philpem.me.uk/Parts-Active/IC-Analog/OpAmps/OpAmpMyths/c007-OpAmpMyths.htm
[6] Hal Smith, *An Introduction to Delay Differential Equations with Applications to the Life Sciences*, 1st ed., Springer 2010.
[7] Nagendra Krishnapura, "EE5390: Analog Integrated Circuit Design," Available: http://www.ee.iitm.ac.in/~nagendra/videolectures