Efficient Determination of Feedback DAC Errors for Digital Correction in ΔΣ A/D converters

2010 International Symposium on Circuits and Systems, Paris, France

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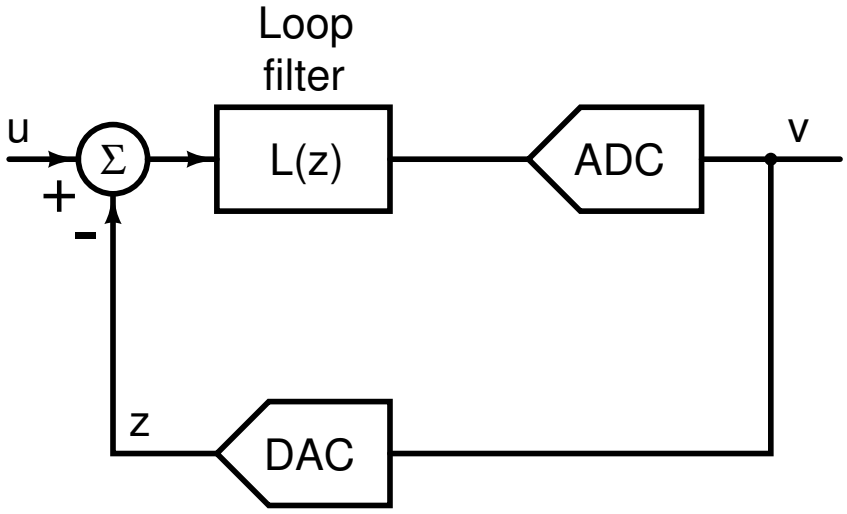
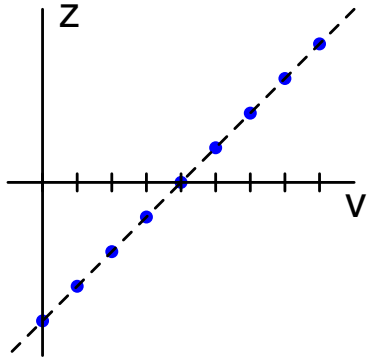
31 May 2010

Outline

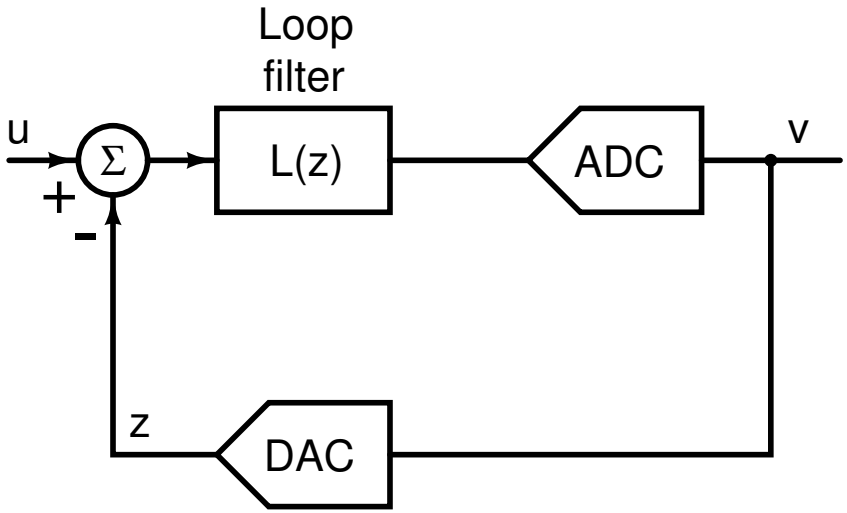
- Motivation
- DAC realizations
- Element usage in idle channel
- Determining correction values
- Simulation results
- Conclusions

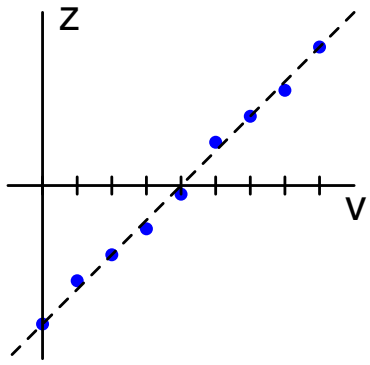
Multi bit ΔΣ ADC



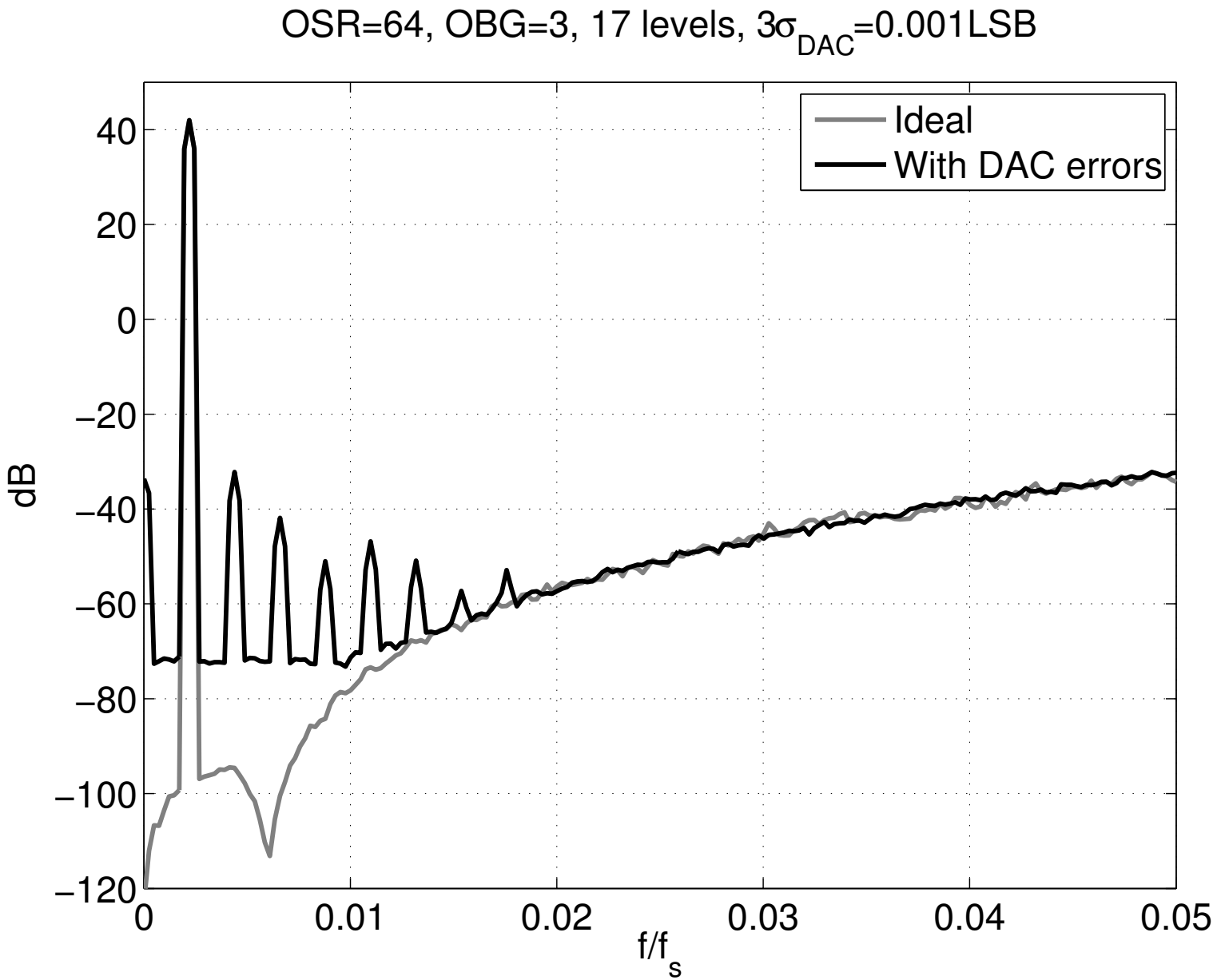


Multi bit ΔΣ ADC—DAC nonlinearity

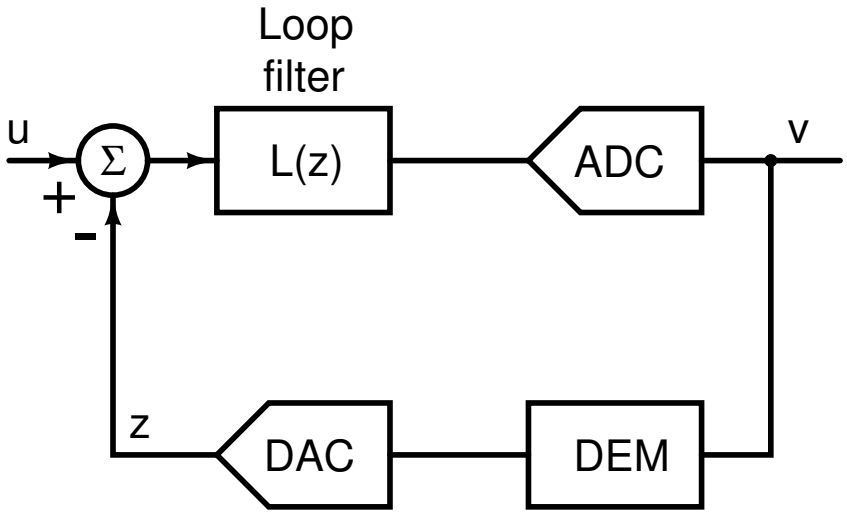


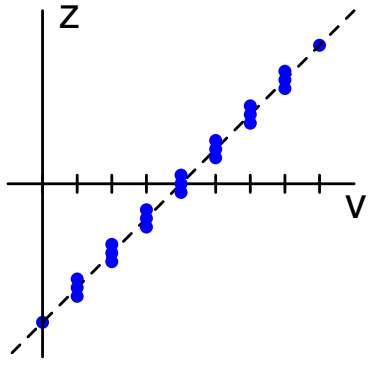


Effect of DAC nonlinearity



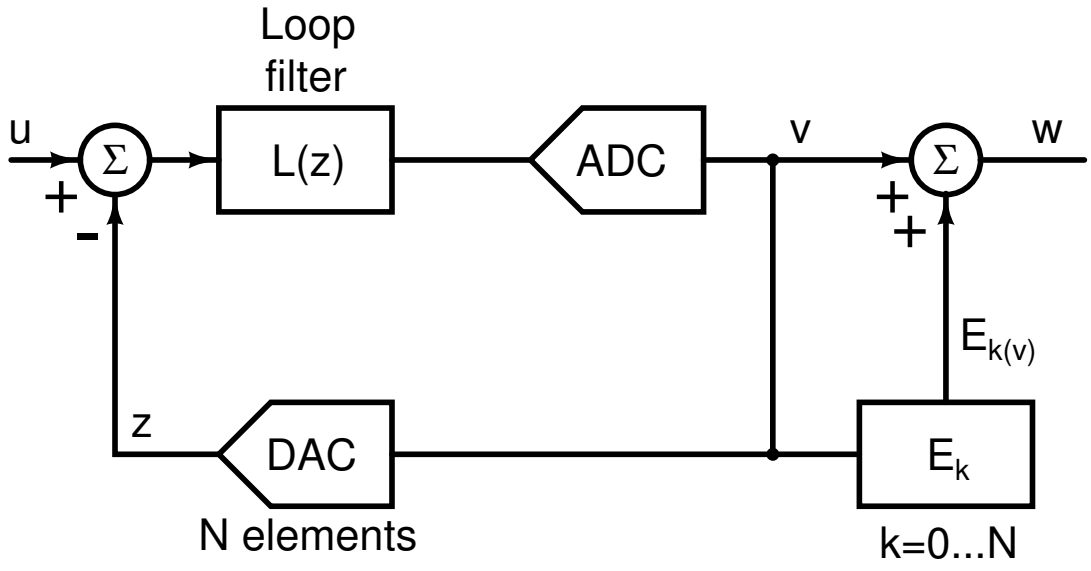
Mitigating DAC nonlinearity—Dynamic element matching





- Excess loop delay
- Tones for low OSR
- Increased DAC dynamic nonlinearity

Mitigating DAC nonlinearity—Digital correction

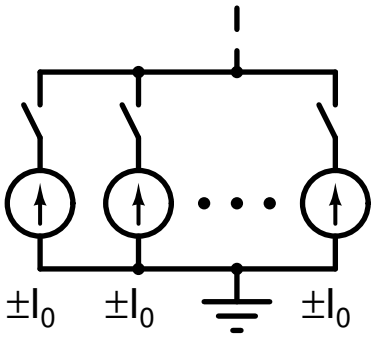


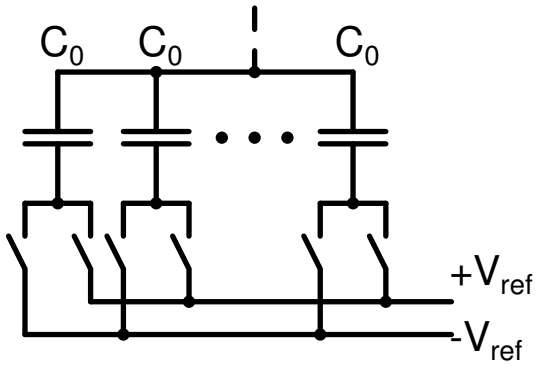
- Reconfigure the loop as a 1 bit $\Delta\Sigma$ modulator and measure all DAC error values E_k

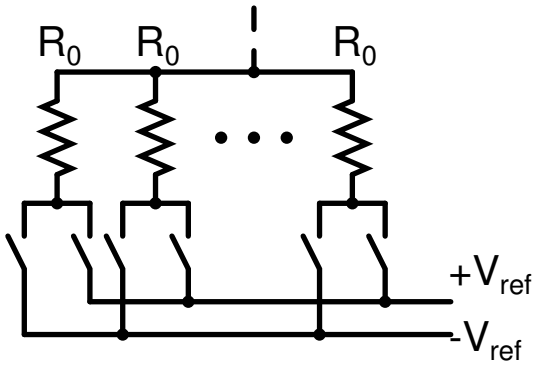
J. Silva, U. Moon, J. Steensgaard, and G. C. Temes, "Wideband low-distortion delta-sigma ADC topology,"

Electronics Letters, vol. 37, no. 12, 2001.

Multi bit feedback DAC-generic representation



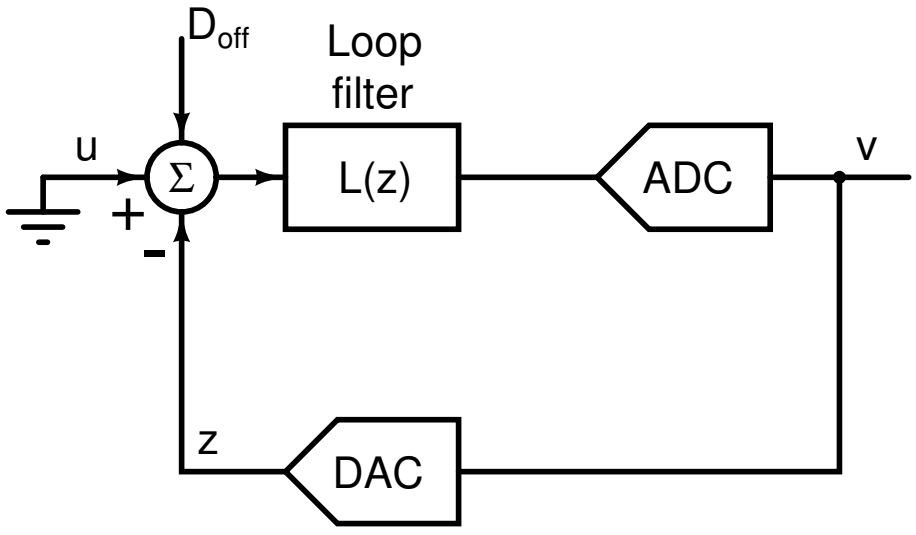


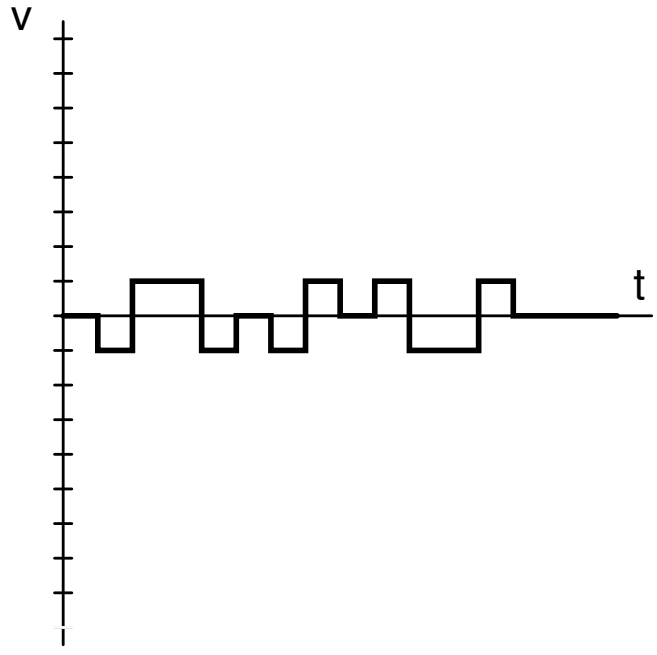


$$
\begin{aligned}
z_0 &= -D_1 - D_2 - D_3 - \ldots - D_N \\
z_1 &= +D_1 - D_2 - D_3 - \ldots - D_N \\
&\vdots \\
z_N &= +D_1 + D_2 + D_3 + \ldots + D_N
\end{aligned}
$$

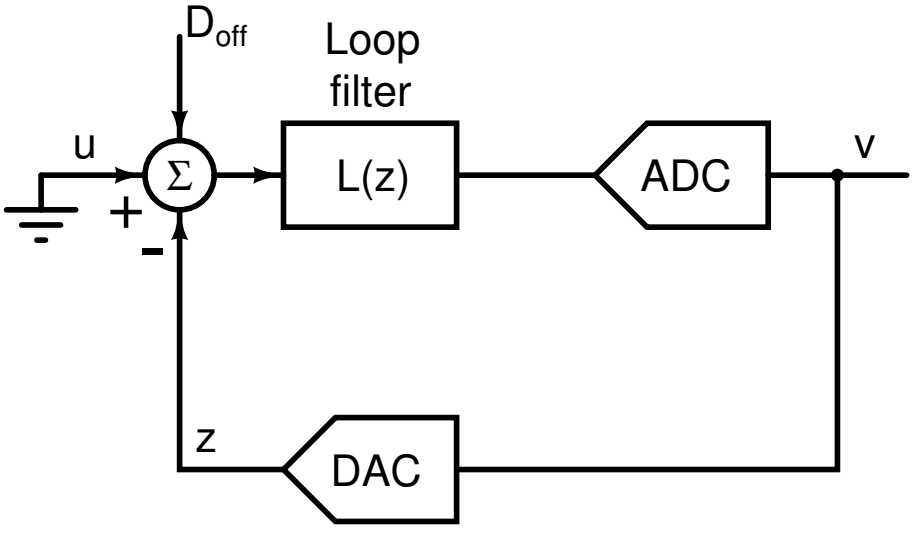
- D_0: I_0, $C_0 V_{ref}$, V_{ref}/R_0
- $D_k = D_0(1 + \delta_k)$
- Assume $D_0 = 1$: Nominal $LSB = 2$, max $= +N$, min $= -N$

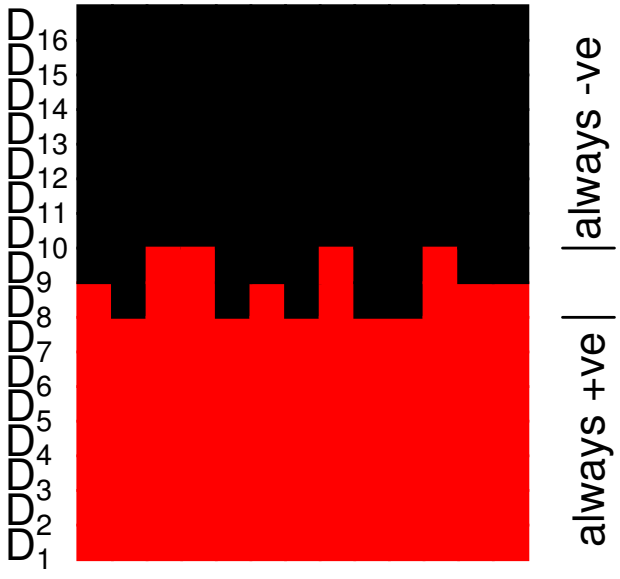
Multi bit ΔΣ modulator—Idle channel



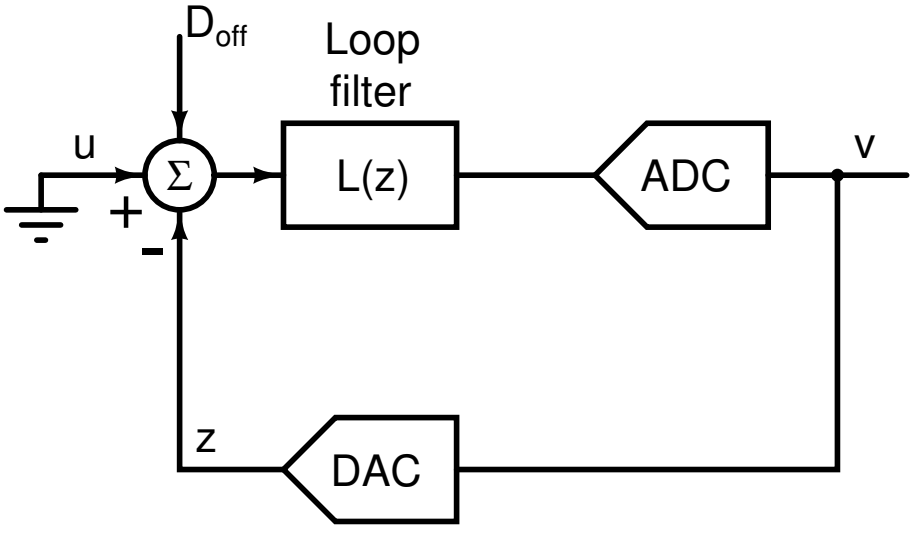


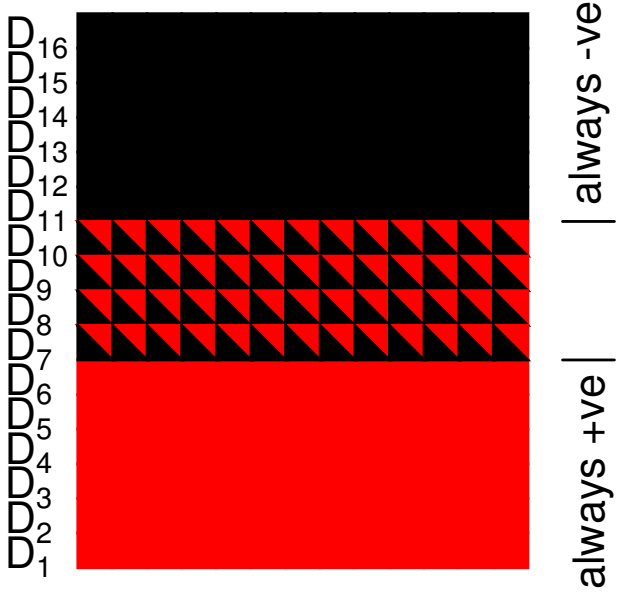
Multi bit ΔΣ modulator—Idle channel



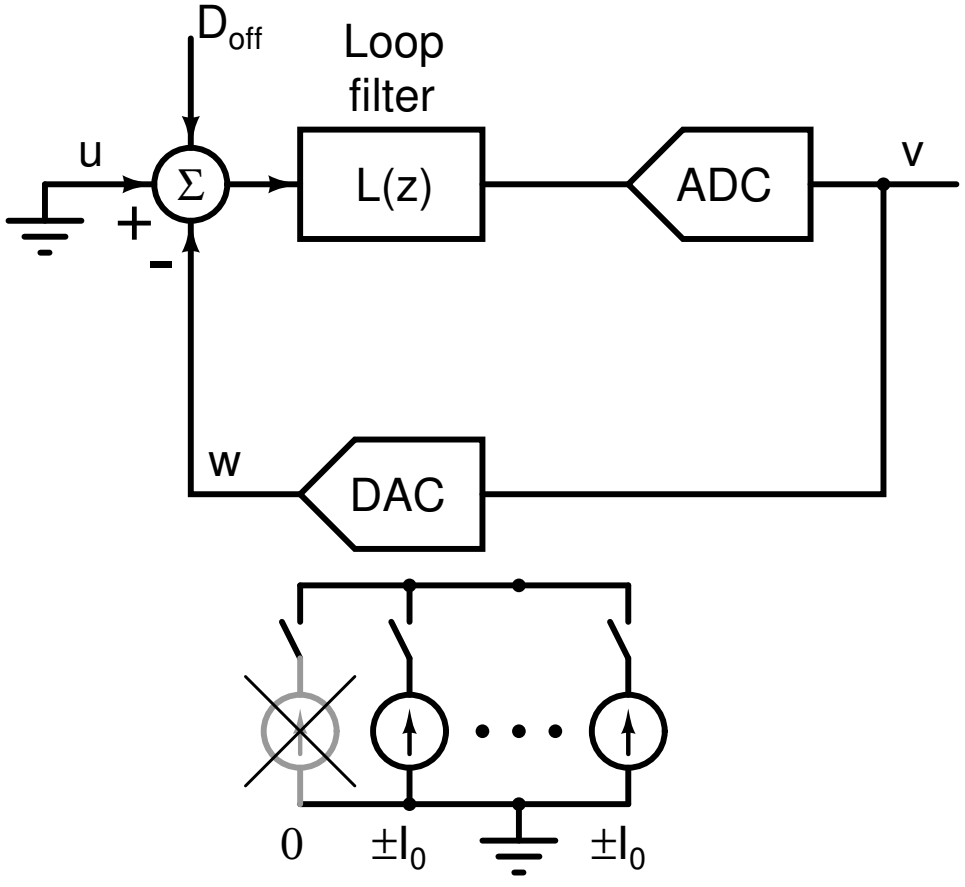


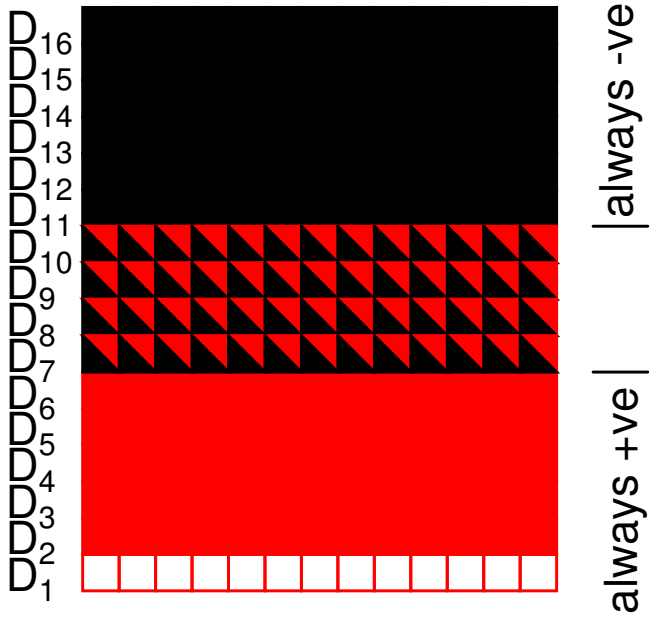
Multi bit ΔΣ modulator—Idle channel





D_1 *removed from the DAC*





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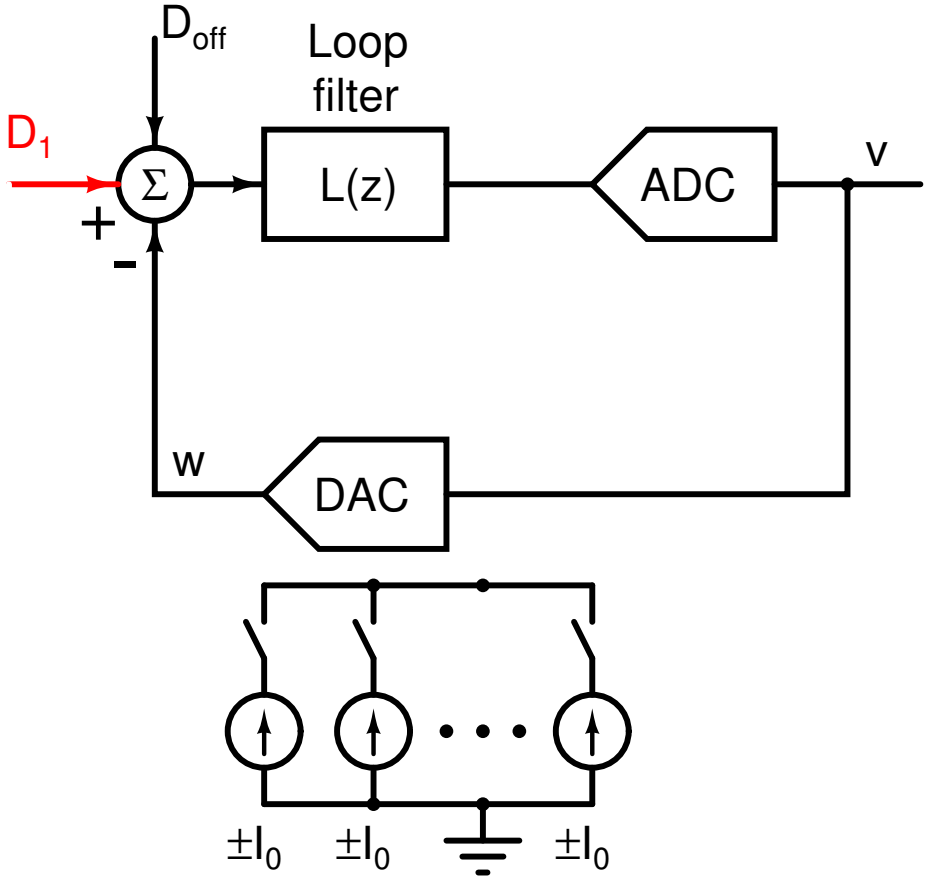
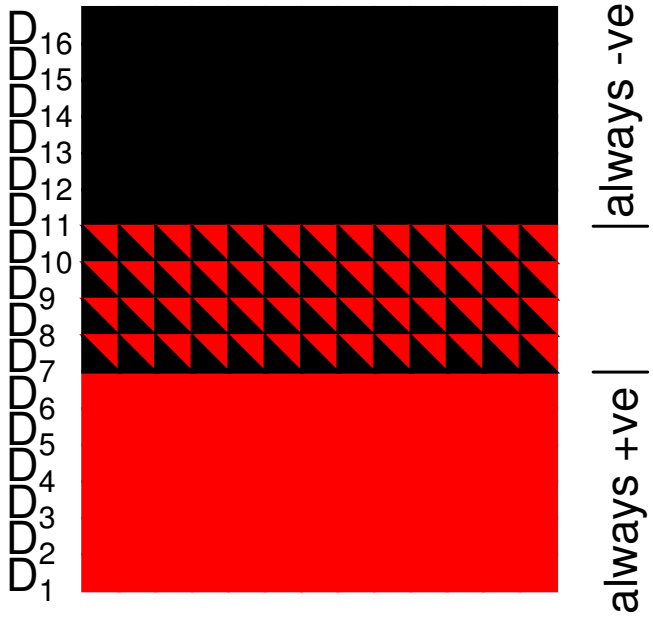
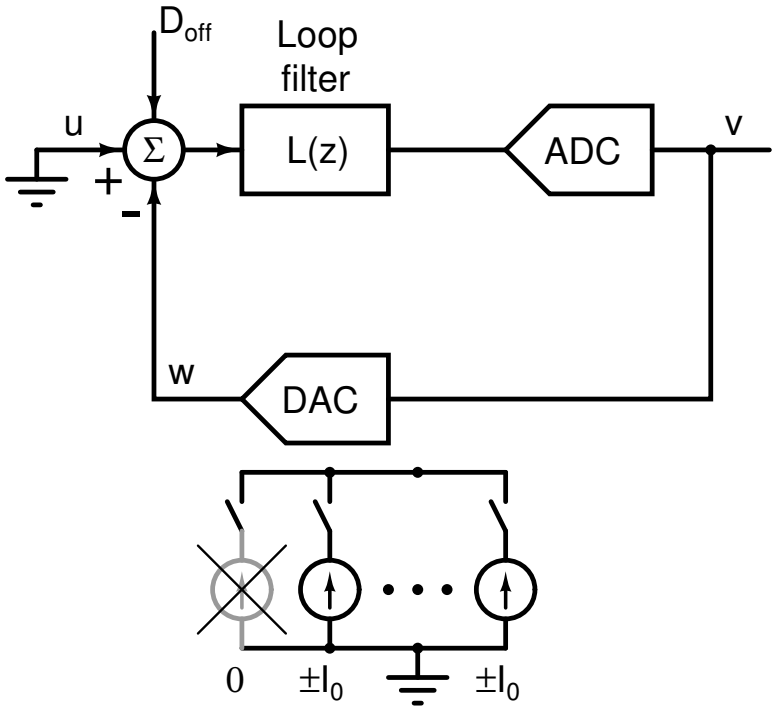
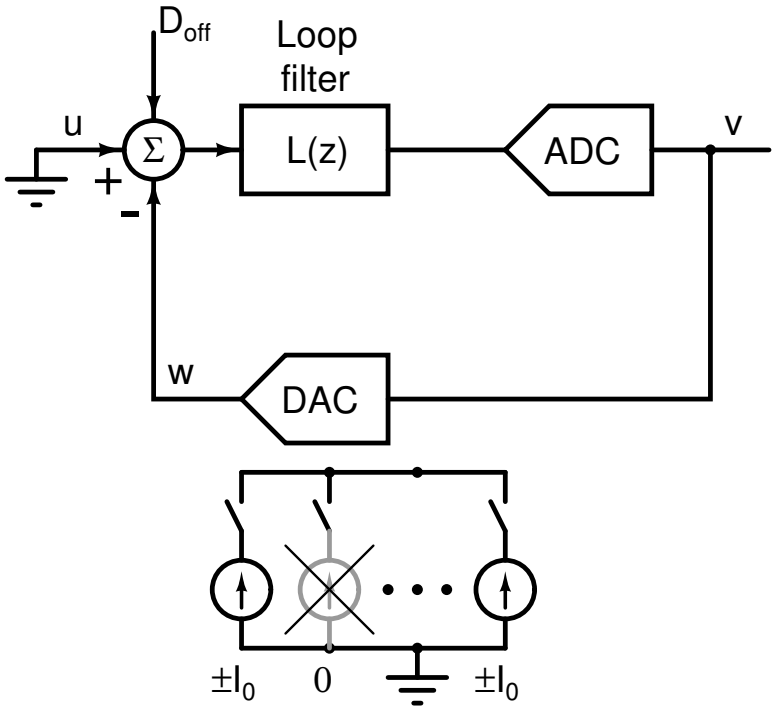




Estimating DAC errors



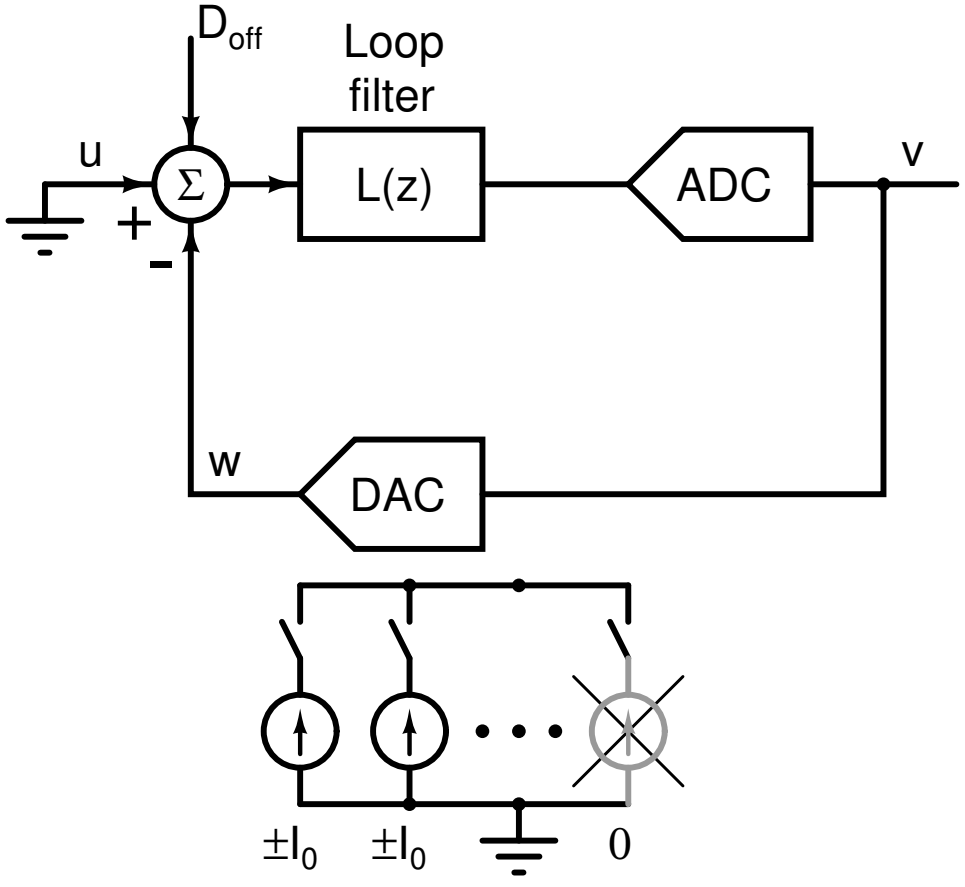
- Remove D_1 from the DAC
- $V_{av,1} = D_1 + D_{off} + NL|_{D_1+D_{off}}$

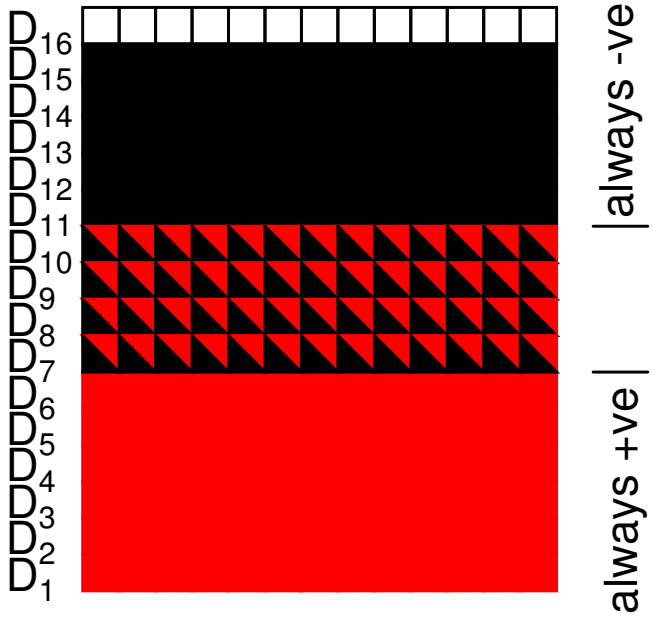


- Remove D_2 from the DAC
- $V_{av,2} = D_2 + D_{off} + NL|_{D_2+D_{off}}$

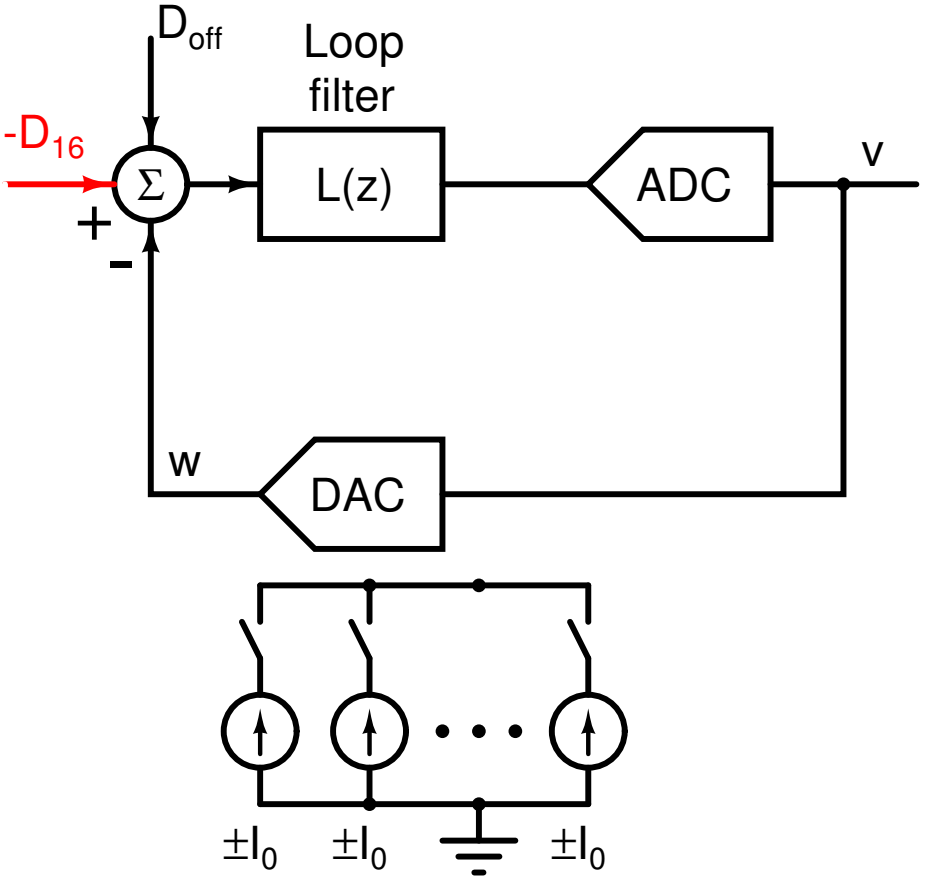
$$
\begin{aligned}
NL|_{D_1+D_{off}} &\approx NL|_{D_1+D_{off}} \\
D_2 - D_1 &\approx V_{av,2} - V_{av,1} \\
D_{k+1} - D_k &= V_{av,k+1} - V_{av,k}
\end{aligned}
$$

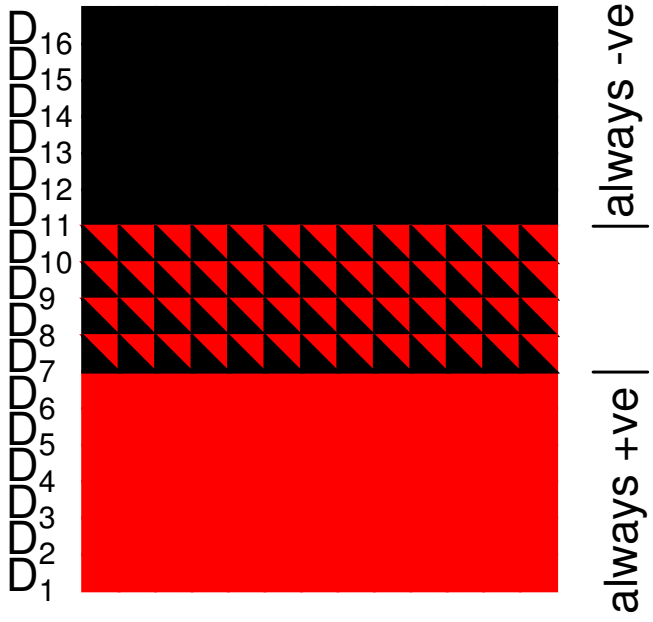
D_{16} *removed from the DAC*





D_{16} *removed from the DAC*





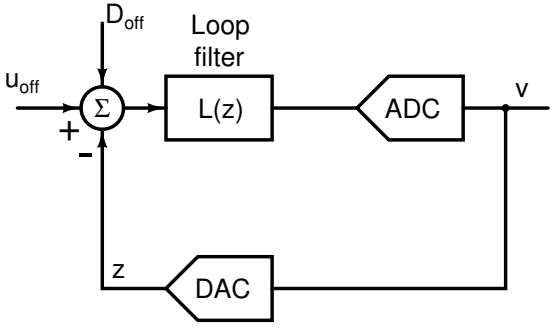
Estimating DAC errors

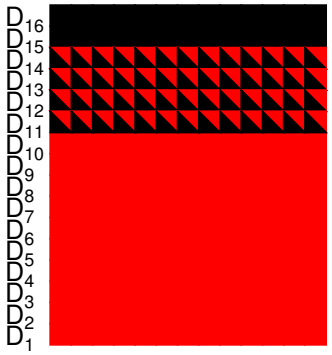
- Remove D_{16} from the DAC
- $V_{av,16} = -D_{16} + D_{off} + NL|_{-D_{16}+D_{off}}$

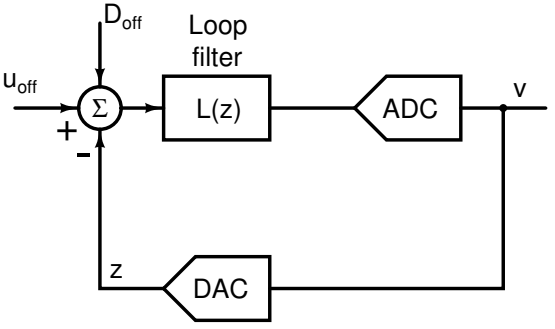
- Remove D_{15} from the DAC
- $V_{av,15} = -D_{15} + D_{off} + NL|_{-D_{15}+D_{off}}$

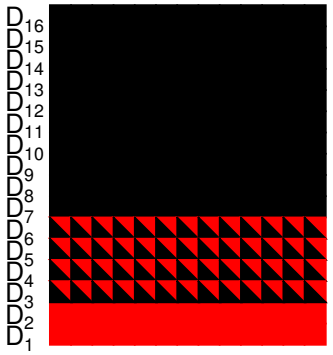
$$\begin{aligned} NL|_{-D_{15}+D_{off}} &\approx NL|_{-D_{16}+D_{off}} \\ D_{16} - D_{15} &\approx -V_{av,16} + V_{av,15} \\ D_{k+1} - D_k &= -V_{av,k+1} + V_{av,k} \end{aligned}$$

Estimating DAC errors







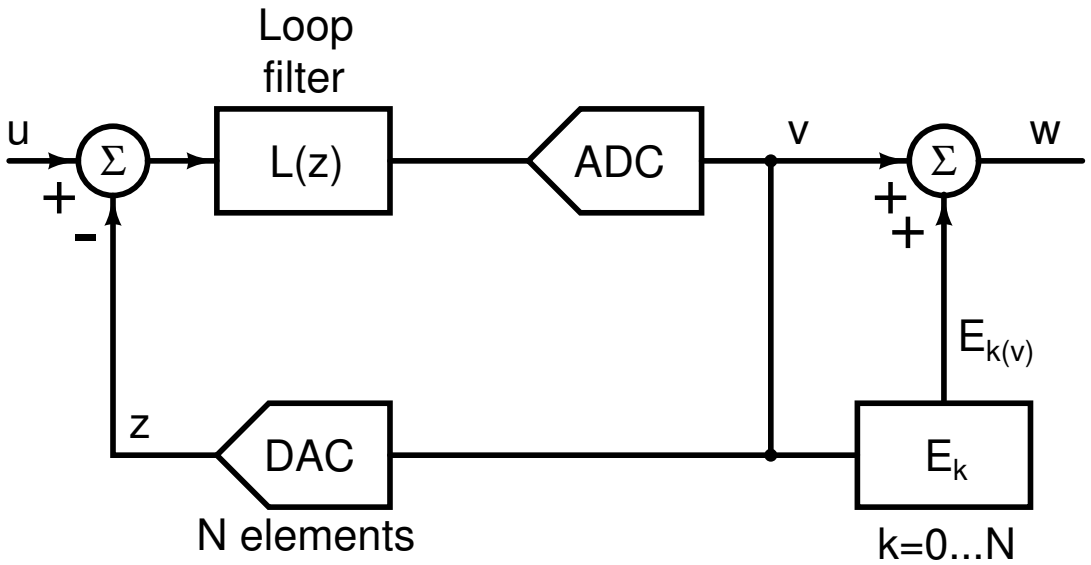


- Add a positive offset
- Determine $D_{k+1} - D_k$ for $k = 1 \ldots 8$
- $D_{k+1} - D_k = V_{av,k+1} - V_{av,k}$

- Add a negative offset
- Determine $D_{k+1} - D_k$ for $k = 9 \ldots 16$
- $D_{k+1} - D_k = -V_{av,k+1} + V_{av,k}$

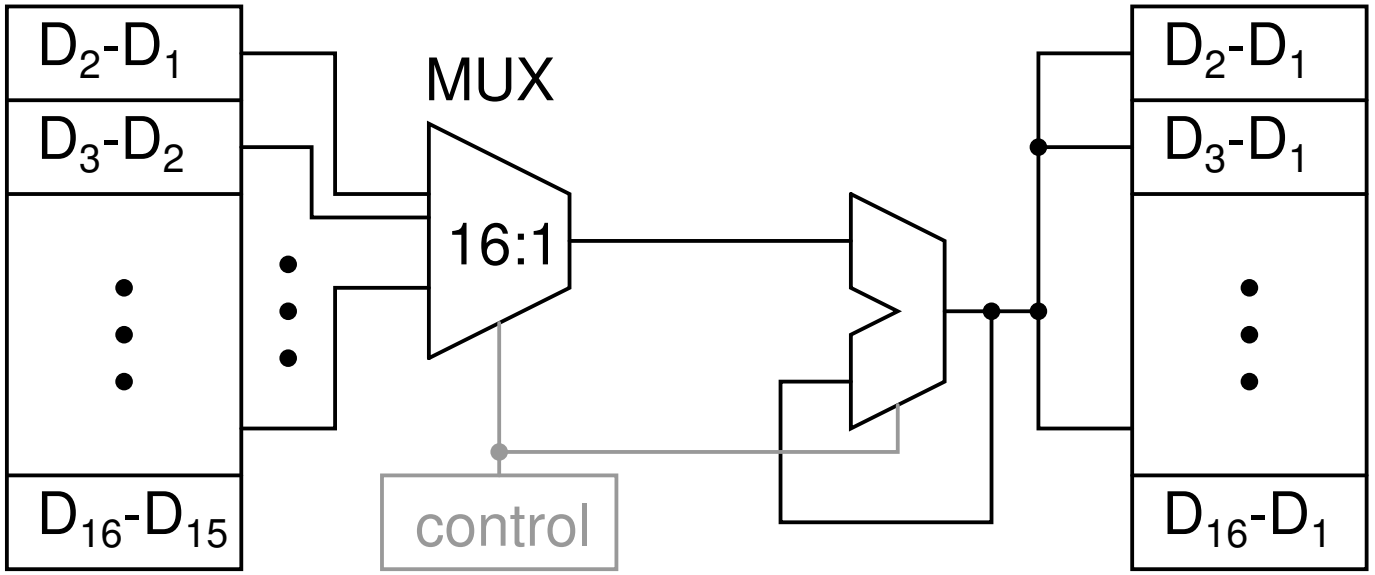
All successive differences $D_{k+1} - D_k, k = 2 \ldots 16$ thus obtained

Digital error correction



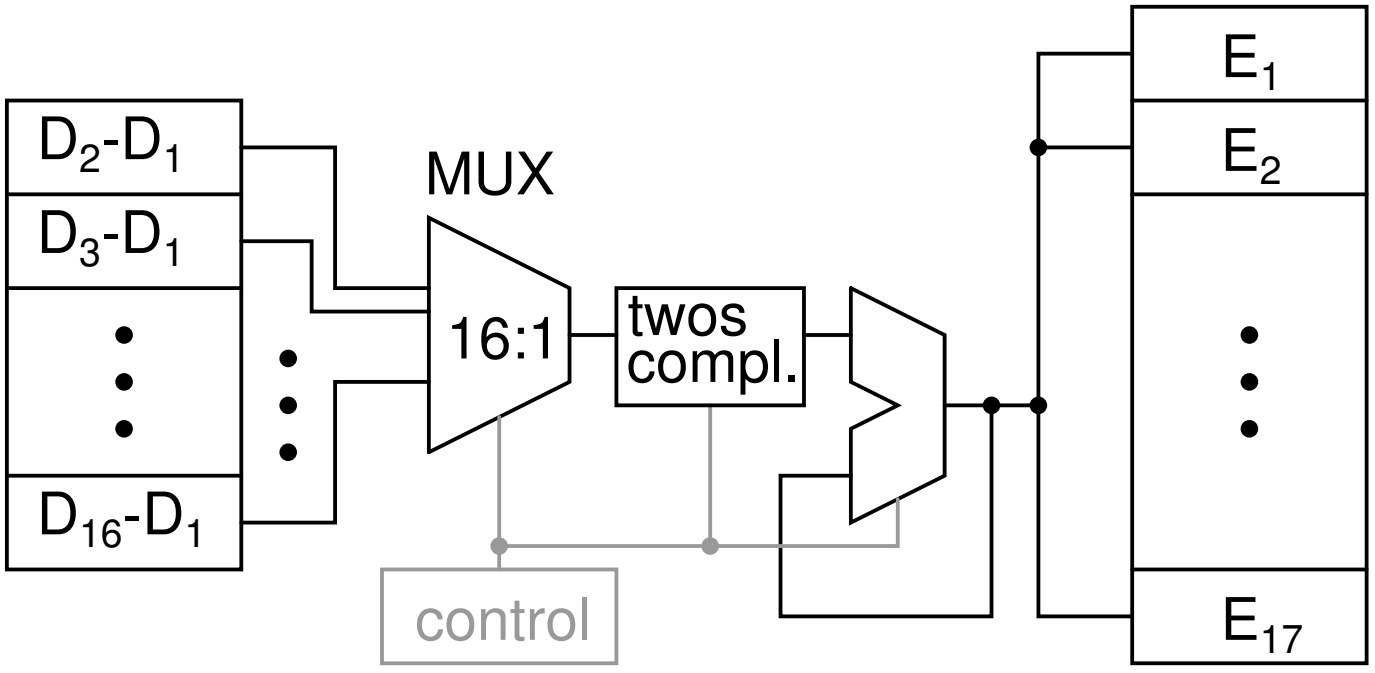
- Correction at DAC output
  - DAC has unequal element values D_k
  - Add $D_1 - D_k$ to D_k ($k = 2 \ldots 16$) to make all elements equal
- Equivalent correction at DAC input
  - Add $\pm(D_1 - D_k)$, $k = 2 \ldots 16$ to v
  - $+(D_1 - D_k)$ if D_k is switched positively
  - $-(D_1 - D_k)$ if D_k is switched negatively

Determine errors wrt one element (D_1)



$$
\begin{aligned}
D_2 - D_1 & \\
D_3 - D_1 &= (D_3 - D_2) + (D_2 - D_1) \\
&\vdots \\
D_N - D_1 &= (D_N - D_{N-1}) + (D_{N-1} - D_{N-2}) + \ldots + (D_2 - D_1)
\end{aligned}
$$

Determine correction values E_k for each level k



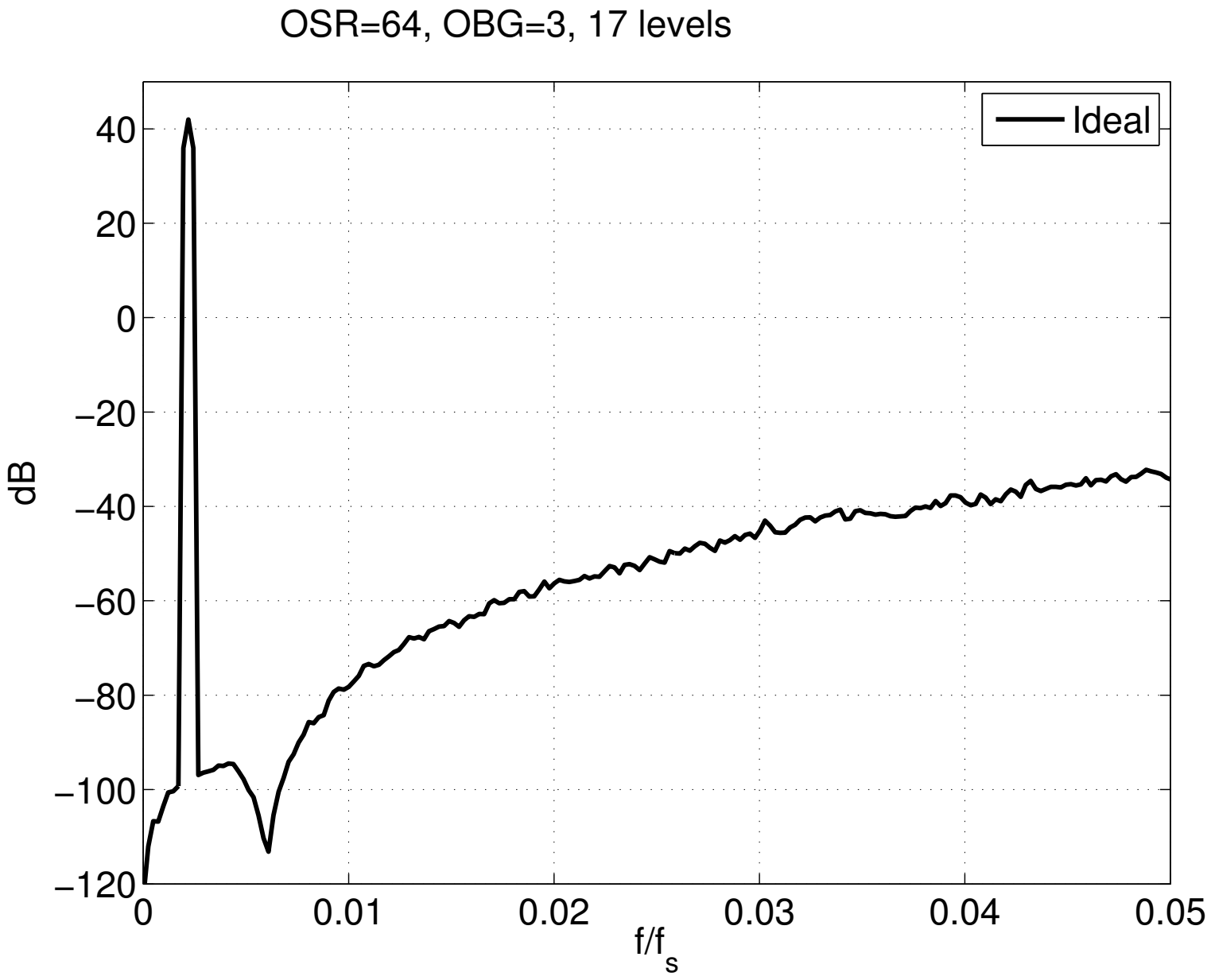
$$\begin{bmatrix} E_0 \\ E_2 \\ \vdots \\ E_N \end{bmatrix} = \begin{bmatrix} -1 & -1 & \dots & -1 \\ +1 & -1 & \dots & -1 \\ \vdots & & & \\ +1 & +1 & \dots & +1 \end{bmatrix} \begin{bmatrix} 0 \\ D_2 - D_1 \\ \vdots \\ D_N - D_1 \end{bmatrix}$$

Extra hardware required

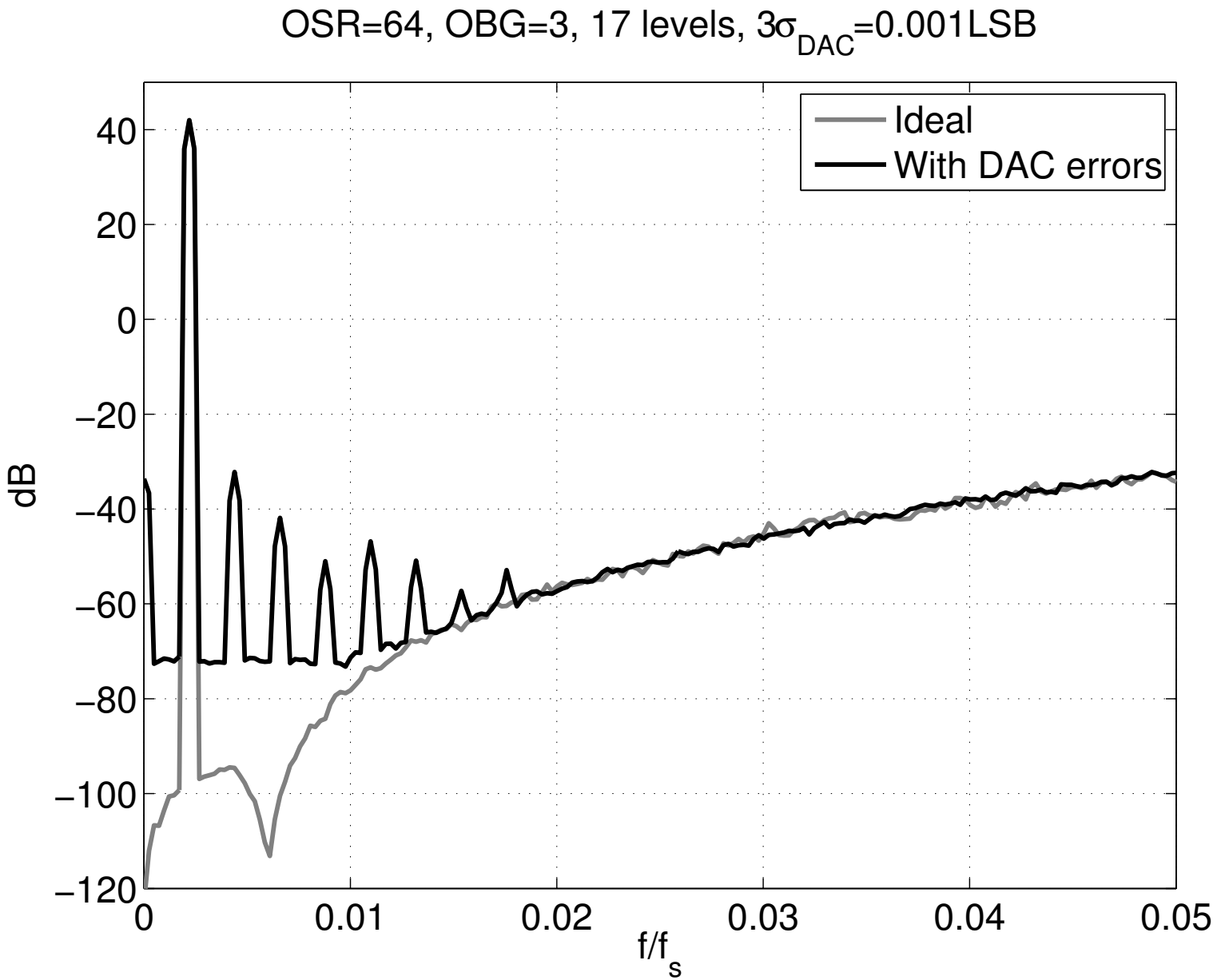
Determining calibration values

- 3 registers
- 1 MUX
- 1 accumulator with 2's complement

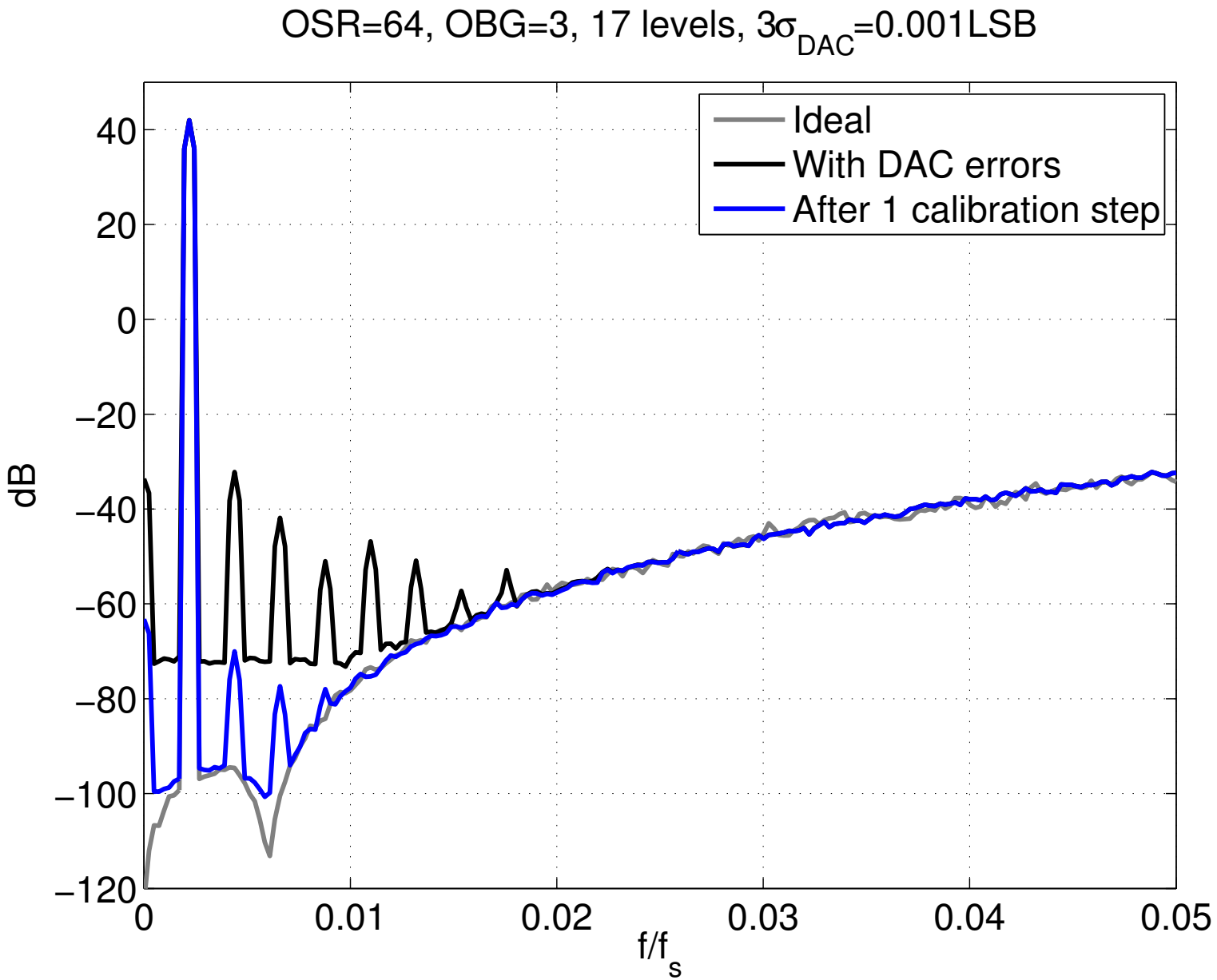
Simulation results: Ideal DAC



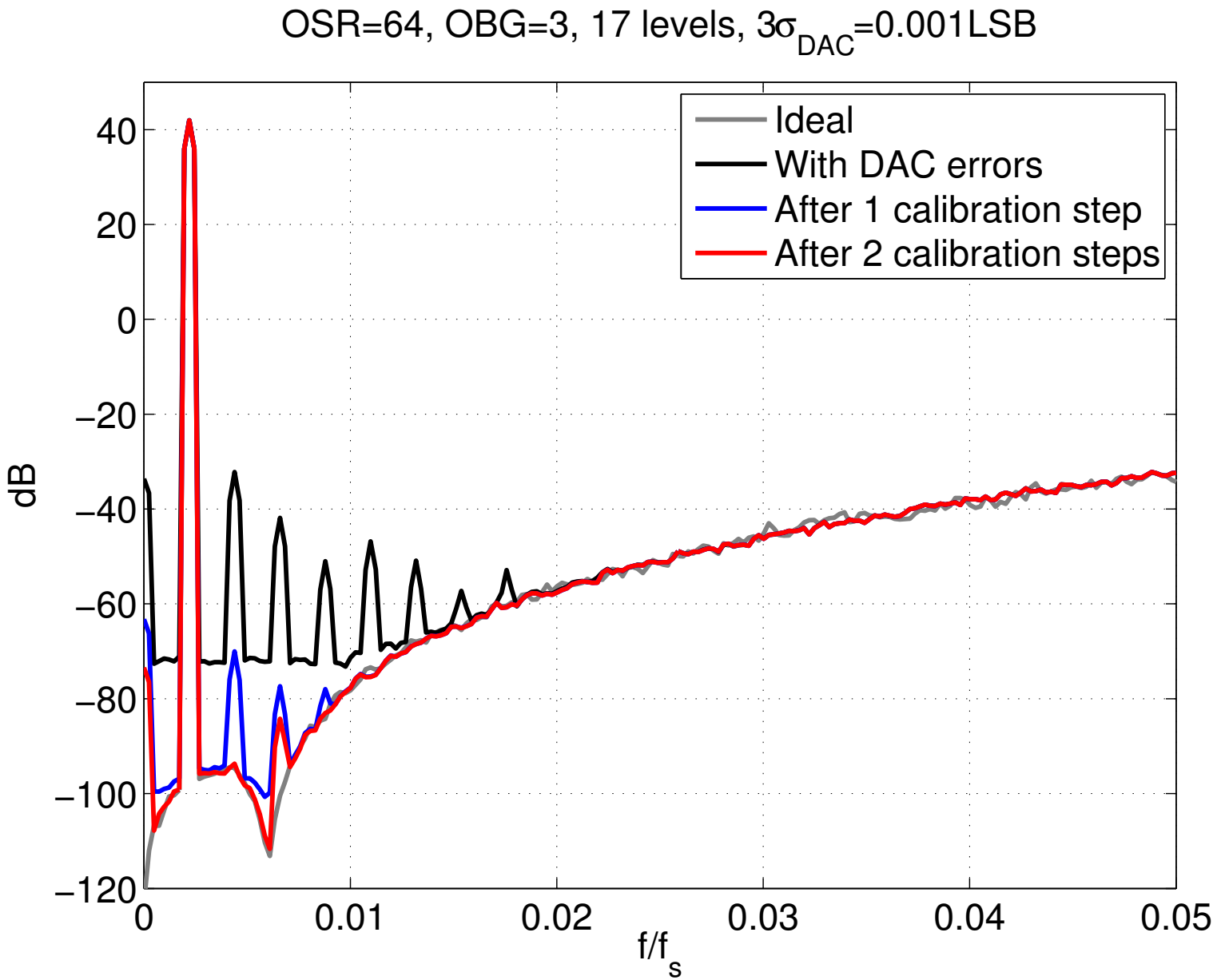
Simulation results: Effect of DAC nonlinearity



After one correction step—residual distortion



Repeat calibration using first correction—nearly ideal



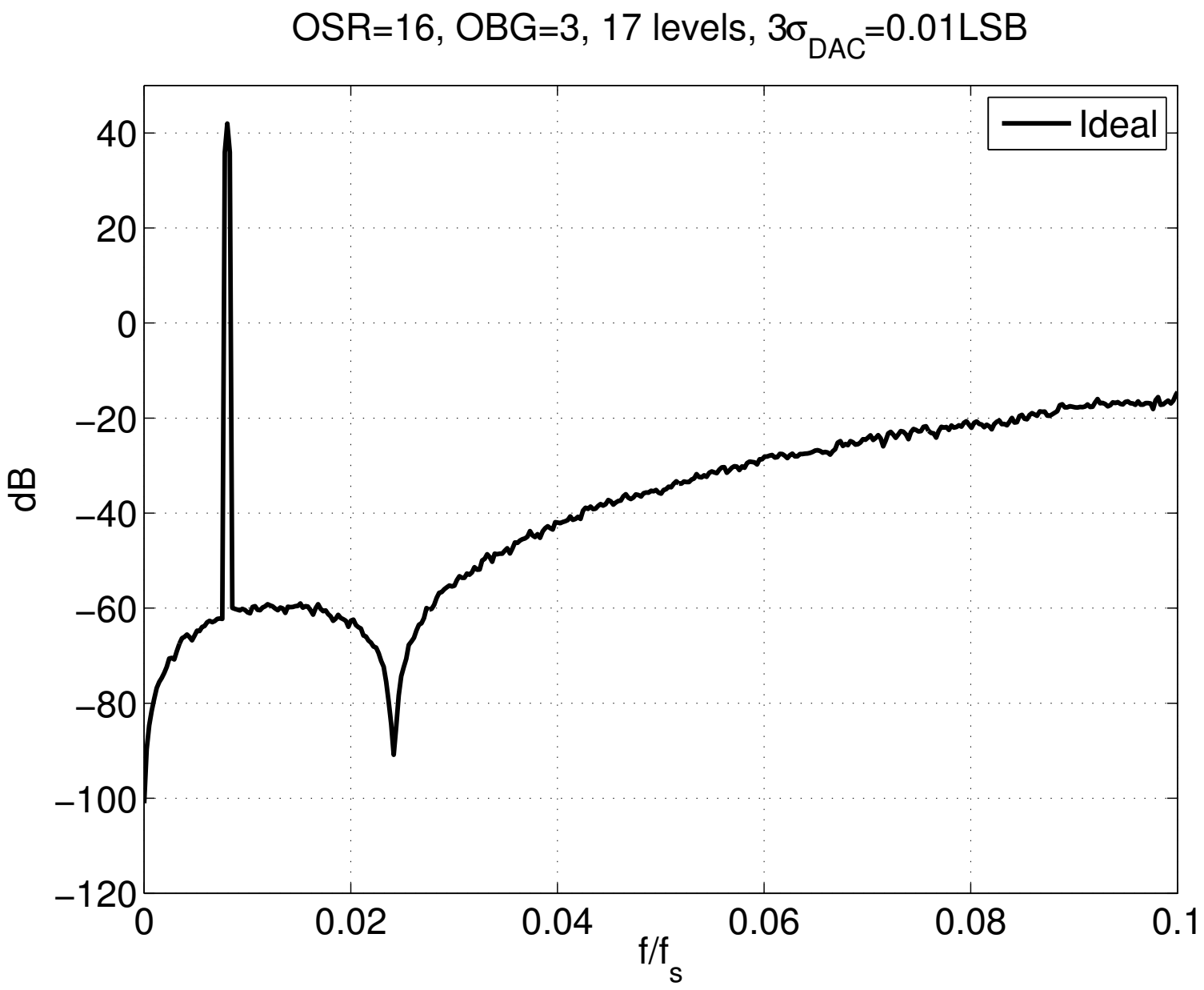
OSR=64, OBG=3, 17 levels, $\sigma_{DAC} = 0.001LSB$

	SNR	HD_2	HD_3
Ideal	121.9 dB	—	—
Without correction	97.0 dB	74.2 dB	83.8 dB
One correction step	120.5 dB	112.0 dB	119.3 dB
Two correction steps	122.0 dB	—	126.0 dB

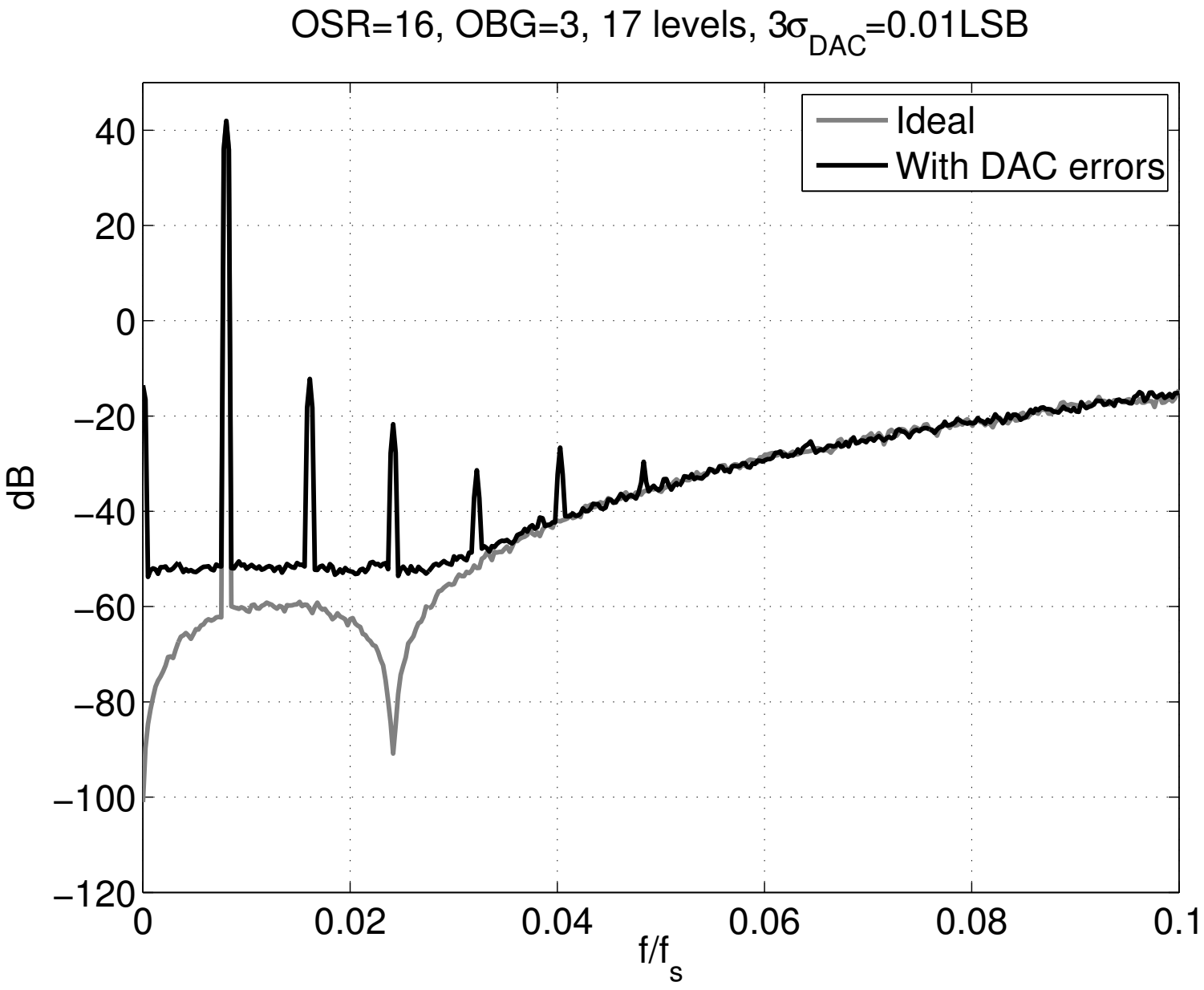
Using only first order averaging

- $\sim 2^{16}$ samples for the first step
- $\sim 2^{18}$ samples for second step
- $\sim 16(2^{16} + 2^{18}) \sim 5 \times 10^6$ samples for calibration

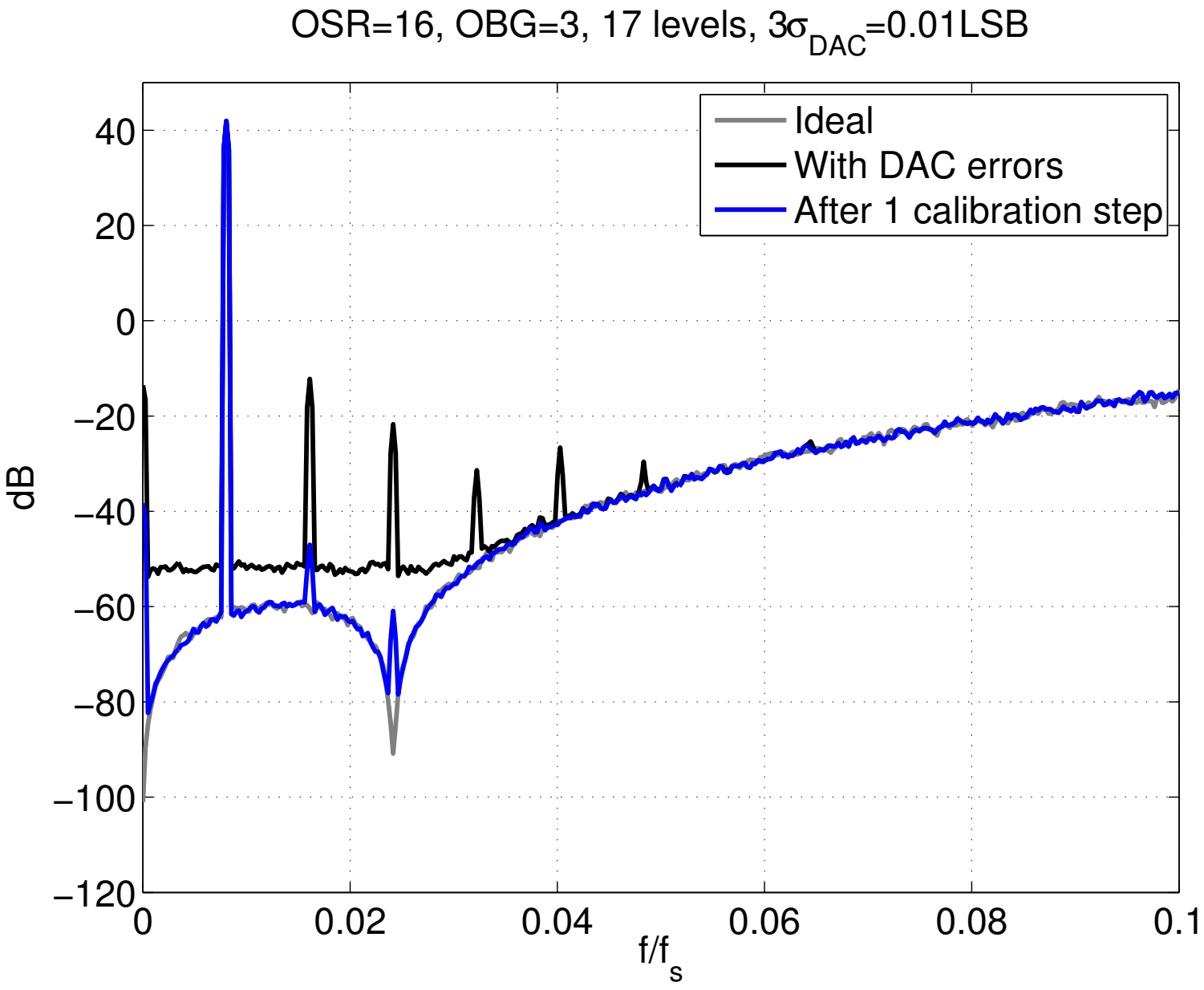
Simulation results: Ideal DAC



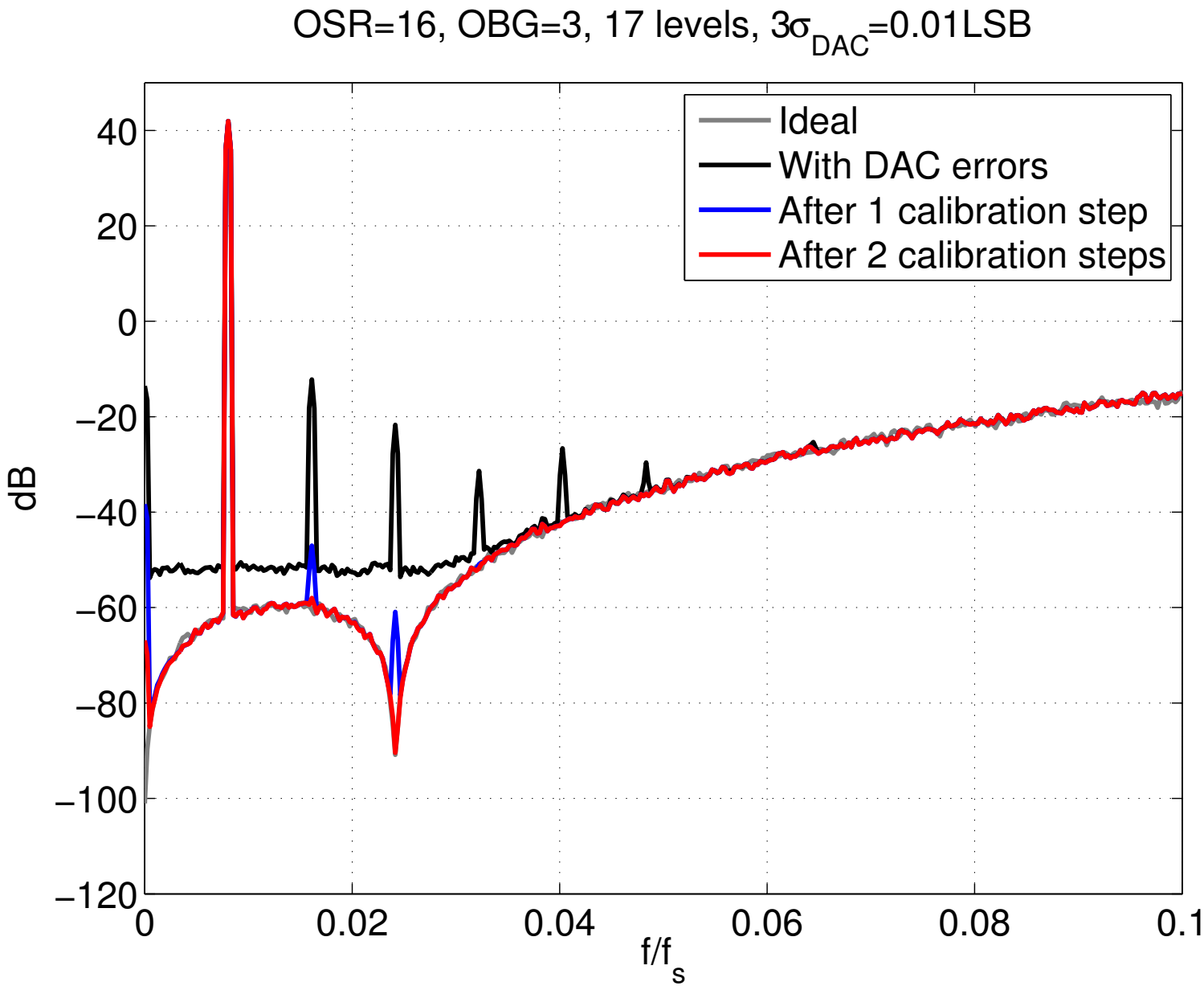
Simulation results: Effect of DAC nonlinearity



After one correction step—residual distortion



Repeat calibration using first correction—nearly ideal



OSR=16, OBG=3, 17 levels, $\sigma_{DAC} = 0.01LSB$

	SNR	HD_2	HD_3
Ideal	83.0 dB	—	—
Without correction	73.9 dB	54.2 dB	63.7 dB
One correction step	83.2 dB	88.7 dB	102.8 dB
Two correction steps	83.2 dB	—	—

Using only first order averaging

- $\sim 2^{15}$ samples for the first step
- $\sim 2^{15}$ samples for second step
- $\sim 16(2^{15} + 2^{15}) \sim 10^6$ samples for calibration

Conclusions

- DAC errors estimated by disabling DAC elements one by one in idle channel
- No reconfiguration of the loop
- Two steps sufficient to recover DAC errors accurately

References

S. R. Norsworthy, R. Schreier, and G. C. Temes (Eds.), *Delta-Sigma Data Converters: Theory, Design, and Simulation*, IEEE Press, 1997

J. Silva, U. Moon, J. Steensgaard, and G. C. Temes, "Wideband low-distortion delta-sigma ADC topology," *Electron. Lett.*, vol. 37, no. 12, 2001.

S. Pavan, N. Krishnapura, R. Pandarinathan, and P. Sankar, "A power optimized continuous-time $\Delta\Sigma$ ADC for audio applications," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 351 - 360, February 2008.