A 100 μW Decimator for a 16 bit 24 kHz bandwidth Audio $\Delta\Sigma$ Modulator

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***Abstract*— A decimation filter for a low power Delta Sigma ($\Delta\Sigma$) modulator with 24 kHz bandwidth and an in band resolution of 16 bits is designed with standard cells in a 1.8 V, 0.18 μm CMOS process. Retiming, Canonical Signed Digits (CSD) encoding along with optimal selection of data width are coded with a hardware description language (HDL) to obtain optimality for power and an automated design. The filter occupies an area of 0.46 mm^2 and consumes 100 μW from a supply of 1.8 V and is operational down to a supply voltage of 0.9 V. This makes it suitable for use with very low power $\Delta\Sigma$ data converters for digital audio.**

I. Introduction

Analog to digital (A/D) conversion for high fidelity audio is achieved using a $\Delta\Sigma$ modulator. A $\Delta\Sigma$ modulator encodes its analog signal with smaller number of bits (1-4) at an oversampled rate. The loop dynamics of a $\Delta\Sigma$ modulator ensure that the quantization noise acquired in the process is shaped out of the signal band. A decimation filter is required to remove the out of band noise to a sufficient level and achieve the full resolution at the Nyquist rate of the signal.

Low power, high dynamic range $\Delta\Sigma$ modulators for digital audio have already been proposed in literature [1][2]. This necessitates a decimation filter with as low power as its modulator to obtain a low power A/D converter. This paper discusses the decimation filter built for such a low power $\Delta\Sigma$ modulator [1]. The specifications of the modulator and the filter are shown in Table I. This paper investigates a filter that uses various architectural optimizations while being amenable to automated synthesis and place and route. The decimation filter was designed with standard cells in 0.18 μm CMOS technology.

TABLE I
Modulator Performance and Decimator Requirements

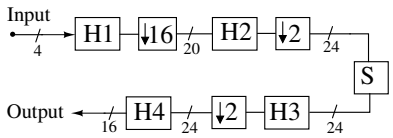
Modulator [1]		**Decimation Filter**	
Modulator order	3	Input No. of bits	4
Sampling rate	3.072 MHz	Passband ripple	0.05 dB
Nyquist rate	48 kHz	Passband edge	21.6 kHz
SNR [1]	93 dB	SNR [1]	96 dB (16 bit)
Power	90 μW	Power	< 100 μW

[1] SNR - Signal to Noise Ratio

The paper is organized as follows. The architecture of the filter is explained in Section II. Individual blocks of the filter are described from Section III to Section VI. Retiming, CSD encoding and optimal choice of hardware are described in Section III and Section IV. Simulation results in the estimation of power are given in Section VII. The measured results from the taped out design are given in Section VIII and Section IX concludes the paper.

II. Architecture of the Decimator

The block diagram of the decimator employing multi-stage decimation is shown in Fig. 1. Filtering and downsampling are done in multiple stages. This reduces the complexity of the first stage filter that operates at the highest rate [3][4]. The SINC4 filter provides the initial filtering, suppressing most of the shaped quantization noise. A large downsampling factor is employed in the first stage. Two more halfband filters downsample the signal to its Nyquist rate. The scaling block in the chain scales the signal to the full scale while the equalizer equalizes the pass band droop of the SINC4 filter. All the chosen filters have symmetric impulse response and hence the system guarantees linear phase response.



H1 - SINC4 H3 - 50th order Halfband
H2 - 10th order Halfband H4 - 34th order FIR (Equalizer)
S - Scaling Block

Fig. 1. Block diagram of the decimator

III. SINC4 Filter

A SINC filter, also called the Moving Average Filter, averages N samples. More stop band attenuation is obtained by cascading the SINC. The transfer function of an N tap SINC filter is,

$$H(z) = 1 + z^{-1} + z^{-2} + z^{-3} + ... + z^{-(N-1)} = \frac{1 - z^{-N}}{1 - z^{-1}}$$

A SINC filter has its nulls at $\frac{f_s}{N}$ where N is the number of taps and f_s is the sampling frequency. When downsampling by N, the aliasing noise falls at these nulls and is heavily attenuated (Fig. 6). Here N is chosen as 16 because the downsampling ratio is 16. Increasing N causes an increased droop in the signal passband and hence requires a complicated equalizer. A typical third order $\Delta\Sigma$ modulator shapes the quantization noise at its output as $E(z)(1 - z^{-1})^3$ where $E(z)$ represents the quantization noise spectrum. Sufficient attenuation of the shaped and boosted quantization noise is obtained with a cascade of four SINC filters (SINC4) that has a $\frac{1}{f^4}$ roll off [5].

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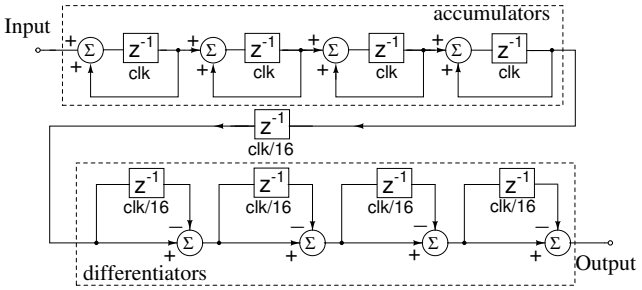

Fig. 2. SINC4 Filter implementation, Retimed, Pipelined Hogenauer structure

The SINC4 filter along with the downsampling of 16 is implemented as a Hogenauer structure [6] as shown in Fig. 2. It has a cascade of four accumulators working at 3.072 MHz and cascade of four differentiators at 192 kHz. This structure reduces hardware and power consumption. Accumulators are implemented in a *Retimed* fashion [7] (register in the forward path instead of the feedback path) which prevents glitches from input and combinational logic in adders in propagating to the next stage. This reduces the unwanted switching power. Similarly a pipelining register at the output of the fourth accumulator prevents the data at 3.072 MHz propagating to the differentiators. Retiming of accumulator's register and the pipelined register helps in saving 46% of power in SINC4.

Overflow in the accumulator register would not cause signal distortion if the signal representation is based on wrap around arithmetic (binary, 2's complement) and all the register width are chosen as [6]

$$\text{Bit width} = B_{in} + k \log_2 N$$

Here B_{in} is the input bit width (4 bit binary), K (4) is the number of cascaded SINC stages and N (16) is the tap length of the SINC. Hence Bit width is chosen as 20.

IV. Halfband Filters

Halfband filters are a class of equiripple FIR filters with order $N_{ord} = 4P + 2$, where $P \in \{1,2,3...\}$. They have symmetric impulse response with odd tap weights zero except the middle one which reduces the number of multipliers. Halfband filters have their -6 dB frequency at one fourth the sampling frequency. Hence the maximum downsampling after the filtering is two. The halfband filtering along with downsamping is implemented as a polyphase structure that reduces the effective operating frequency of filter and hence the power consumption [3][4]. The order of the halfband filters are chosen such that the overall decimator's passband ripple is constrained to 0.05 dB and the aliasing noise does not cause degradation in the in band SNR. Tap weights of the filter are encoded in Canonical Signed Digits (CSD) (similar to Booth multiplication) that reduces the number of computations [4][8]. The signal is represented in 2's complement. Truncation of the coefficients to finite number of CSD alters the frequency response. The accuracy of the frequency response, here the passband ripple, decides the number of CSD. Here the encoded tap weights have an accuracy of 2^{-14}.

A. First Halfband Filter

The input to the first halfband filter is the data from the SINC4 filter at 192 kHz. The chosen tenth order filter has an aliasing band (74.4 kHz - 96 kHz) attenuation around 60 dB and a relaxed transition band (Fig. 7). The filter's effective operating rate is 96 kHz because it is implemented as a polyphase structure. The block diagram of the polyphase implementation of the filter is shown in Fig. 3. The P_4 block in the figure pads four LSB to the data path and b_0, b_2, b_4, b_5 are tap weights.

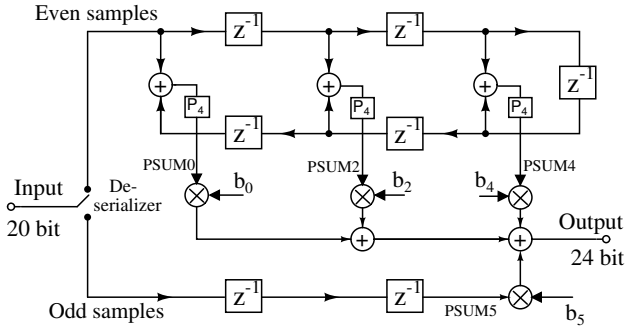

Fig. 3. Polyphase implementation of the first halfband filter (10th order)

The internal state of the filter, showing multiplication of coefficients, is implemented as shown in Fig. 4. The multiplication of a coefficient is nothing but addition or subtraction of shifted signals. This arithmetic is further nested based on Horner's rule [7]. This reduces the effective right shift operation and hence the effect of truncation noise. For e.g. $2^{-3} - 2^{-5} - 2^{-7} = 2^{-3}\{1 - 2^{-1}(2^{-1} + 2^{-3})\}$. A 2^{-1} is equivalent to right shift of one bit and is obtained by dropping an LSB in the multiplicand. This nested multiplication demands extra shifting operations compared to the non nested multiplication, but can be implemented without any additional hardware.

An optimum number of bits for the adder and the data path is 24 which is explained as follows. The quantization noise Power Spectral Density (PSD) of a full scale sinusoid (with 0 dB power) quantized to $Q1$ bits with a sampling rate 1 Hz is $N_1(f) = 10^{-6Q1/10}$. If a small band of its quantization noise has to be attenuated by R dB then in that small band $N_2(f) = 10^{-6Q2/10}$ and the number of bits $Q2$ has to be more than $Q1$. Hence it can be written

$$10\ log_{10}\frac{N_2(f)}{N_1(f)} = R \quad or \quad Q2 = Q1 + \frac{R}{6}$$

Every extra bit can handle 6 dB more dynamic range. Here the dynamic range of the signal is 96 dB (16 bit). Hence employing 24 bits in the filter attenuates the aliasing quantization noise to a maximum of 48 dB with respect to the in band noise floor and is sufficient to preserve the in band SNR.

B. Second Halfband Filter

The final filtering is done by the second halfband filter before the signal is downsampled to the Nyquist rate (48 kHz). The chosen fiftieth order filter has its input data at 96 kHz and

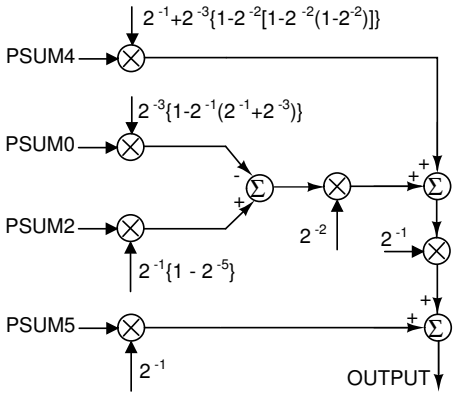

Fig. 4. Internal state representation of the first halfband filter

operates with an effective frequency of 48 kHz. The aliasing band (26.4 kHz - 48 kHz) has an attenuation around 50 dB (Fig. 7). The requirement of a sharp transition band and small in band ripples necessitates the high filter order. Similar CSD encoding and nested arithmetic are employed.

V. Scaling Block

If the input signal amplitude of a ΔΣ modulator exceeds a certain percentage of the full scale of the quantizer, the modulator becomes unstable and its output does not faithfully reproduce its input signal. The maximum amplitude that can be fed to the modulator is called the Maximum Stable Amplitude (MSA). For the ΔΣ modulator in [1] MSA is 85% of the full scale. The output of the modulator will seem to swing fully in four bits because high frequency noise is riding on the actual signal. The scaling is done after the first halfband filter where the high frequency noise is attenuated to a level comparable to the noise floor in the in band. Scaling the signal also reduces the effect of truncation noise in filters that follow it.

$$S = \frac{1}{0.8605} = 1 + 2^{-2}\{2^{-1} + 2^{-2}(2^{-1} + 2^{-3}[1 - 2^{-2}])\}$$

The scaling value is kept slightly smaller than 1/MSA to prevent overflow in the presence of passband ripples in other filters. This scaling value is also encoded in CSD and implemented with Horner's rule.

VI. Equalizer

The passband droop caused by the SINC4 filter is equalized by this filter and works at the Nyquist rate (48 kHz). The equalizer's magnitude response is the inverse of the magnitude response of SINC4 in the in band (0 - 24 kHz). From this an FIR approximation to fit the desired magnitude response is obtained by *Parks McClellan* method. A thirty fourth order filter equalizes the overall passband magnitude response to unity while constraining the passband ripple to 0.05 dB. Similarly tap weights of the filter are encoded in CSD and implemented according to Horner's rule as discussed in the section IV.

VII. Synthesis and Simulation Results

The design was synthesized in 1.8 V, 0.18 μm CMOS technology with standard cells using the tool *Synopsys Design Compiler* and Placed and Routed using *Cadence Encounter*. Fig. 5 shows the layout of the fabricated chip. The test data to estimate the power of the filter is the output from the ΔΣ modulator [1] stimulated with an appropriate signal. The power consumption is evaluated using the tool *Synopsys Primepower* that estimates power based on the switching activity of various nodes in the circuit. The power consumption of the filter for three different test input to the modulator is mentioned in the Table II. The Table III shows the block level power consumption of the filter when the test signal is a tone at 1.6875 kHz. The frequency response of the SINC4, halfband filters and the equalizer are shown in Fig. 6, Fig. 7 and Fig. 8 respectively. The shaded area in the frequency responses are the noise aliasing bands for the filter. The Fig. 8 also shows the passband magnitude response before and after the equalization. The enlarged plot shows that the equalized frequency response has ripples constrained to 0.0465 dB.

TABLE II
Power consumption for various test inputs

Modulator Stimulus	Filter Power (μW)
Tone at 1.6875 kHz	96.7
White noise	100.9
Zero input	99.7

TABLE III
Power Profile

Block	Power (μW)	Area (μm^2)
SINC4	46.4	29958
Halfband one	5.9	41941
Halfband two	14.1	191731
Equalizer	15.2	186621
Scaling Block	2.3	7374
Clock dividers, buffers	12.7	3226
Total	**96.7**	**460851**

VIII. Measured Results

The design was fabricated in 1.8 V, 0.18 μm CMOS technology. An FPGA was programmed to generate the required test stimulus corresponding to the ΔΣ Modulator [1] and the output samples from the chip were captured. The SNR was calculated from the spectrum of these output samples and it matches exactly with the result obtained through simulation. The measured power consumption of the chip at 1.8 V supply was 104 μW and matches close to the simulation estimate of 96 μW. It was also verified that the chip was operational correctly down to supply voltage of 0.9 V while running at 3.072 MHz. The corresponding reduction in power can be observed from the Table IV.

IX. Conclusion

A low power decimation filter for digital audio employing architectural optimizations with the aid of automated CAD

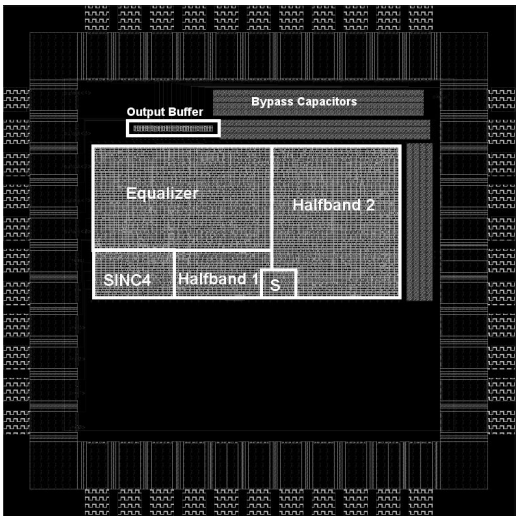

Fig. 5. Layout of the chip

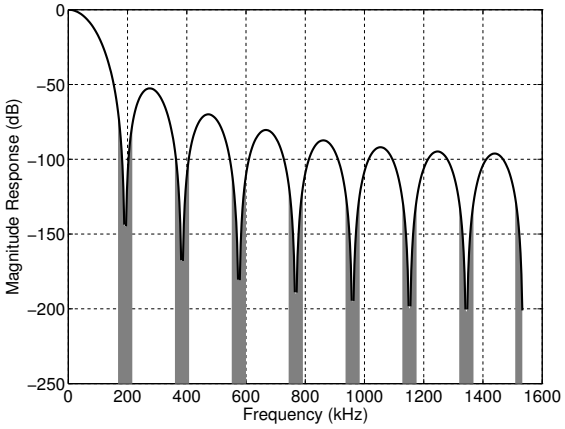

Fig. 6. Frequency Response: SINC4 (Aliasing bands are shown in gray)

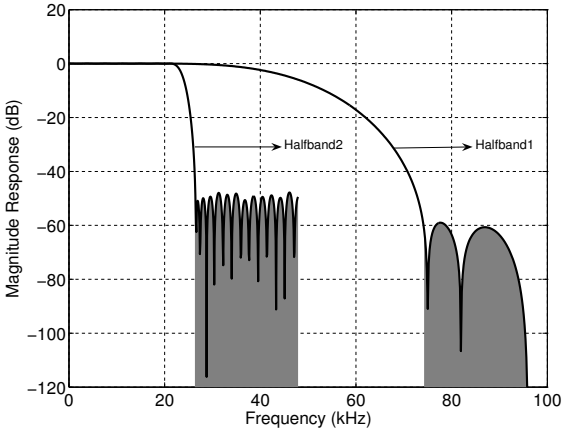

Fig. 7. Frequency Response: Halfband one and Halfband two (Aliasing bands are shown in gray)

tools has been developed. The test results of the fabricated design matches well with the estimation of power through simulation. The filter achieves a low power consumption

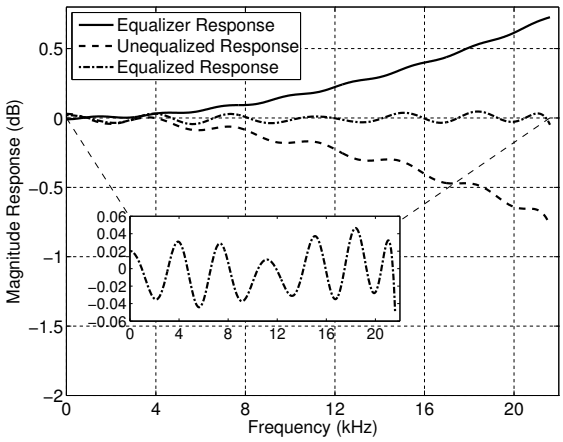

Fig. 8. Frequency Response: Equalizer, Unequalized & Equalized decimator

TABLE IV
POWER CONSUMPTION AT VARIOUS SUPPLY VOLTAGES

Power Supply(V)	Current Drawn(μA)	Power Consumption(μW)
1.8	58	104.4
1.5	46	69.0
1.2	36	43.2
1.0	29	29.0
0.9	26	23.6

without the need of handcrafted circuitry making it amenable to automation with CAD tools. This also proves that it is possible to design a decimation filter with as low power as recently published $\Delta\Sigma$ modulators. The filter consumes 100 μW from 1.8 V. As the filter is functional down to 0.9 V, the power consumption can be further reduced by a factor of two by using a linear regulator to provide 0.9 V from a 1.8 V supply.

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