A 90μW 15-bit $\Delta\Sigma$ ADC for Digital Audio

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***Abstract*— Architecture, circuit design details and measurement results for a 15 bit audio continuous-time $\Delta\Sigma$ modulator (CTDSM) are given. The converter, designed in a 0.18 μm CMOS technology, achieves a dynamic range of 93.5 dB in a 24 kHz bandwidth and dissipates 90 μW from a 1.8 V supply. It features a third order active-RC loop filter, a very low power 4-bit flash quantizer and an efficient excess delay compensation scheme to reduce power dissipation.**

I. Introduction

Power reduction and implicit anti-alias filtering are key motivators for using CT-DSMs for digitizing low frequency analog signals. Several implementations targeting the audio range have been reported recently [1] [2] [3] [4] [5]. The first three of these designs use a single-bit quantizer. Single bit CT-DSMs have several problems, which can be mitigated by using a multibit quantizer in the loop. In this work, we describe the design of a 15-bit CT-DSM for audio applications. Implemented in a 0.18 μm CMOS technology, the modulator (operating with an OSR of 64) consumes 90 μW from a 1.8 V supply and achieves a dynamic range of 93.5 dB for a signal bandwidth of 24 kHz. The modulator employs several strategies to reduce power consumption. A large input signal swing (3 V peak-to-peak differential) is used to reduce noise requirements of the opamps and offset requirements in the flash ADC. An appropriate choice of the loop Noise Transfer Function (NTF) results in a performance that is tolerant of comparator offsets. The deleterious effect of extra poles in the loop filter (due to the finite bandwidth of the opamps) is mitigated using a novel excess delay compensation technique. This enables the use of very low bias currents in the operational amplifiers.

The architectural and circuit details of the modulator form the subject of the rest of the paper, which is organized as follows. In Section II, we justify the various design choices made in this work. Section III delves into the implementation issues of various circuit blocks used in the modulator. Experimental results from a prototype modulator designed in a 0.18 μm CMOS process are shown in Section IV. Section V gives the conclusions.

II. Choice of Architecture

A single loop topology was chosen over a MASH design to avoid the complexity resulting from the additional circuitry needed to match the NTF and the digital noise cancelling filter. A third order NTF was chosen so that a peak Signal to Quantization Noise Ratio (SQNR) well above the 92 dB SNR required of the modulator could be achieved. This way, the performance of the design would be limited by thermal noise. We now justify the other architectural choices made in the converter.

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A. Single-bit versus Multi-bit Quantization

A multibit quantizer, while having an inherently low quantization noise, also allows a more aggressive NTF when compared to a single bit design. This results in a significant reduction of in band quantization noise. For example, with a four-bit quantizer in the loop, an NTF with an out-of-band gain of 2.5 results in a peak SQNR of about 118 dB. The effect of clock jitter on the modulator is also greatly reduced when a multi-bit quantizer is used.

The input to the loop filter is shaped quantization noise. The amplitude of this noise is much lower in a multibit design when compared to a single bit modulator. It is thus seen that the loopfilter opamps need a lower slew rate, which translates into a lower power dissipation for the entire modulator. Based on the discussion above, a single loop multibit architecture was chosen. A four bit quantizer was chosen as a reasonable compromise between the benefits offered by multibit operation and the exponential complexity of implementation.

B. Noise Transfer Function

A maximally flat NTF with an out-of-band gain of 2.5 was chosen as a compromise between quantization noise, jitter noise and sensitivity to variations in RC time-constants of the loop filter. The peak Signal to Quantization Noise Ratio (SQNR) was simulated to be about 118 dB. The in band noise due to 200 ps RMS clock jitter was calculated to be -98 dBFS.

C. Loop Filter Topology

A "cascaded integrators with feedforward summation" (CIFF) architecture was chosen to implement the loop filter. In this work a resistive feedback DAC was used to reduce thermal noise due to the DAC. The more common distributed feedback modulator would require three such DACs which result in a large chip area. It can also be shown that the size of the first integrating capacitor is smaller for a CIFF loop filter, when compared to a distributed feedback structure. The peaking in the Signal Transfer Function (STF) was not an issue in this particular design.

III. Circuit Design

A. Loop Filter

Weighted addition of the integrator outputs is performed using a summing amplifier. The first integrator uses an opamp with a PMOS input stage for low $1/f$ noise. The other integrators and the summing amplifier use operational amplifiers with NMOS input pairs. The input referred noise of the loop filter is dominated by the thermal noise from the input and DAC resistors and the input referred noise of the first opamp. The first integrator uses resistors of 100 kΩ, while larger resistors are used in subsequent integrators. The third integrator has the largest time constant, and using a large integrating resistor

has the additional benefit of reducing the area of the third capacitor.

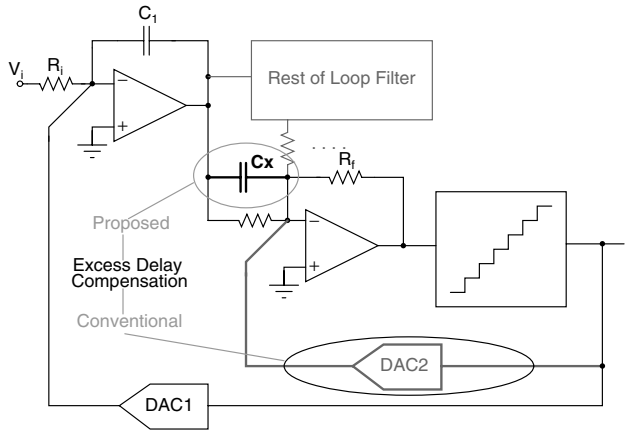

Fig. 1. Excess delay compensation - conventional and proposed.

The poles in the opamps introduce excess delay in the loop filter, which can potentially cause instability in the modulator. One way of mitigating this problem (at the expense of power dissipation) is to use wideband opamps. An alternative approach is to use low speed (power) opamps, and compensate for the delay introduced by the loop filter. A conventional way of combating excess delay is to have a direct path around the quantizer using a second DAC, as shown in Fig. 1. This needs an extra DAC, which occupies a large area. In this work, we use a feed-in capacitor C_x (drawn using a dark line) to accomplish the same task. With ideal opamps, the equivalent gain of the direct path around the quantizer is seen to be $\frac{R_f C_x}{R_i C_1}$.

A CAD routine and methodology were developed to determine the relative weighting factors and C_x required in the summing amplifier to realize the desired NTF. The routine accounts for the frequency response of the operational amplifiers and the (small) excess delay introduced by the ADC & DEM logic.

B. Operational Amplifiers

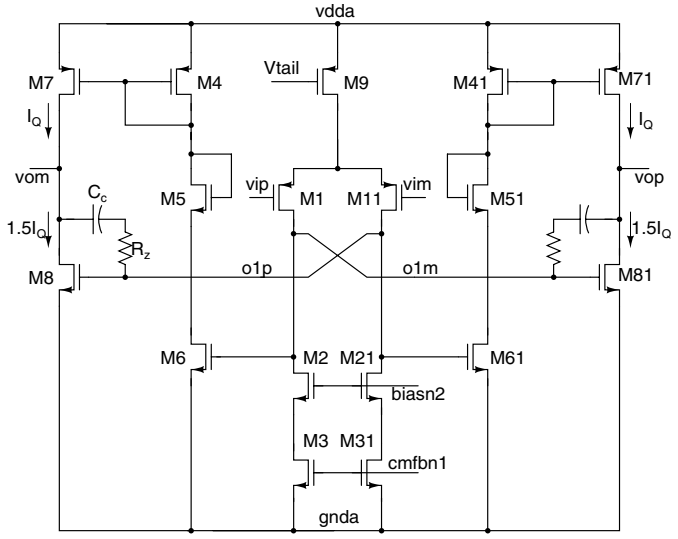

Fig. 2. Operational amplifier used in the first integrator.

The first integrator determines the overall noise and linearity of the modulator. The circuit schematic of the opamp used in the first integrator is shown in Fig. 2 [6]. It is a two stage design, with a first stage using a PMOS input pair with long channels to lower input referred 1/f noise, and a class AB second stage. The opamp is Miller-compensated using R_z and C_c, as shown in Fig. 2. A common-mode feedback circuit stabilizes the output level of the the first stage. The quiescent output voltage at nodes $o1p$ and $o1m$ (which is also the gate-source voltage of $M6$-$M61$, and $M8$-$M81$) sets the quiescent currents in the second stage. To set the output quiescent currents accurately, the common-mode reference is derived from a diode connected transistor biased with a fixed current. Since the signal swings at $o1p$ and $o1m$ are modest, the linearity of the common-mode detector is not critical. The first stage uses a $4\,\mu$A tail current. At high frequencies, where the compensation capacitors C_c can be considered shorts, the common-mode output impedance of the opamp in Fig. 2 consists of the parallel combination of the positive resistance of the diode connected (through C_c) transistors $M8$ and $M81$ and the negative resistance formed by the loop $M6$-$M4$-$M7$ and $M61$-$M41$-$M71$. If equal quiescent currents are used in $M8$ and $M7$, this impedance is infinite. In presence of mismatches, it is possible for the common-mode output impedance to have a negative real part and lead to instability. To prevent this, quiescent currents in the lower transistors $M8$ and $M81$, which contribute to the positive resistance, are made 1.5 times larger than quiescent currents in the upper transistors $M7$ and $M71$. The rest of the quiescent current is provided by the common-mode feedback circuitry. This technique ensures stability and reliable operation of the common-mode feedback loop. Quiescent current through each output branch ($M8$, $M81$) is $1.2\,\mu$A. The schematic of the operational amplifier used in the second and third integrators and the summing block is similar to that shown in Fig. 2, except that an NMOS input pair, with a smaller bias current is used.

C. Flash A/D Converter & Dynamic Element Matching Logic

The block diagram of the 4-bit flash ADC used in this work is shown in Fig. 3. It consists of 15 differential comparators, a resistor ladder and a digital backend. The nominal LSB size is 187.5 mV. This greatly relaxes the offset requirements of the comparators. The circuit diagram of the comparator and the corresponding clock waveforms are shown in Figs. 3(b) and (c) respectively. The comparator operates as follows. When LC is high, the nodes X & Y are connected to ip & im through two coupling capacitors C_b, which have been charged to $V_{refp} - V_{cm}$ and $V_{refm} - V_{cm}$ respectively. Thus, the differential voltage between nodes X & Y at the end of the on-phase of LC is $(V_{ip} - V_{im}) - (V_{refp} - V_{refm})$. L goes high after LC goes low. In this phase, the back to back inverters formed by M1, M2, M3 & M4 are activated, thereby regenerating the difference between the voltages at nodes X & Y. After allowing for some regeneration time, the decision made by the latch is held on C^2MOS inverters, which are clocked by Ld, which goes low before L goes low. Even after L goes low, the nodes X & Y will remain at $\mathrm{V_{dd}}$ or ground. Hence, a small reset phase LR is necessary to clear the latch of its prior decision. At the end of this phase, the absolute potentials at X and Y are brought to $\mathrm{V_{dd}}/2$. Note that when L is high, the coupling capacitors C_b are charged to $V_{refp} - V_{cm}$ and

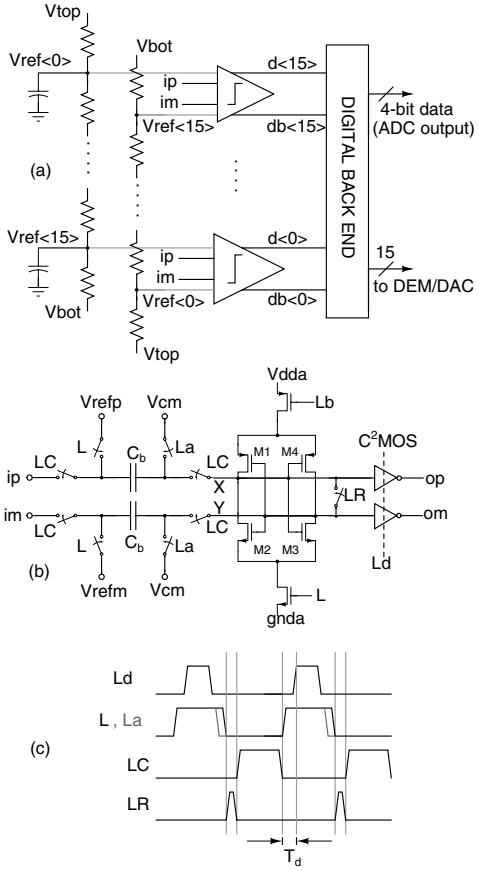

Fig. 3. (a) Block diagram of the flash quantizer (b) Comparator Schematic & (c) Clocks

$V_{refm} - V_{cm}$. To prevent reference dependent charge injection on to the coupling capacitors, their "bottom" plate is turned off first, using a slightly advanced version of L, denoted by La. The sampling instant of the ADC is the falling edge of LC, and the output is available at the rising edge of Ld. The latency of the ADC is denoted as $\mathrm{T_d}$ in Fig. 3(c). The estimated $3\,\sigma$ random offset of the comparator was about 50 mV.

The comparator of Fig. 3(b) has several advantages, making it an appropriate choice in the context of a $\Delta\Sigma$ modulator. Note that it consumes no static power. The dynamic offset of the latch is also small, since nodes X & Y are biased at mid-supply. During the LC phase, the coupling capacitors C_b share their charge with the small parasitic capacitances at nodes X & Y. Hence, only this small amount of charge has to be replenished when L is high. Thus large resistors can be used in the resistor ladder, reducing power dissipation. Many flash converters used in $\Delta\Sigma$ modulators use offset-cancelled preamplifiers to reduce latch offset. This strategy increases area and power dissipation. Cancelling the offset in every clock cycle also necessitates large bias currents in the preamplifiers. In this work, we eliminate the preamplifier by using a large LSB size. Further, the 4-bit ADC output code is generated from the thermometer code by summing the number of 1's the thermometer code. This makes the quantizer characteristic inherently monotonic.

The modulator was simulated for various levels of Gaussian distributed offsets in the comparators. 1000 trials for each level of offset were run. Fig. 4 shows the results. The lines

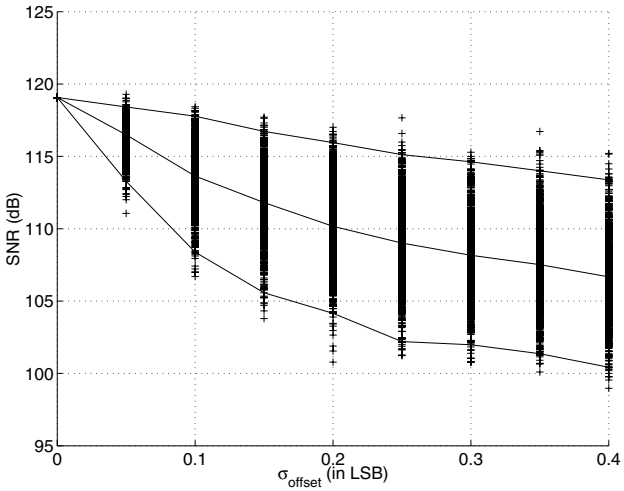

Fig. 4. Effect of comparator random offset on in-band SNR - for each level of offset, 1000 trials were simulated. The lines show the modulators with the best 1% SNR, mean SNR and the worst 1% SNR respectively.

represent the mean, the best and the worst 1% of the SNRs. It is thus seen that to achieve a 15 bit performance from the modulator, random offsets in the comparator with a standard deviation of up to 0.4 LSB can easily be tolerated, as long as the characteristic of the quantizer is monotonic.

The thermometer coded output of the flash ADC is converted into a binary code, which is also the modulator output. The binary code is generated by summing the number of ones in the thermometer output, by tree structured combinational logic. In this work, Data Weighted Averaging (DWA) is used to shape mismatch noise from the feedback DAC away from the signal band.

D. Feedback DAC & Reference Generation

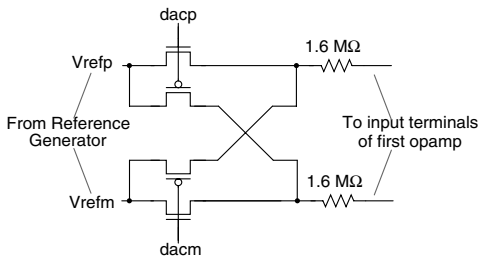

Fig. 5. DAC unit element.

The feedback DAC consists of resistive unit elements, each of value 1.6 MΩ. The width of these resistors is chosen to be as small as possible to reduce parasitic capacitance which causes excess delay in the loop. Matching requirements are greatly relaxed, thanks to dynamic element matching. Fig. 5 shows the a unit element of the DAC. The resistors are driven by differential reference voltages V_{refp} & V_{refm}. The other ends of the resistors are connected to the virtual ground terminals of the first integrator. The polarity of the current flowing into the loop filter is determined by the control bits.

IV. Measurement Results

The third order continuous-time $\Delta\Sigma$ ADC was fabricated in a 0.18 μm CMOS process through Europractice. Fig. 6

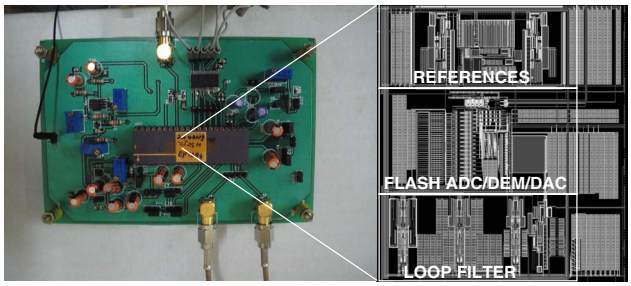

Fig. 6. Test board and chip layout.

shows the two-layer test board used for characterization and the layout of the integrated circuit. The die area is about $0.72\,\mathrm{mm}^2$. An Audio Precision (SYS-2722) differential signal source and a Tektronix AWG2021 clock source were used to characterize the ADC. Five million samples from the modulator output were captured using an Agilent 16500C Logic Analyzer. A 16K Blackman-Harris window was used for PSD computation.

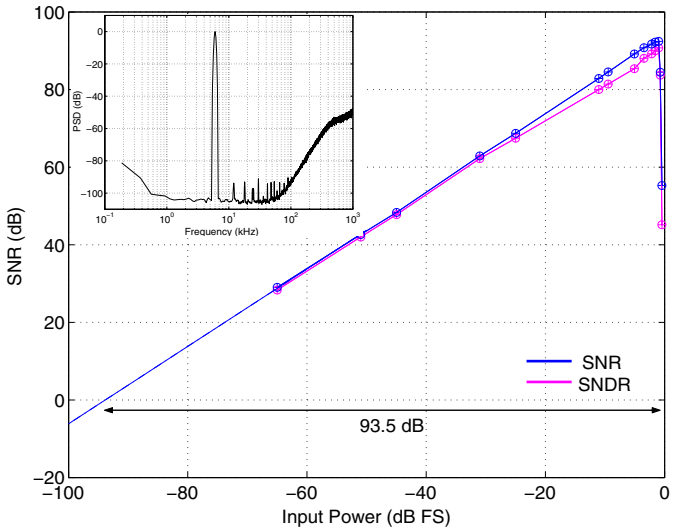

Fig. 7. Measured SNR and SNDR - the dynamic range is 93.5 dB.

Fig. 7 show the measured SNR and SNDR of the modulator. The peak SNR and SNDR are 92.5 dB and 90.8 dB respectively. The measured dynamic range of the modulator is 93.5 dB. Thanks to the four bit quantizer employed in the loop, the modulator is stable for signals as large as -0.7 dBFS. The harmonics are about 94 dB below the fundamental & no nonharmonic tones are observed above the noise floor. A

TABLE I

SUMMARY OF MEASURED ADC PERFORMANCE.

Signal Bandwidth/Clock Rate	24 kHz / 3.072 MHz
Quantizer Range	$3\,V_{pp,diff}$
Input Swing for peak SNR	-1 dBFS
Dynamic Range/SNR/SNDR	93.5 dB/92.5 dB/90.8 dB
Active Area	$0.72\,\mathrm{mm}^2$
Process/Supply Voltage	$0.18\,\mu$m CMOS/1.8 V
Power Dissipation (Modulator)	$90\,\mu$W
Power Dissipation (Modulator & Reference Buffers)	$121\,\mu$W
Figure of Merit	0.049 pJ/level

summary of measured performance is given in Table I. The figure of merit of the converter is determined as [1]

$$FOM = \frac{P}{2 \times f_B \times 2^{(DR-1.76)/6.02}} \quad (1)$$

where P, f_B and DR denote the power dissipation, signal bandwidth & dynamic range respectively. Our converter achieves 0.049 pJ/level.

TABLE II

COMPARISON WITH OTHER CT-$\Sigma\Delta$ MODULATORS

Reference / Bandwidth	Technology	Dynamic Range	Power	FOM (pJ/level)
[1]/25 kHz	$0.35\,\mu$m	80 dB	$135\,\mu$W	0.25
[2]/25 kHz	$0.35\,\mu$m	81 dB	$250\,\mu$W	0.45
[4]/20 kHz	$0.35\,\mu$m	106 dB	18 mW	2.788
[5]/20 kHz	65 nm	95 dB	2.2 mW	1.196
[7]/3.4 kHz	$0.50\,\mu$m	80 dB	$210\,\mu$W	3.77
This work / 24 kHz	$0.18\,\mu$m	93.5 dB	$90\,\mu$W	0.049

Table II compares the performance of several continuous-time modulators presented in the literature with the ADC presented in this work. Thanks to the proposed architectural and circuit techniques, this work achieves the lowest energy per level of resolution when compared with the implementations reported in the literature.

V. CONCLUSIONS

We presented the design a 15-bit low power continuous-time $\Delta\Sigma$ converter for digital audio. Using a multibit quantizer and large signal swings results in improved power efficiency. An active-RC loop filter with class-AB opamps and a resistive feedback DAC were chosen to reduce noise & power dissipation. The effect of parasitic poles in the loop filter were mitigated by using a new excess delay compensation technique. These techniques were applied to the design of an audio frequency third order CTDSM implemented in a $0.18\,\mu$m CMOS technology. The ADC has a measured dynamic range of 93.5 dB while dissipating $90\,\mu$W from a 1.8 V supply.

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