A 16MHz BW 75dB DR CT ΔΣ ADC Compensated for More Than One Cycle Excess Loop Delay

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Motivation

Maximize the signal bandwidth of a continuous-time ΔΣ modulator in a given process technology

- SQNR increases with order, OBG
  - For low OSR, SQNR doesn't increase much with order
  - OBG limited to ~ 3 by stability considerations
- $\Rightarrow$ Sampling rate (OSR) must be increased
  - Shorter sampling period
  - Process sets a lower limit on ELD
  - ELD can exceed the sampling period

Need a way to compensate ELD exceeding the sampling period

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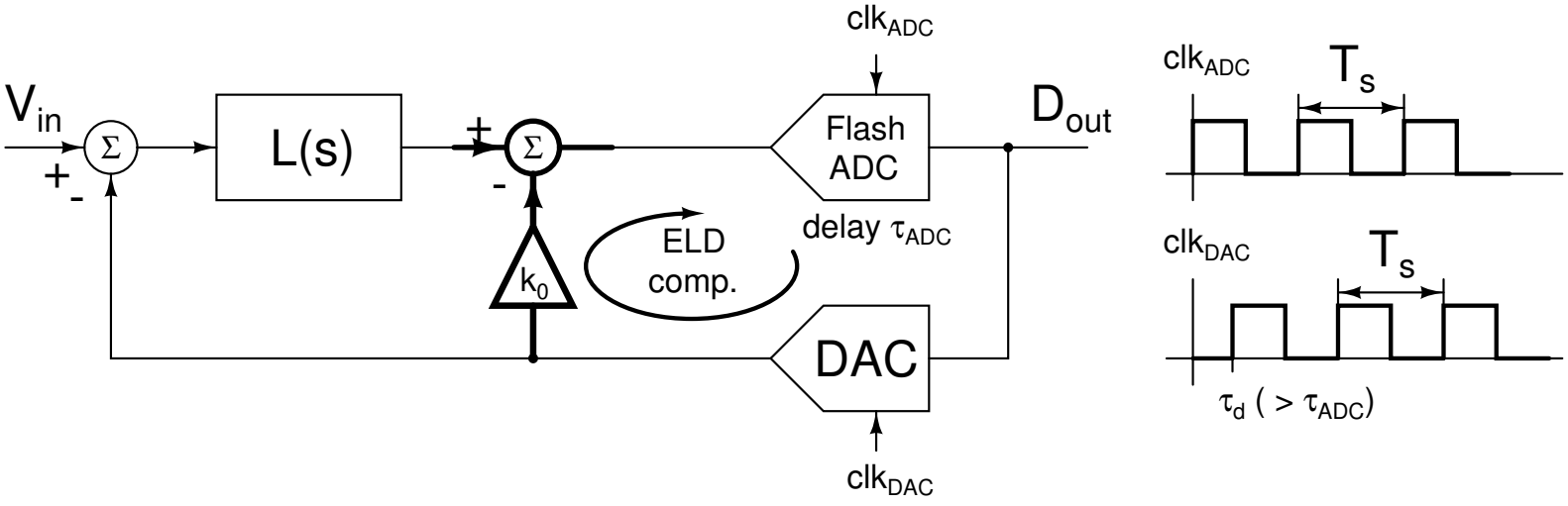
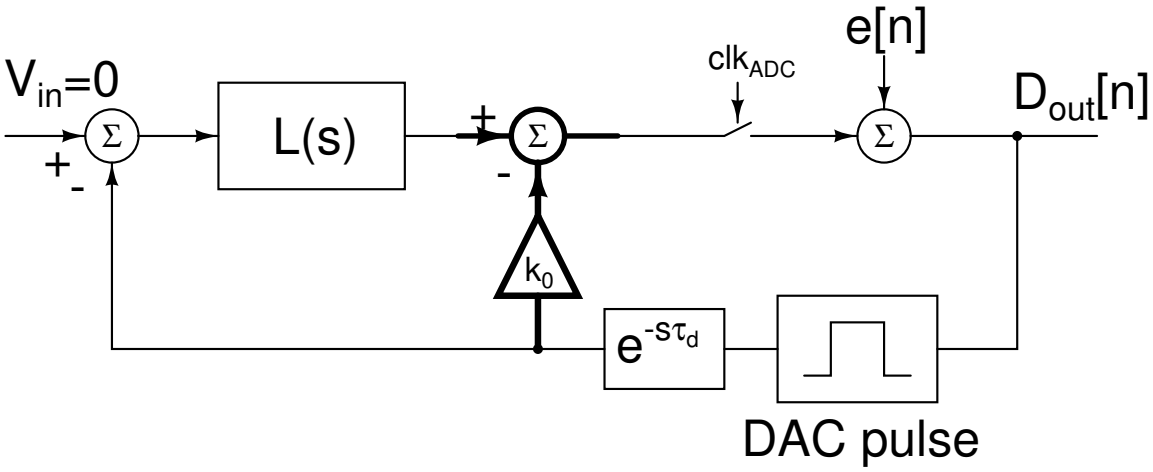
Outline

- Principle
  - Speed limit of CT $\Delta\Sigma$ modulators
  - Compensating ELD greater than a clock period
  - Simulation results
- 800 MHz $\Delta\Sigma$ modulator in a 0.18 μm process
  - Architecture
  - Circuit details
  - Simulation results
- Measured results
- Conclusions

$\Delta\Sigma$ *modulator with ELD compensation*



Noise transfer function (NTF)



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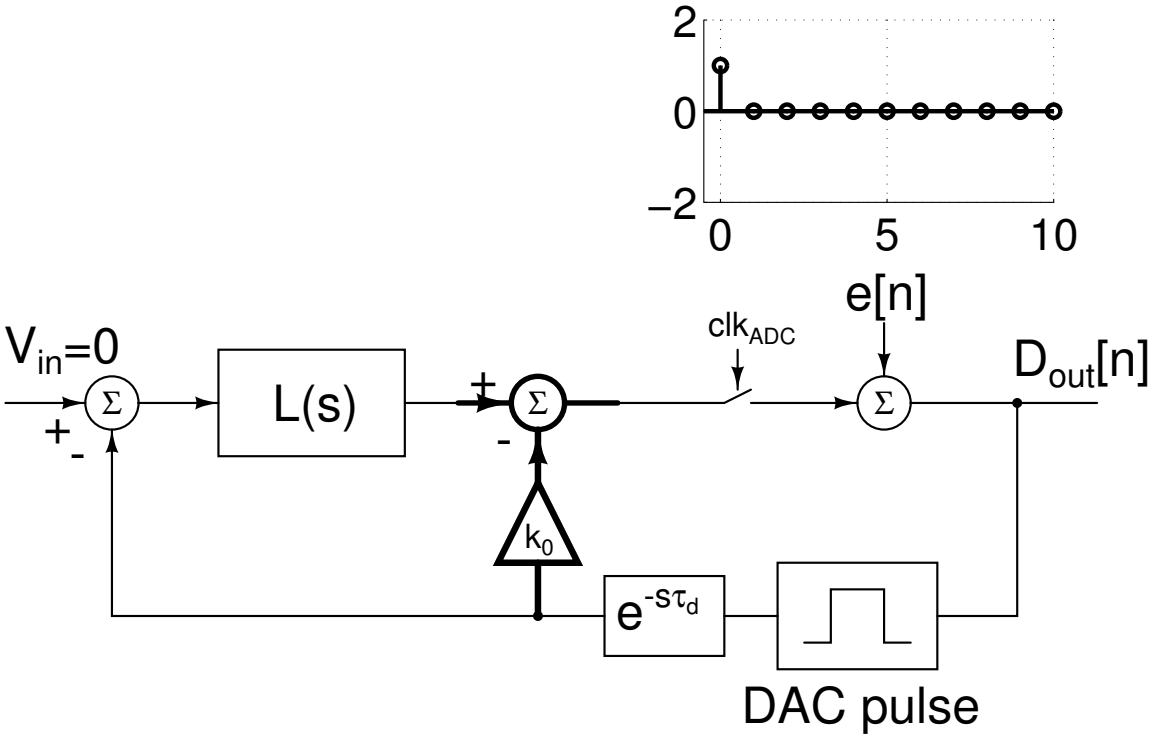

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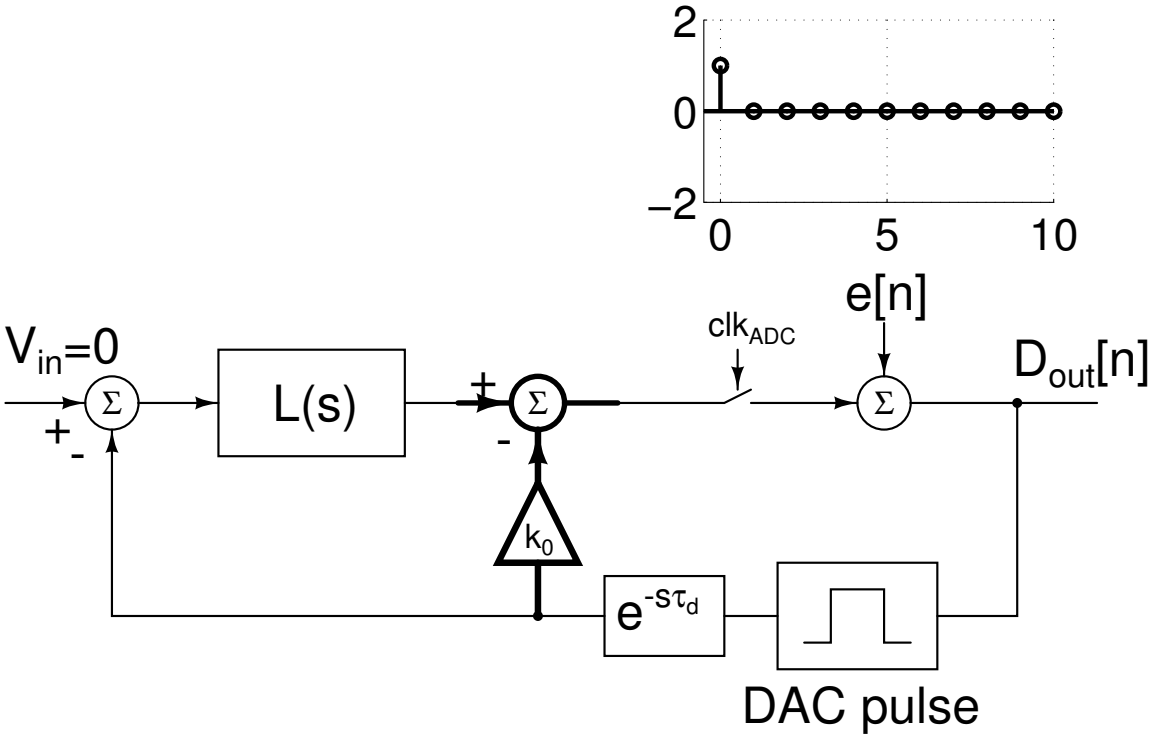
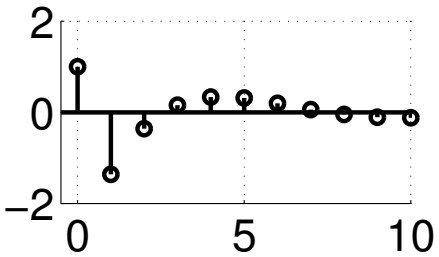
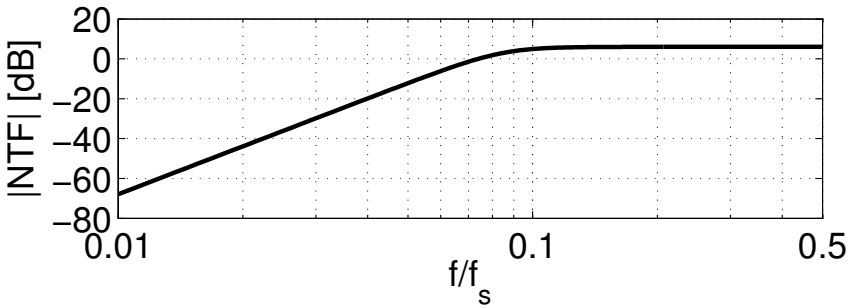
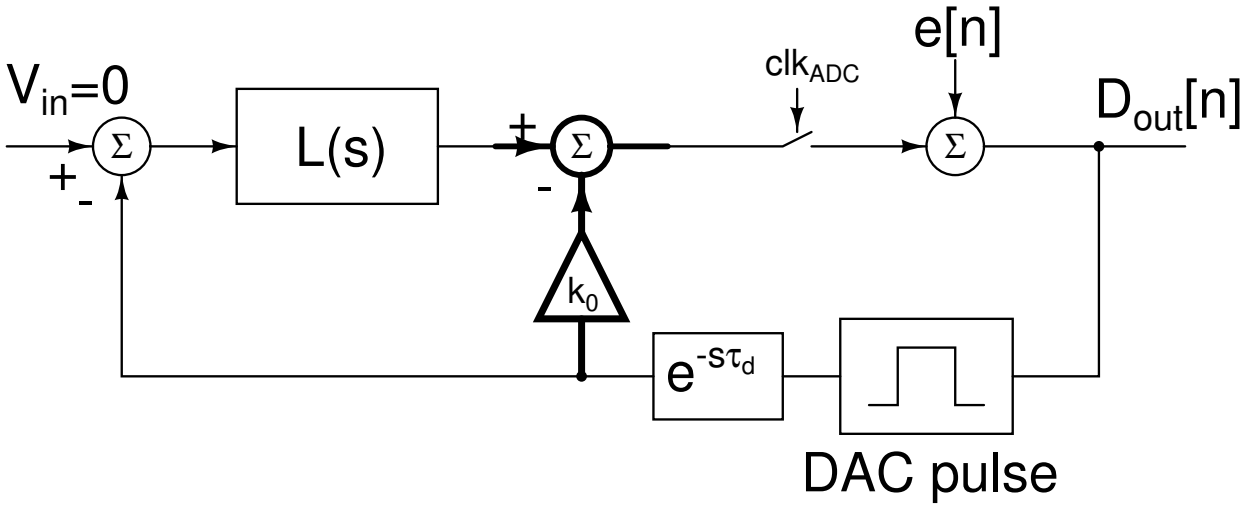






Limits on ELD compensation



- k_0 contributes nothing to $h_{NTF}[1]$ if ELD $> T_s$
- In practice, only ELD $< T_s/2$ can be compensated
- ELD $\geq \tau_{ADC} \geq \tau_{ADC,min}$
- **Highest sampling rate is** $\sim 1/2\tau_{ADC,min}$

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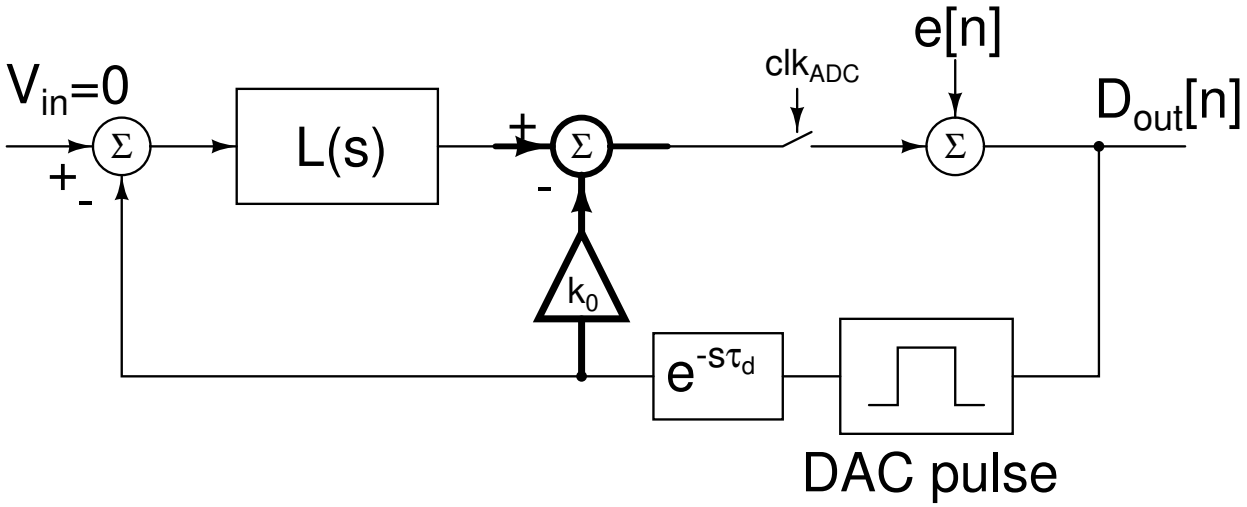

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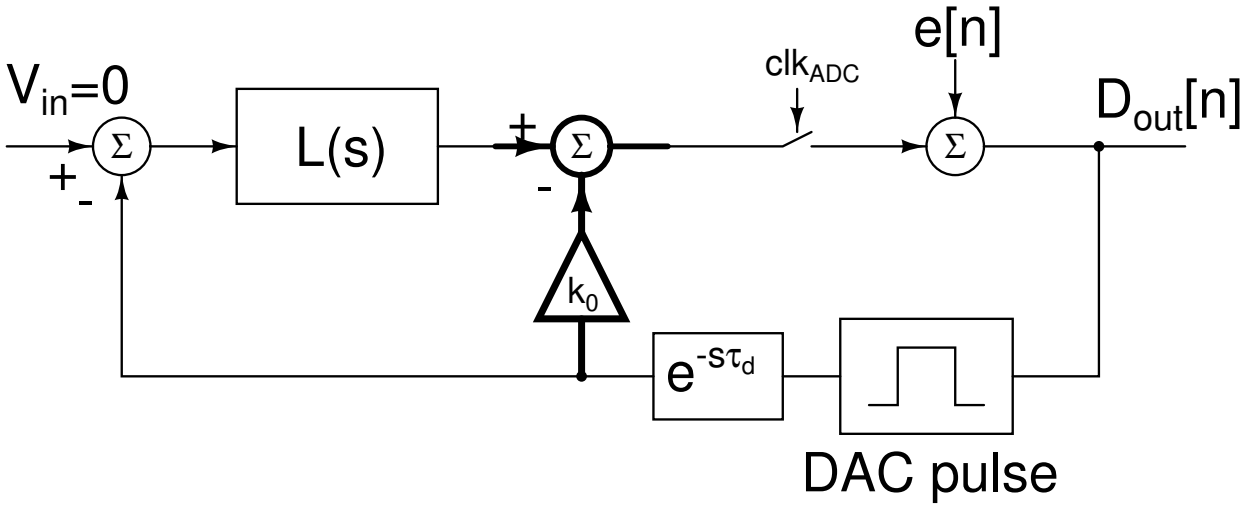

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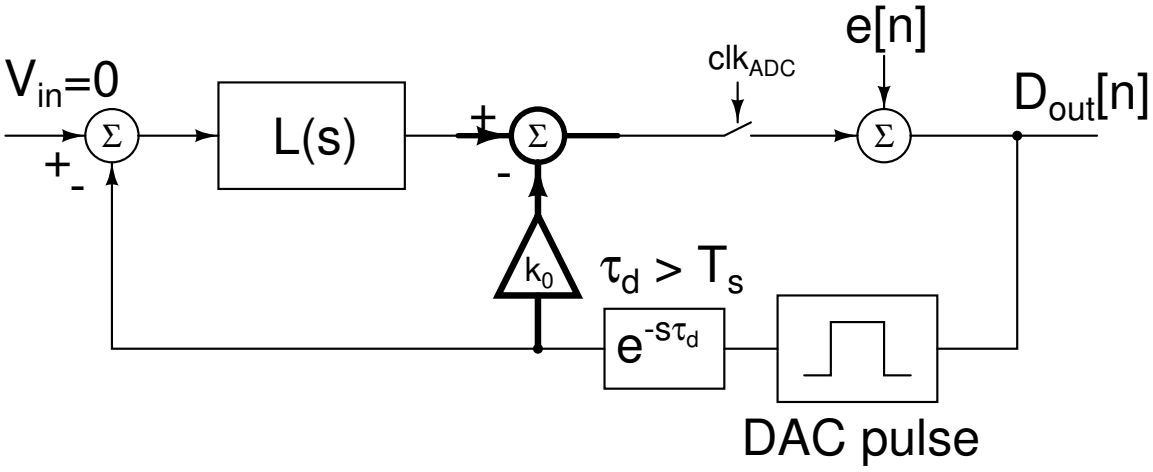
Conventional compensation for ELD $> T_s$



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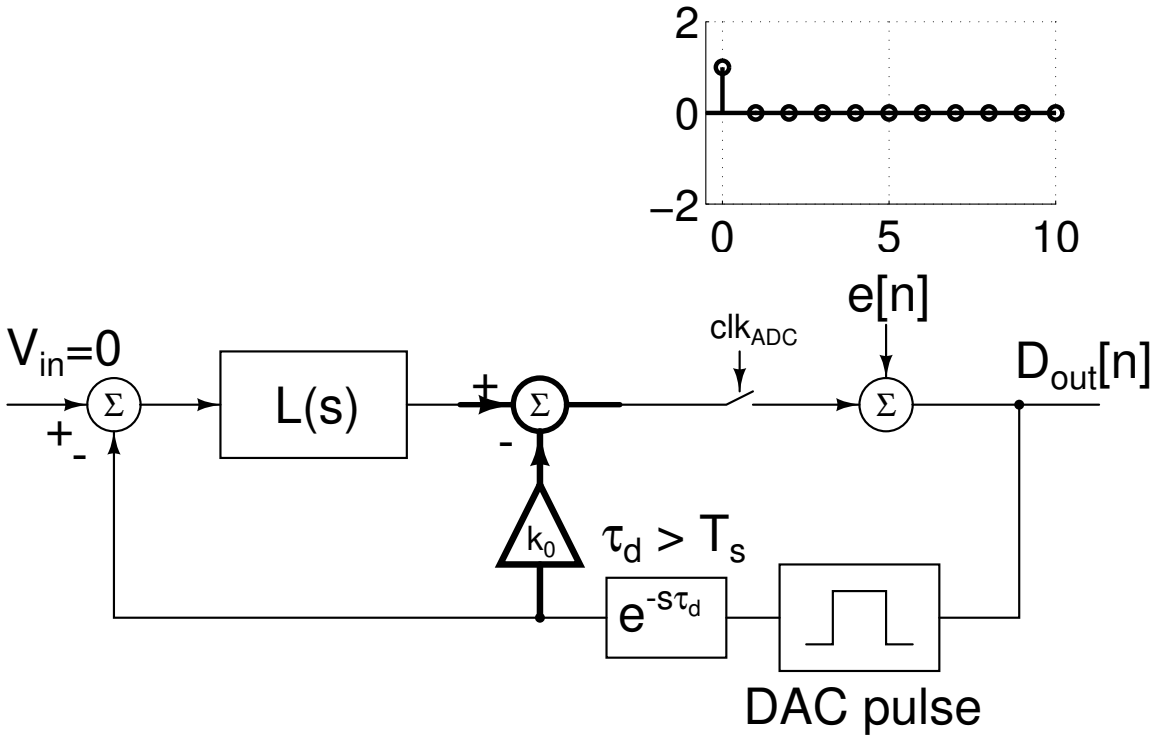

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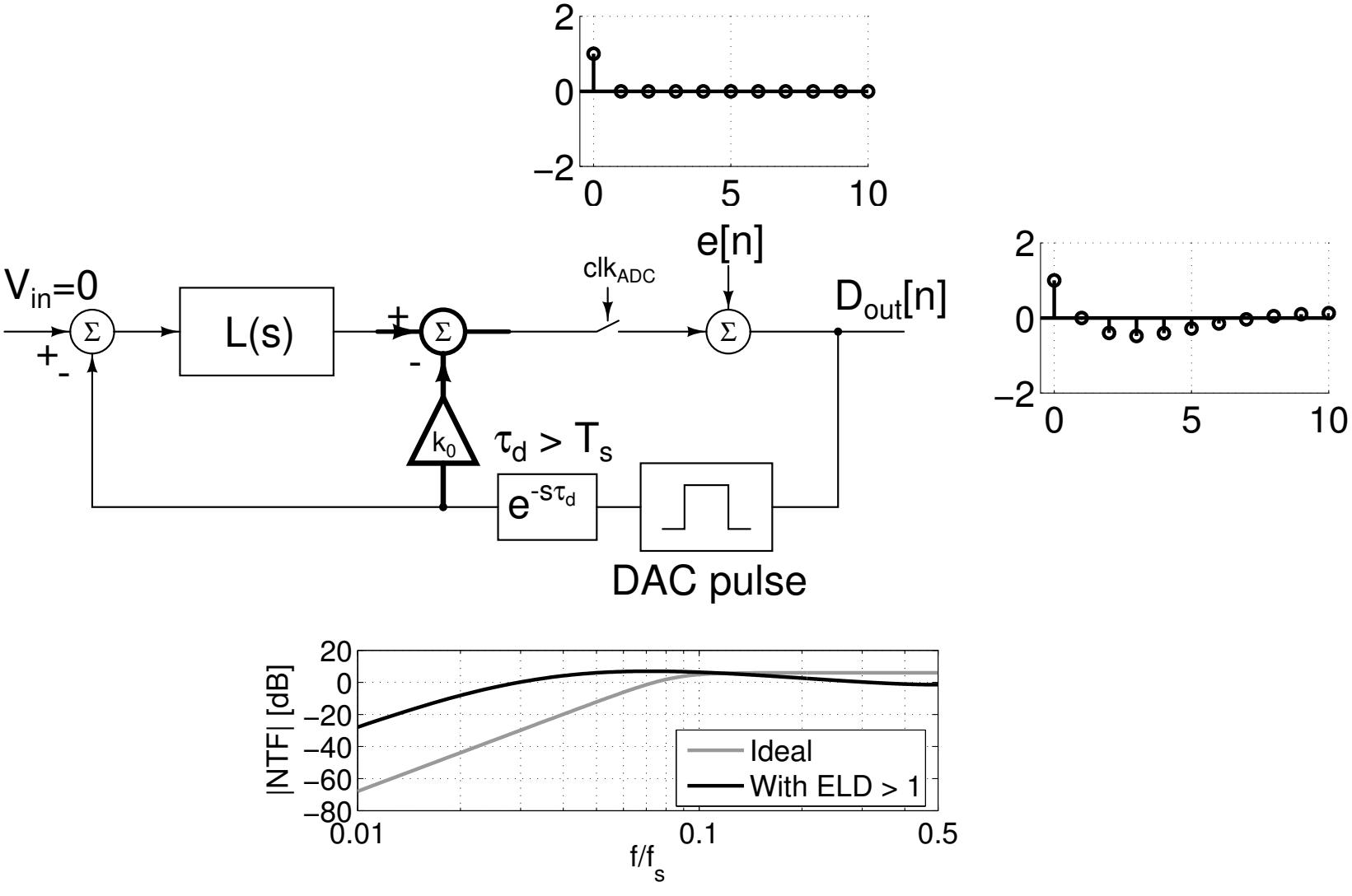


Stable conventional CTDSMs with ELD > T_s

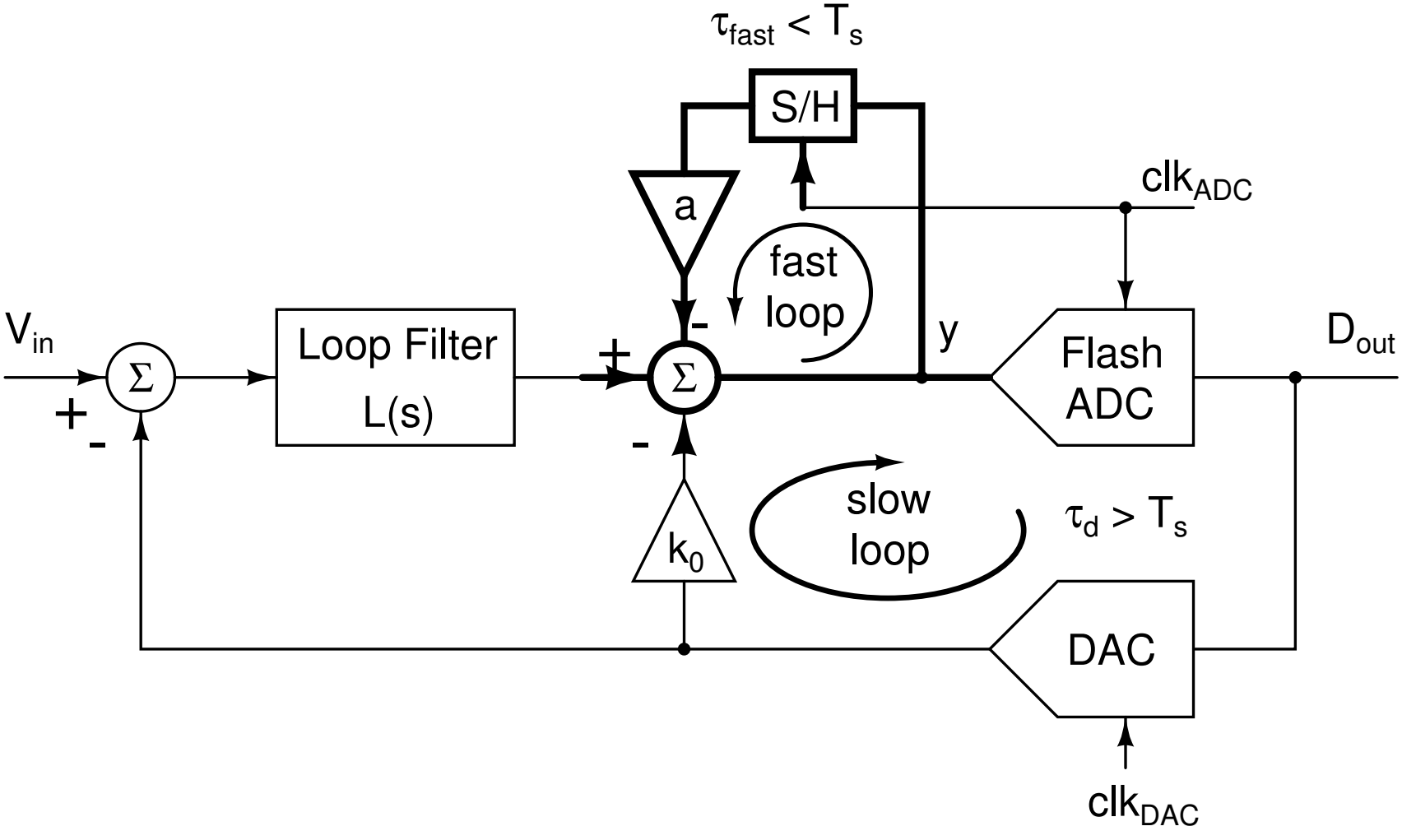
- For a stable, minimum phase NTF with $h_{NTF}[1] = 0$

$$\int_0^{\pi} \log \left| \text{NTF}\left(e^{j\omega}\right) \right| \cos(\omega) d\omega = 0$$

- $\Rightarrow$ Good NTFs for lowpass modulators cannot be realized with $h_{NTF}[1] = 0$

- J. Harrison and N. Weste, “Analytic limitations on sigma-delta modulator performance,” *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 3, 2000, pp. 746-749.

Fast loop outside the ADC



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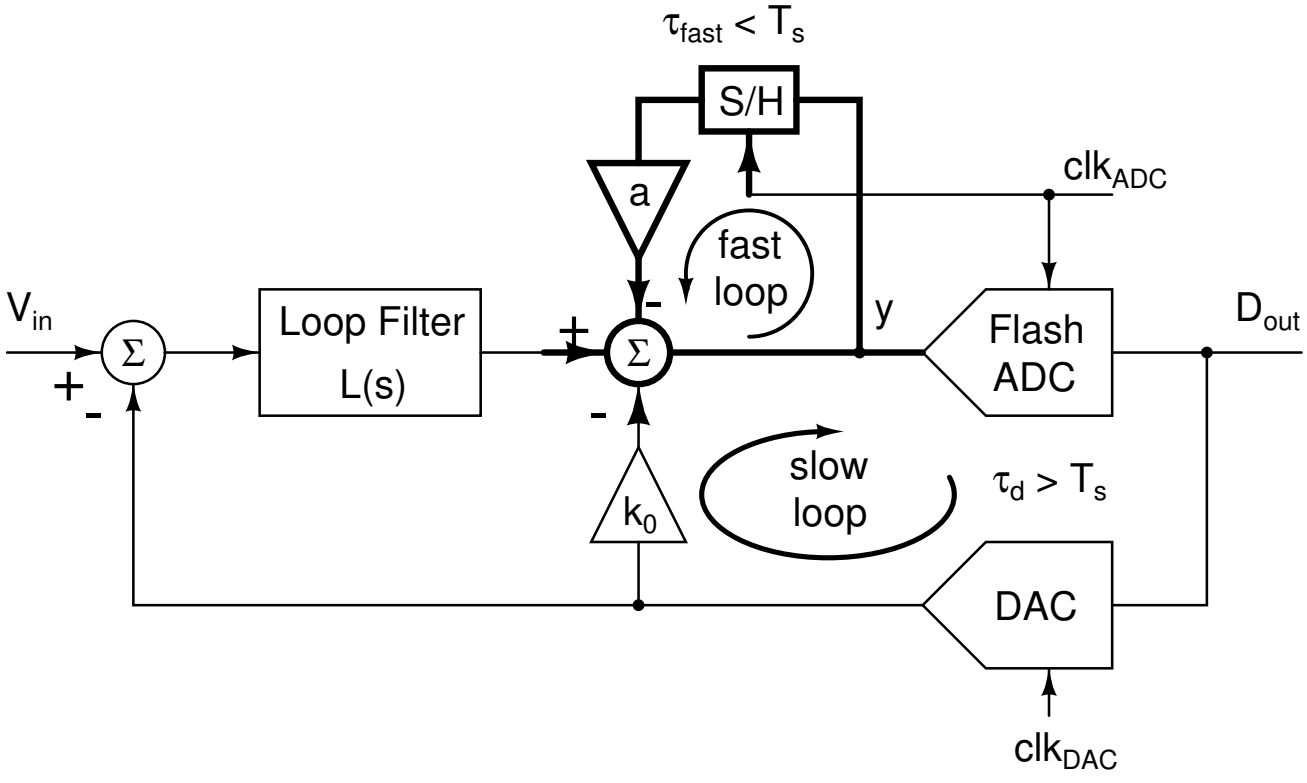

- A. Yahia et al., “Bandpass delta-sigma modulators synthesis with high loop delay,” *Proc. IEEE ISCAS*, vol. 1, 2001, pp. 344-347.
- V. Singh et al., “Compensating for quantizer delay in excess of one clock cycle in Continuous-Time ΔΣ Modulators,” *IEEE Transactions on Circuits and Systems: Part II Express Briefs*, vol. 57, no. 9, pp. 676-680, Sep. 2010.

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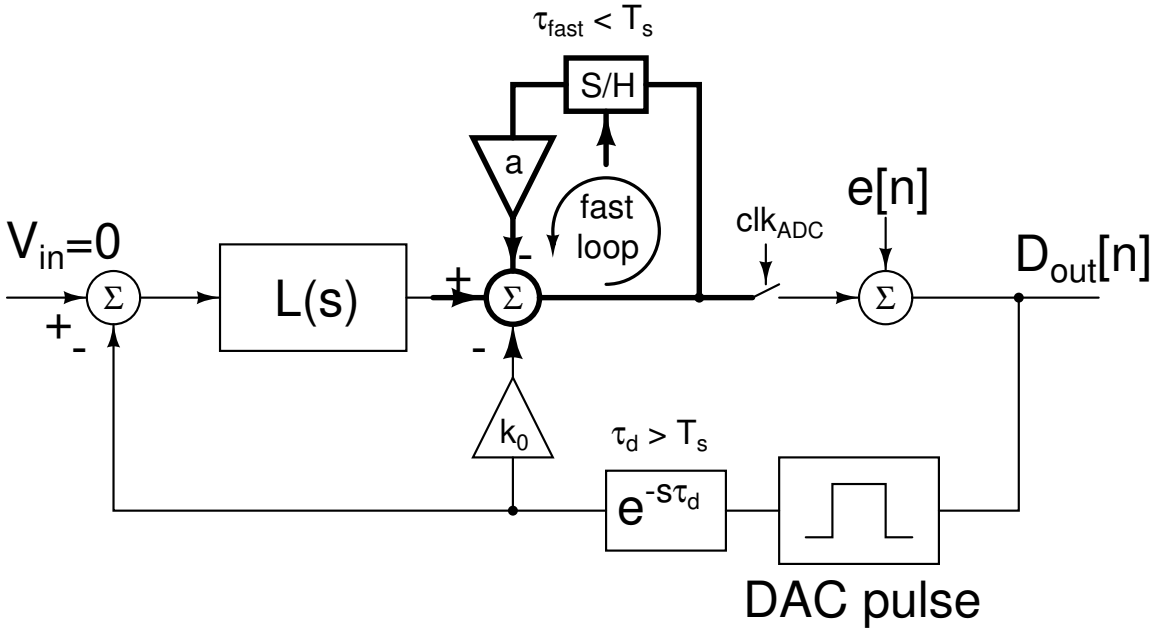

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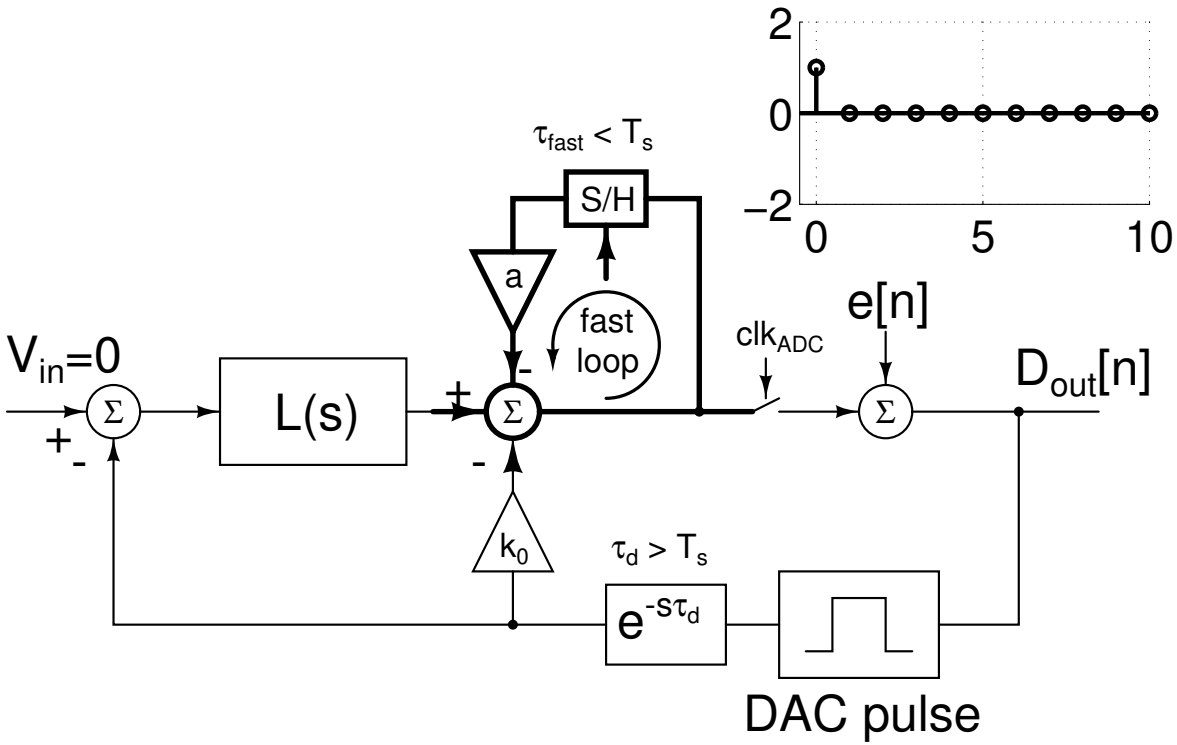

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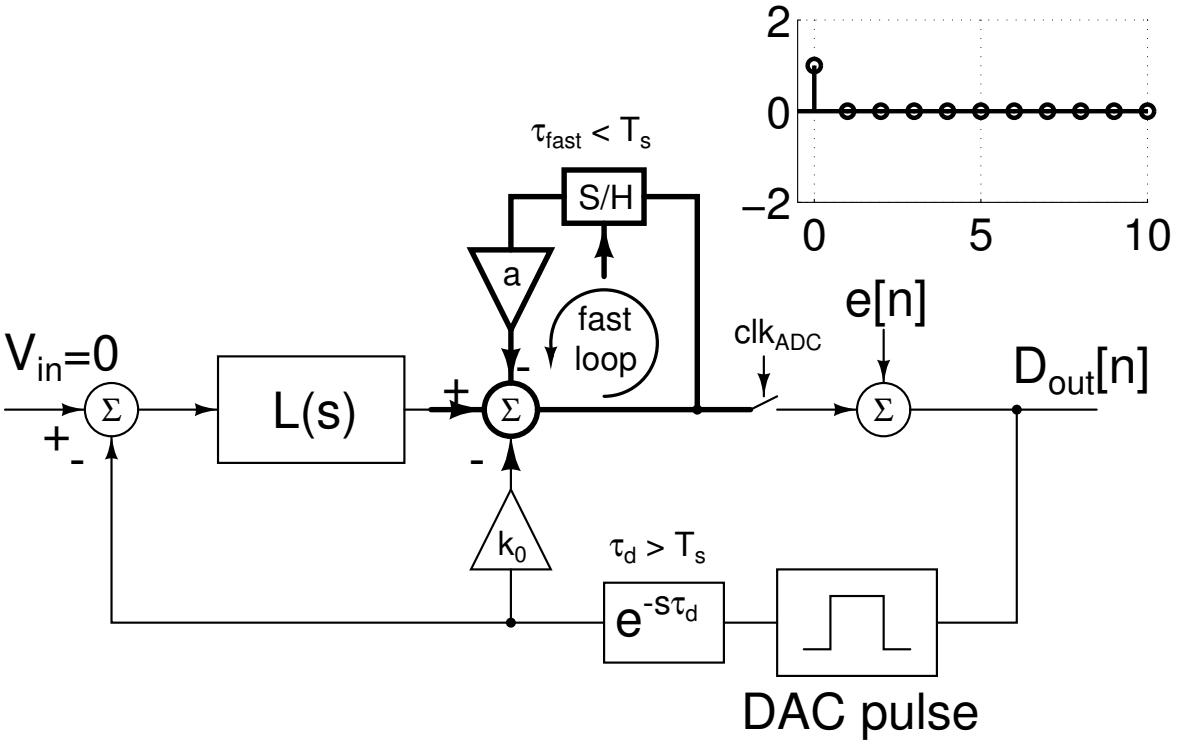

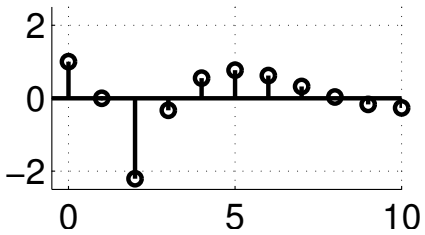

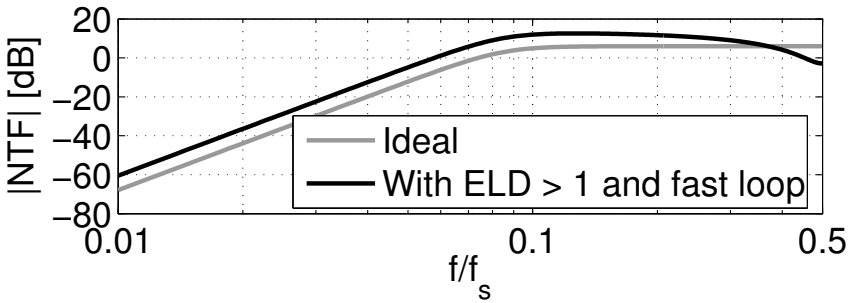

NTF with the fast loop outside the ADC

$$\mathrm{NTF}_{new}(z) \quad = \quad \left(1 + az^{-1}\right) \mathrm{NTF}_{orig}(z)$$

- NTF_{new} has a zero at $a > 1$ (outside the unit circle)
- Not a minimum phase NTF
- Demands an increase in order by 1

ELD compensation using a fast path outside the ADC

Path k_0

- ELD $\leq T_s/2$ compensated by k_0
- ELD $\geq \tau_{ADC,min}$
- $f_{s,max} \sim 1/2\tau_{ADC,min}$

Fast loop and path k_0

- ELD $\leq T_s/2$ compensated by k_0
- ELD $= T_s$ compensated by fast path
- ELD $= 3T_s/2$ compensated in total
- ELD $\geq \tau_{ADC,min}$
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$f_{s,max}$ can be increased by $3\times$ in a given process

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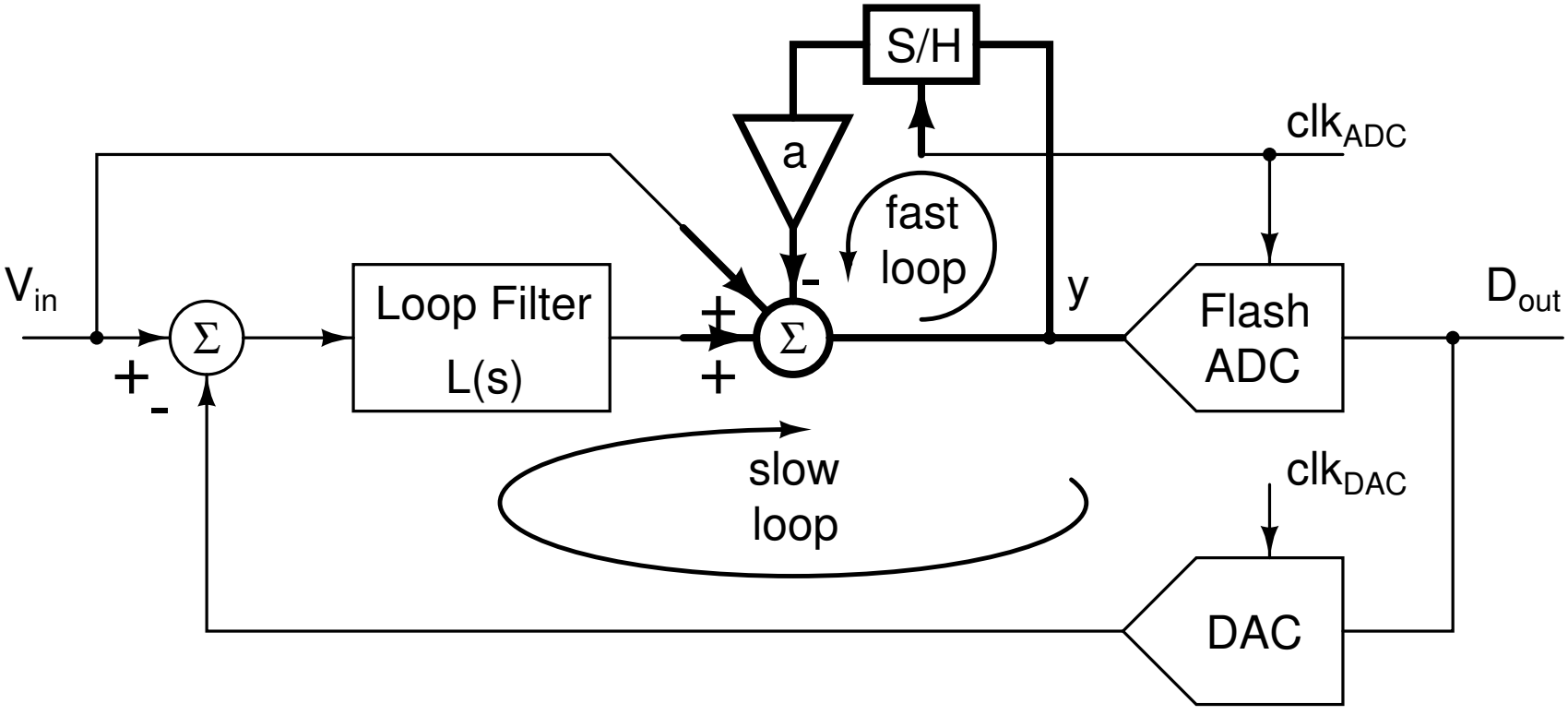
800 MHz $\Delta\Sigma$ modulator in a 0.18 μm process

- Architecture
- Loop filter
- Flash ADC
- Feedback DAC
- Simulation results

Prototype DSM architecture

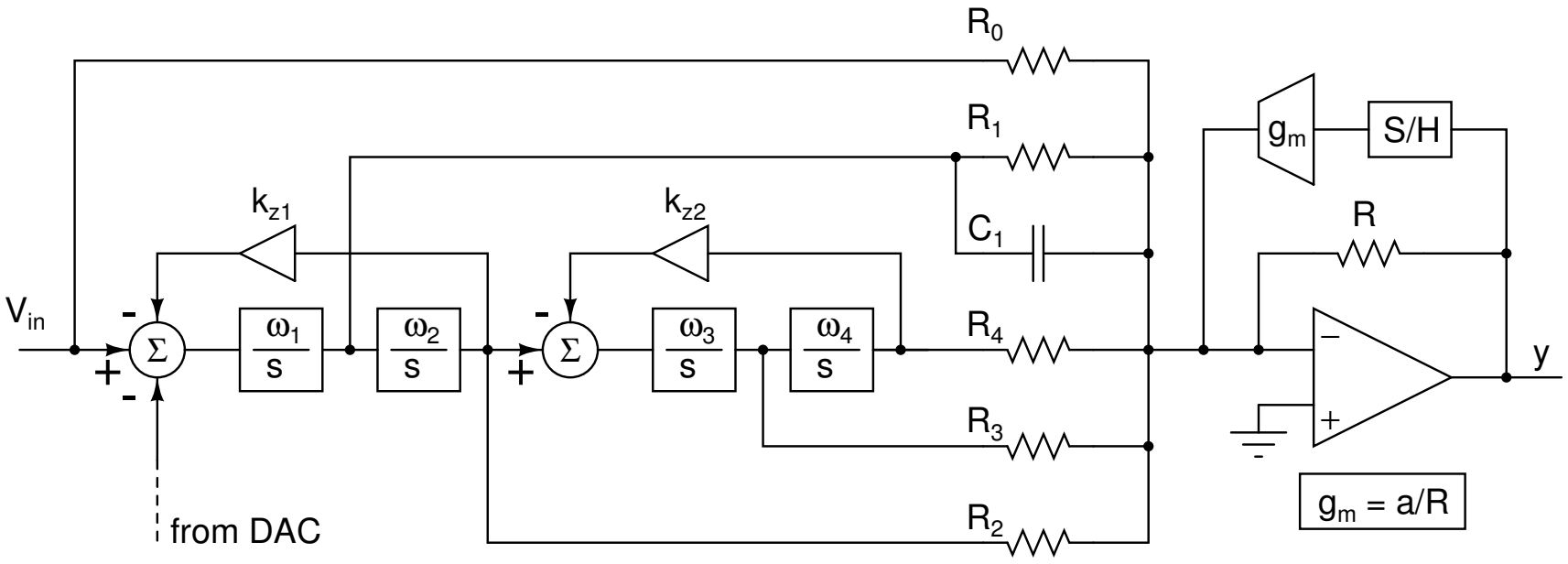
- 0.18 μm CMOS, 1.8 V supply
- Fourth order NTF_{orig}
  - OBG=2
  - Fast loop outside ADC
  - Optimized zeros
  - SQNR = 98 dB with OSR = 25
- $f_s = 800$ MHz; BW = 16 MHz
- CIFF loop filter
- 4 bit flash ADC with $3\,V_{ppd}$ full scale
- Calibrated current steering DAC

DSM block diagram



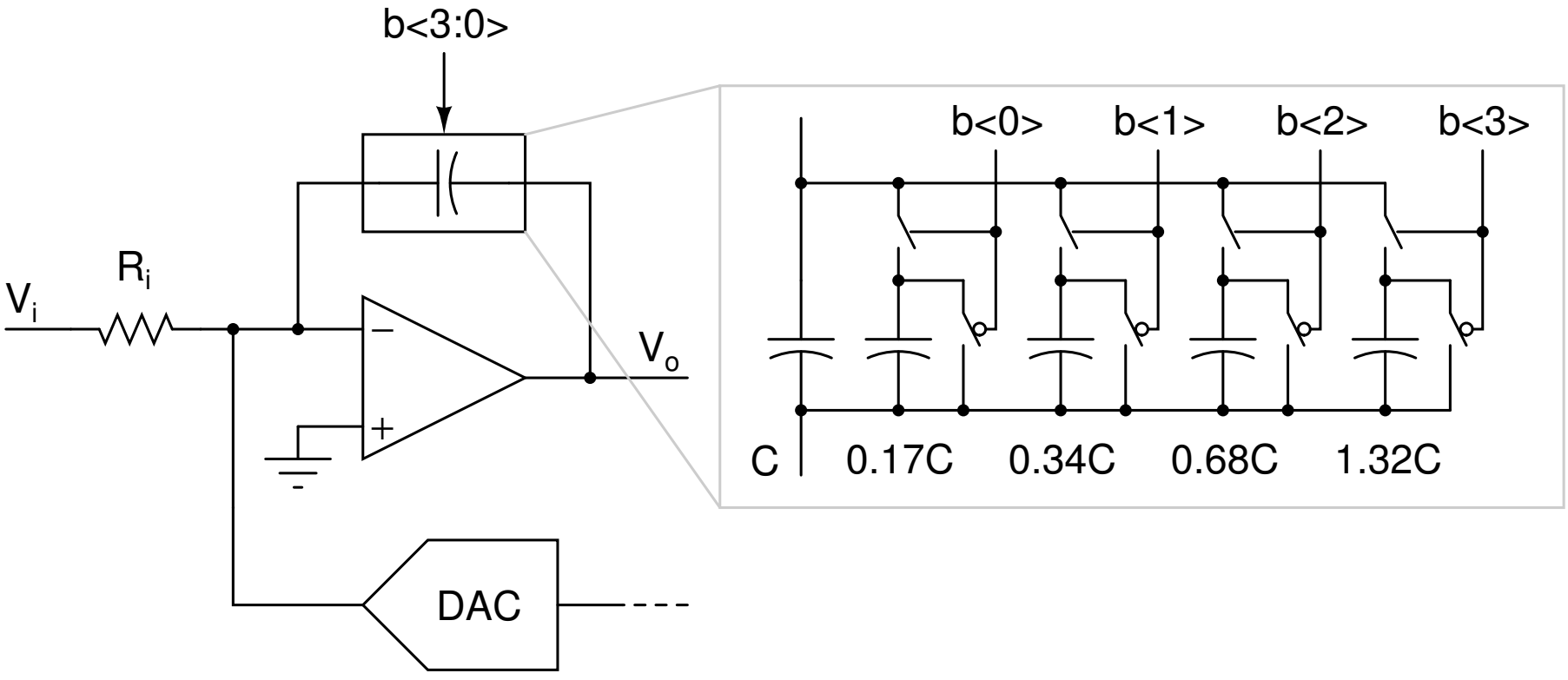
- Feedforward summation of input signal—reduces summing amplifier coefficients

Loop filter



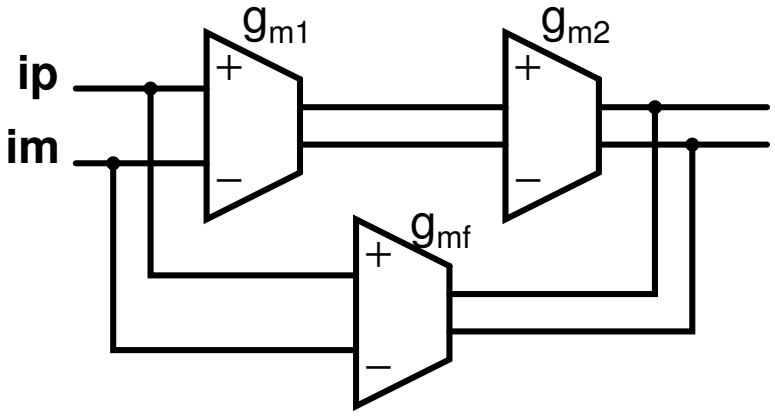
- Active-RC for linearity
- Fast path—S/H and g_m around the summing opamp
- k_0 inside the loop filter
- Integrator output swings scaled down to 0.8 V_{ppd}

Integrator



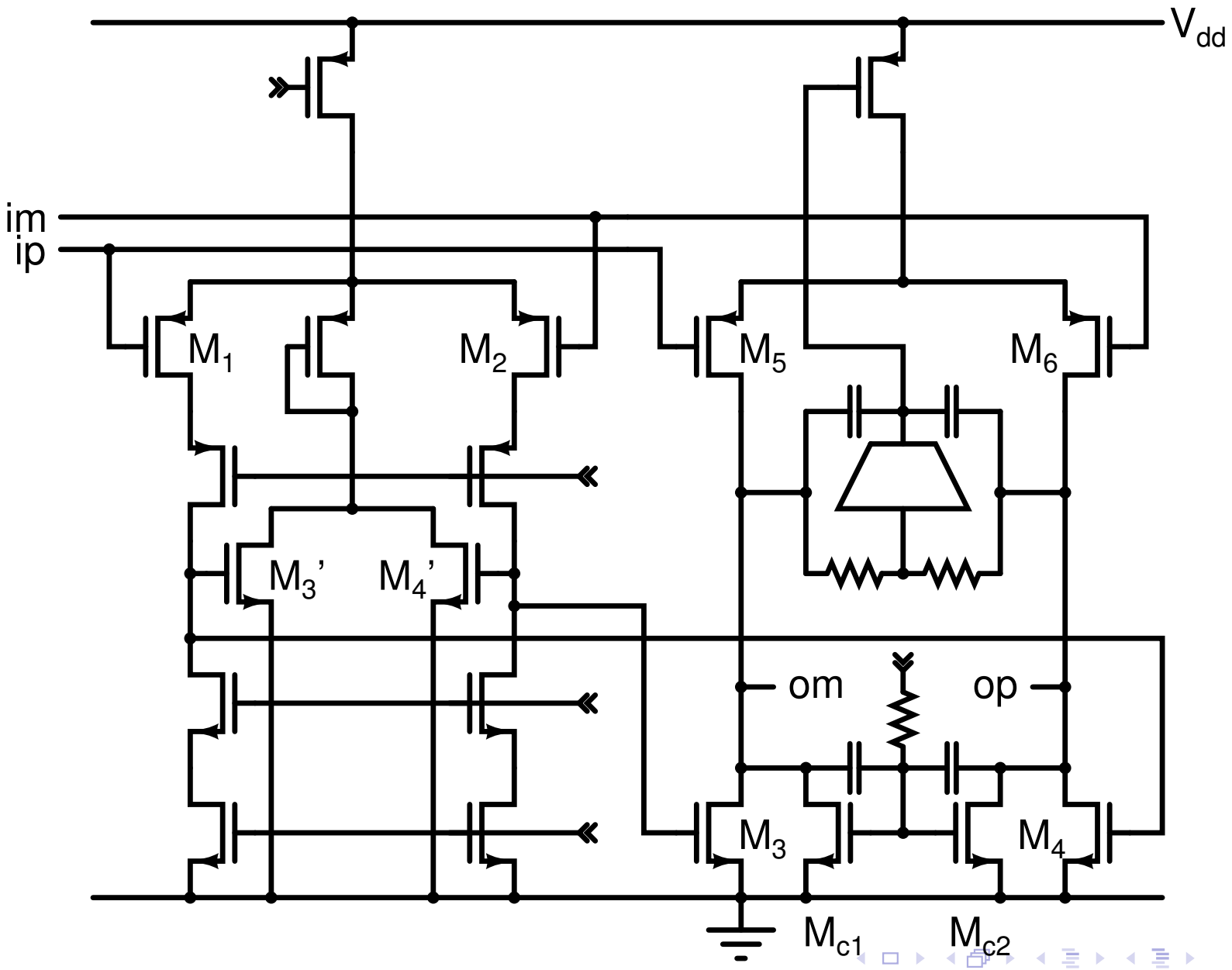
- 4 bit programmable time constant

First opamp

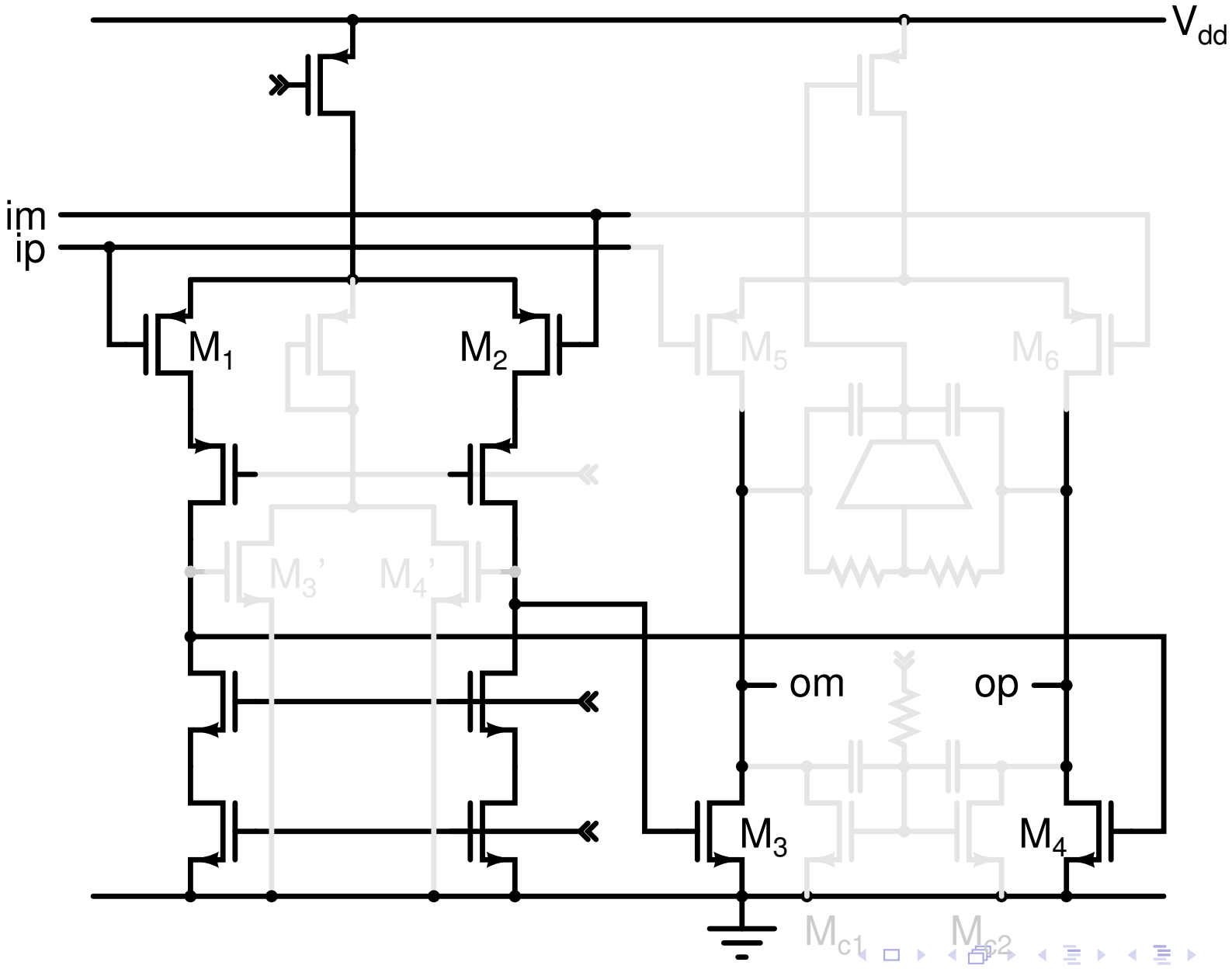


- Feedforward compensated opamp

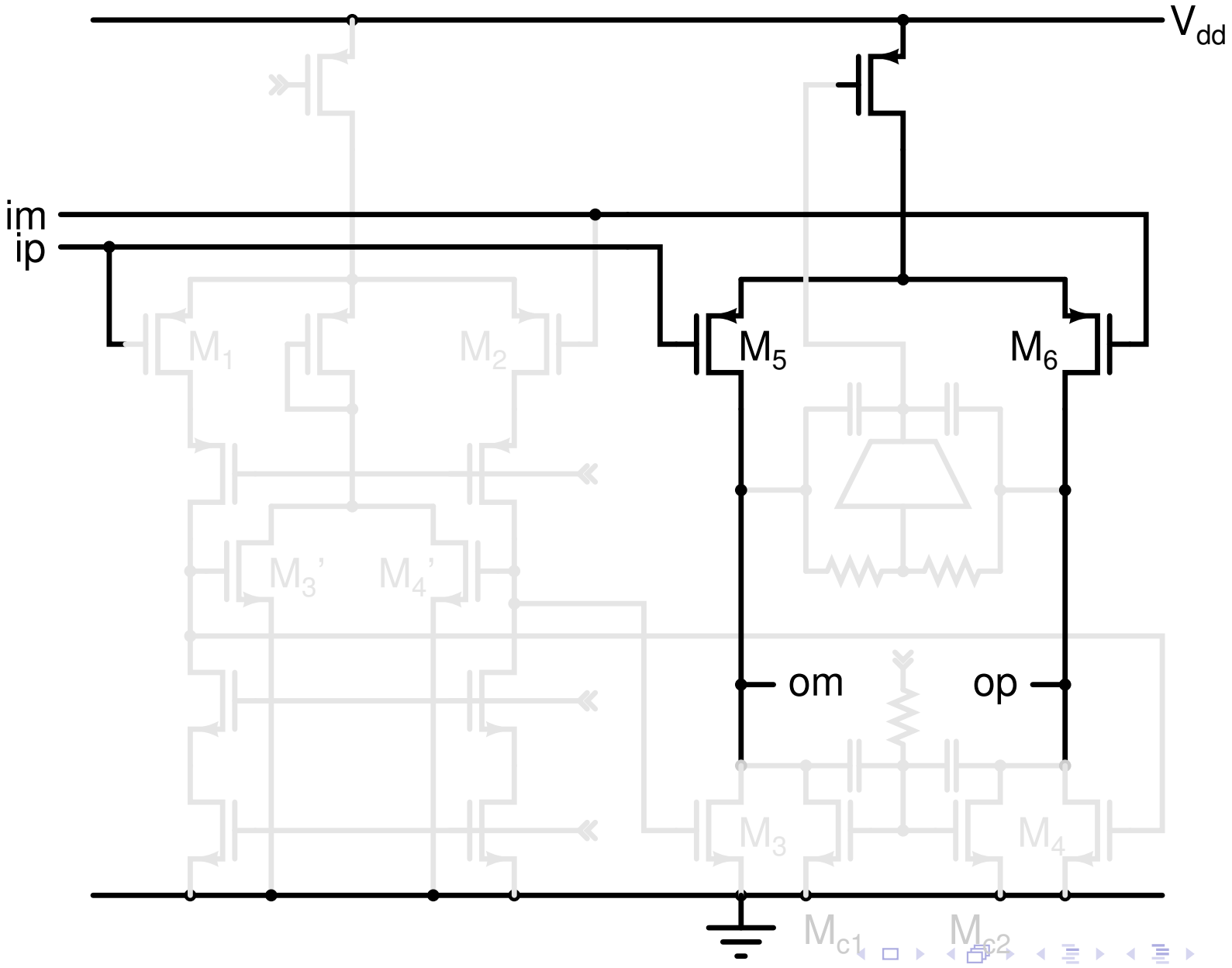
First opamp



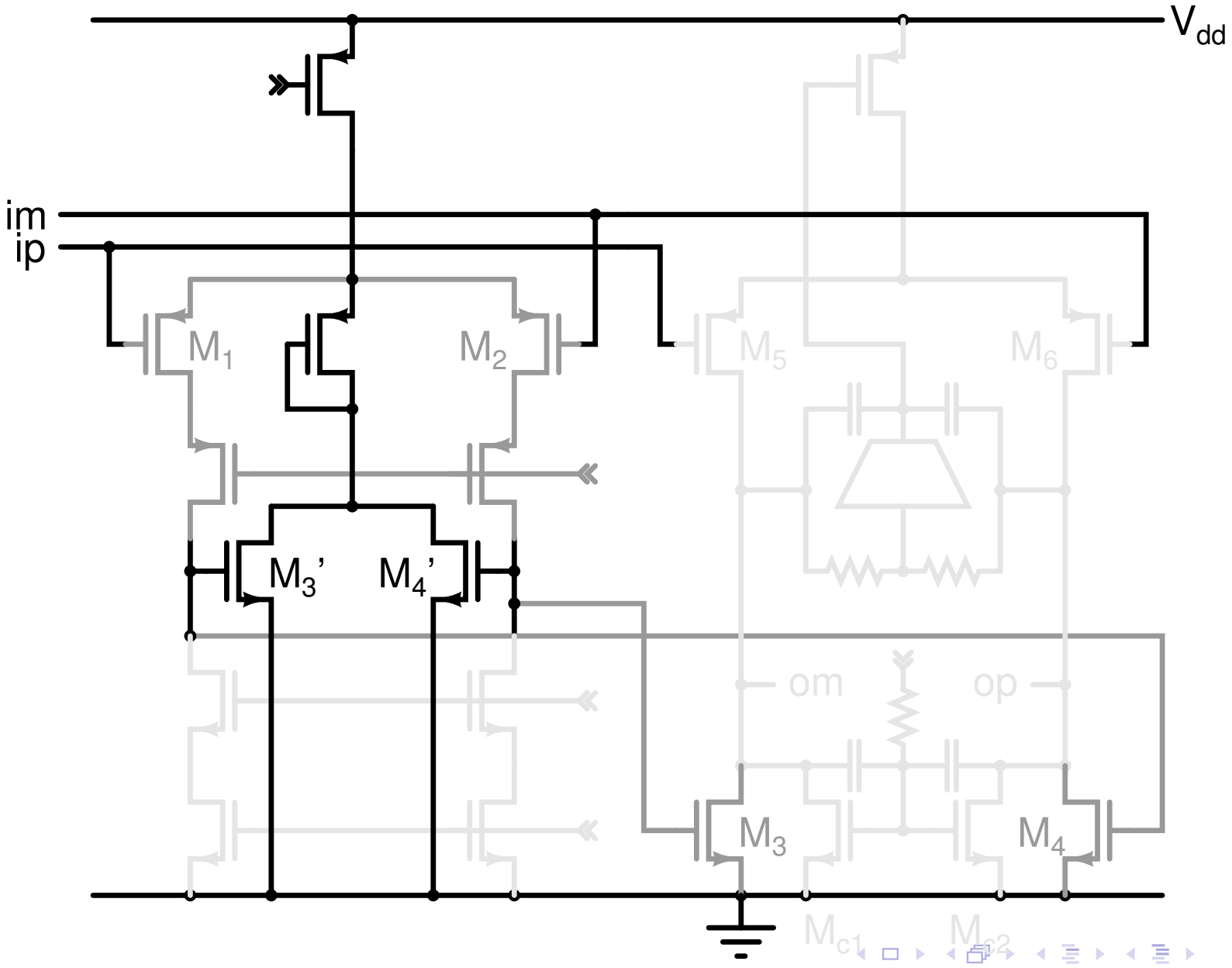
First opamp—Gain stages



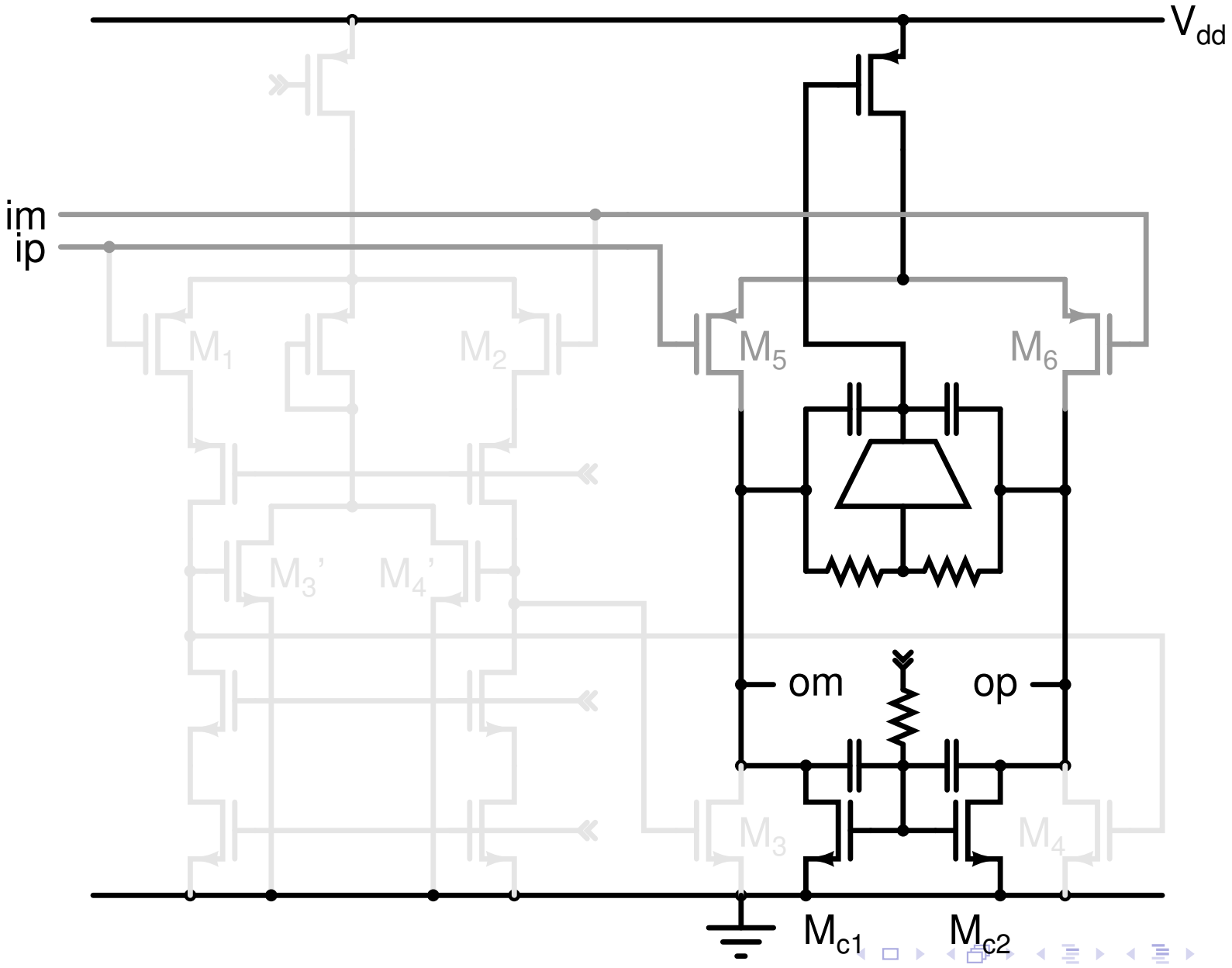
First opamp—Feedforward stage



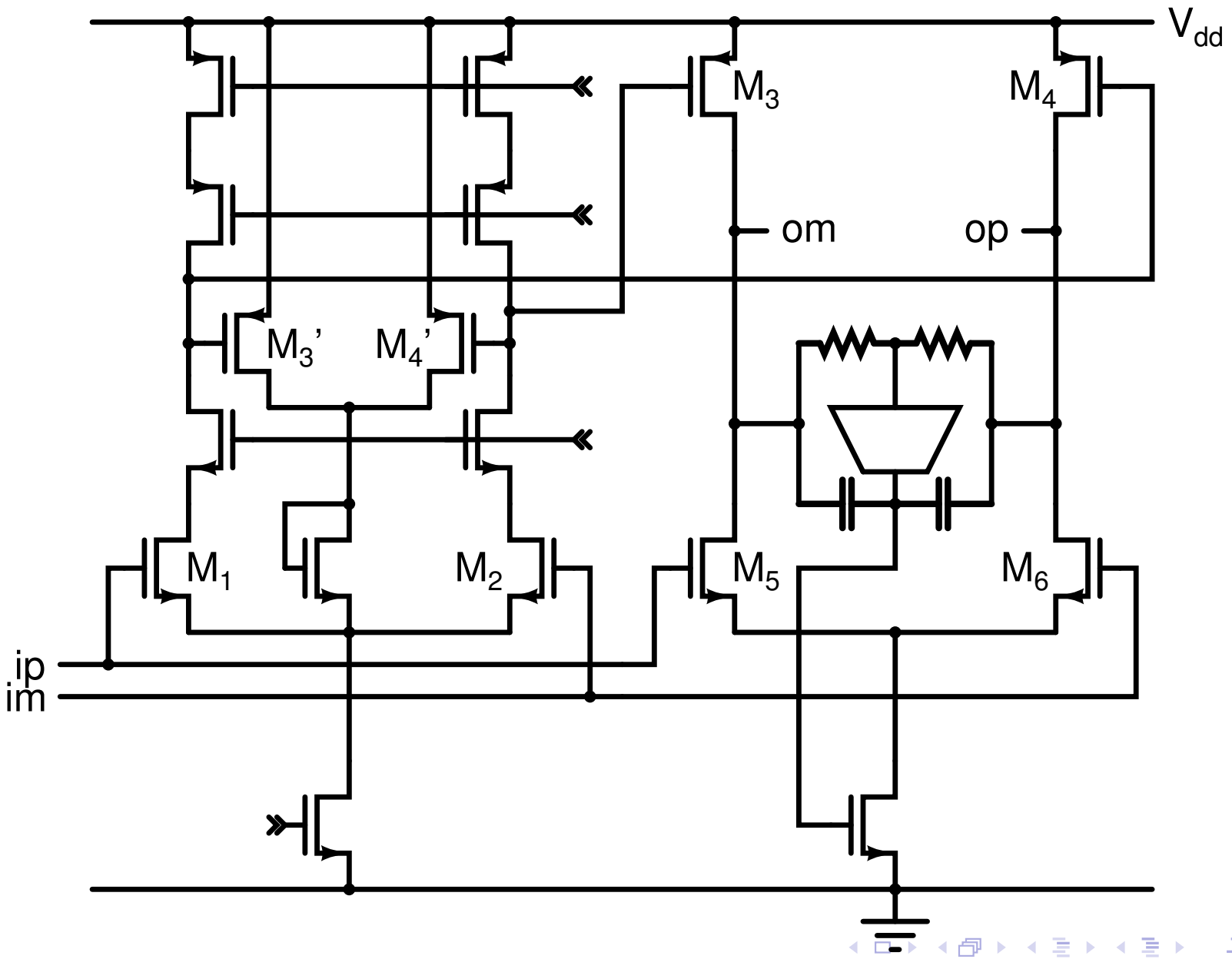
First opamp—First stage CMFB



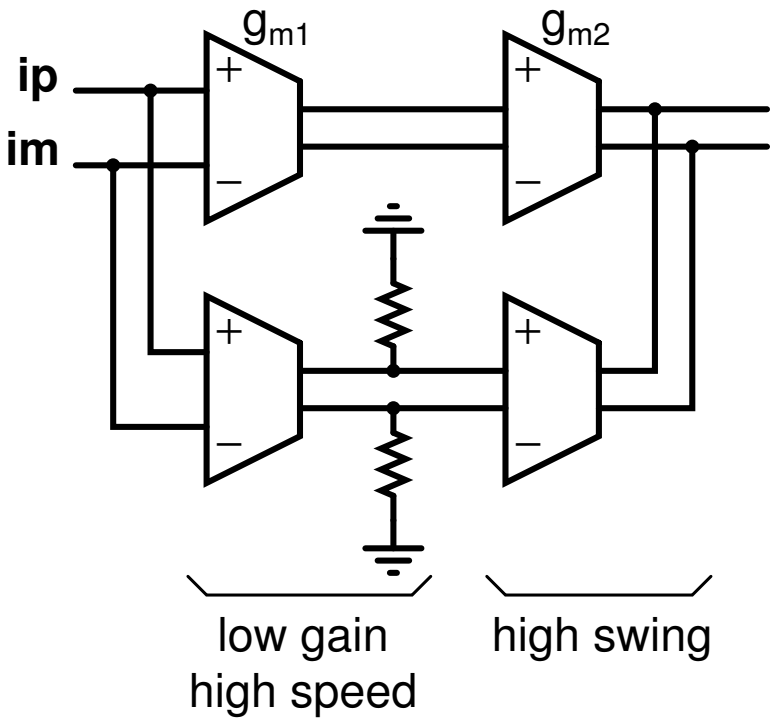
First opamp—Second stage CMFB



Second, third, and fourth opamps

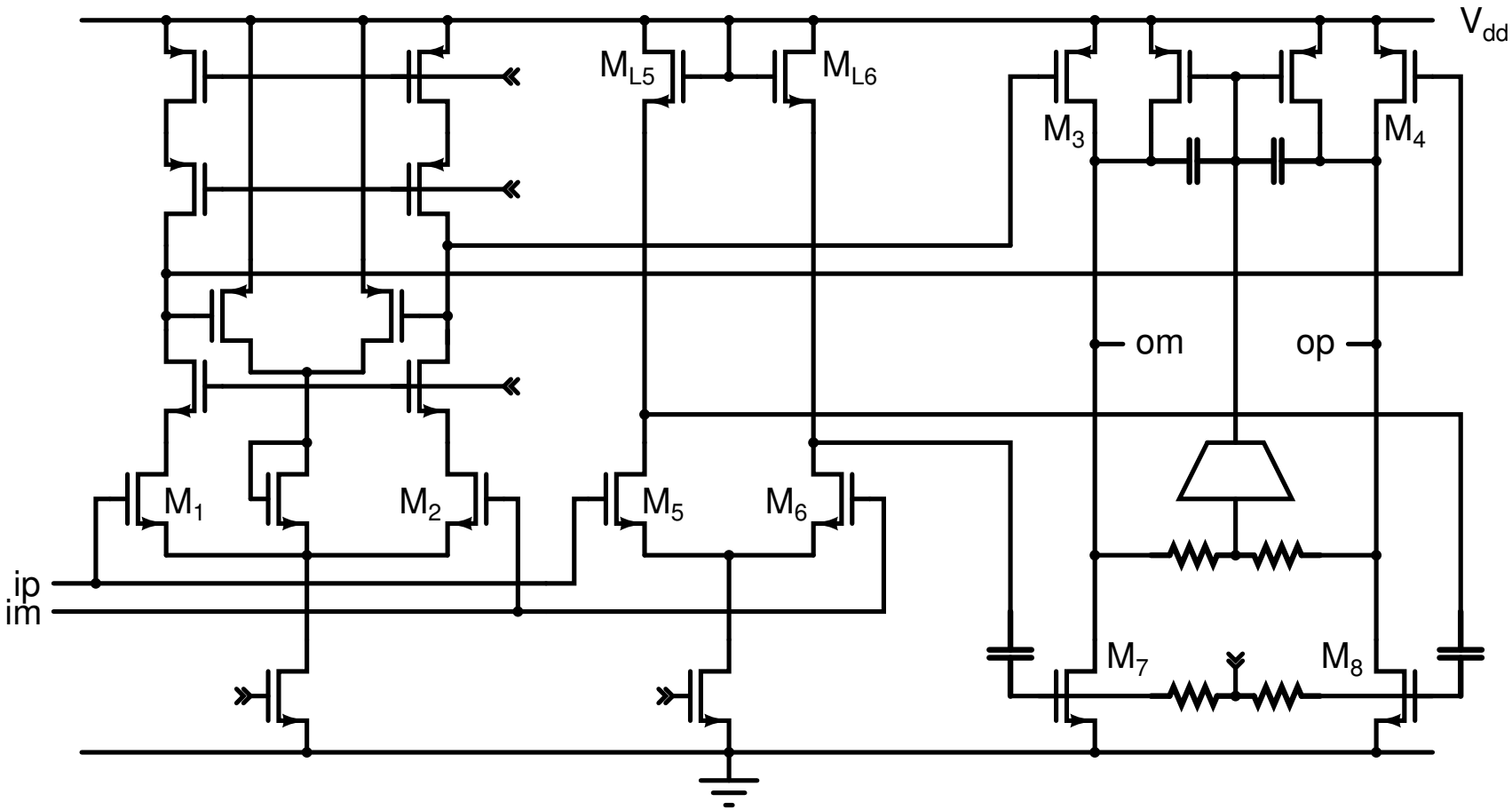


Summing opamp

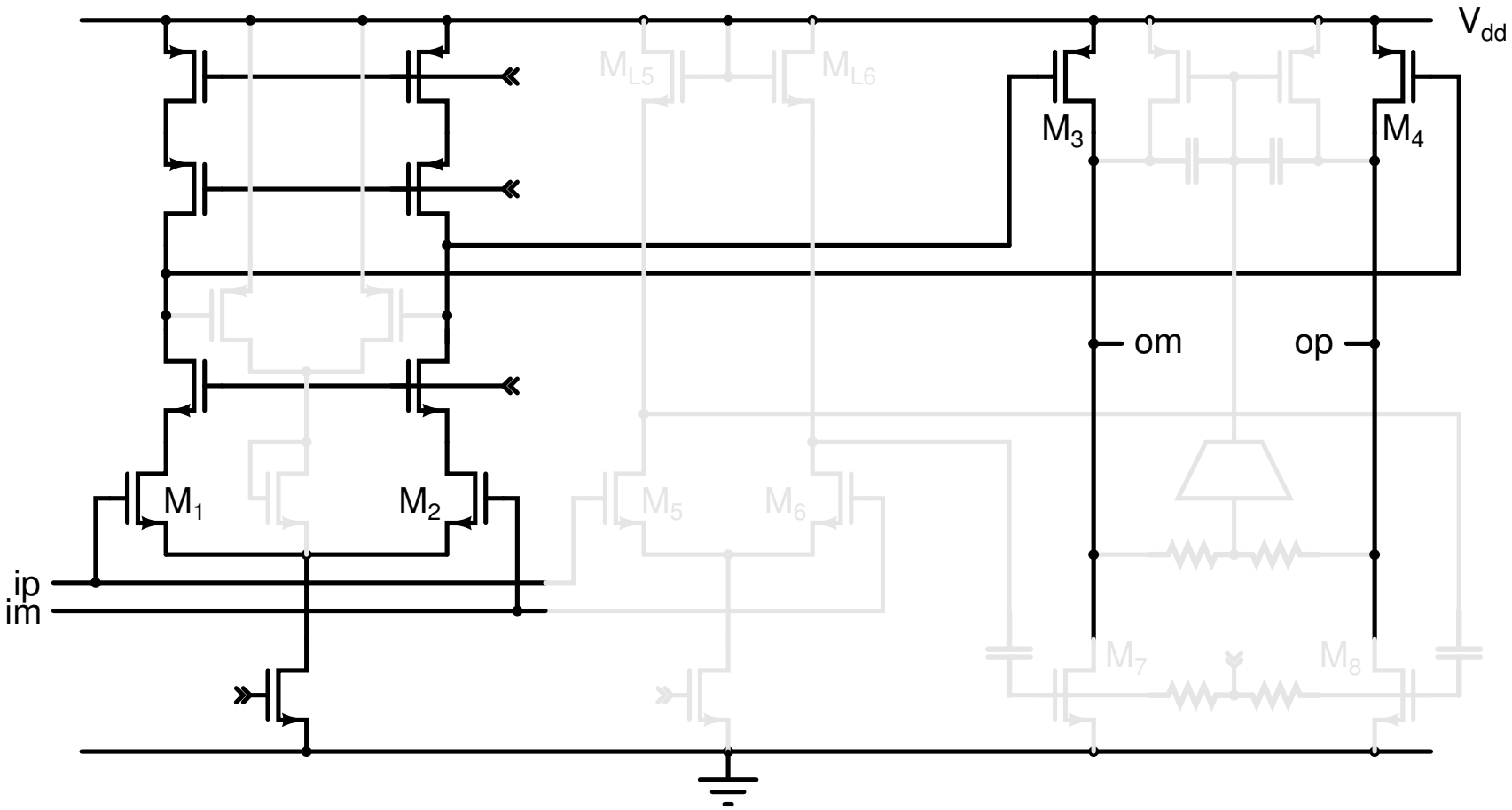


- Feedforward compensated opamp
- Two stage feedforward path to support a high swing

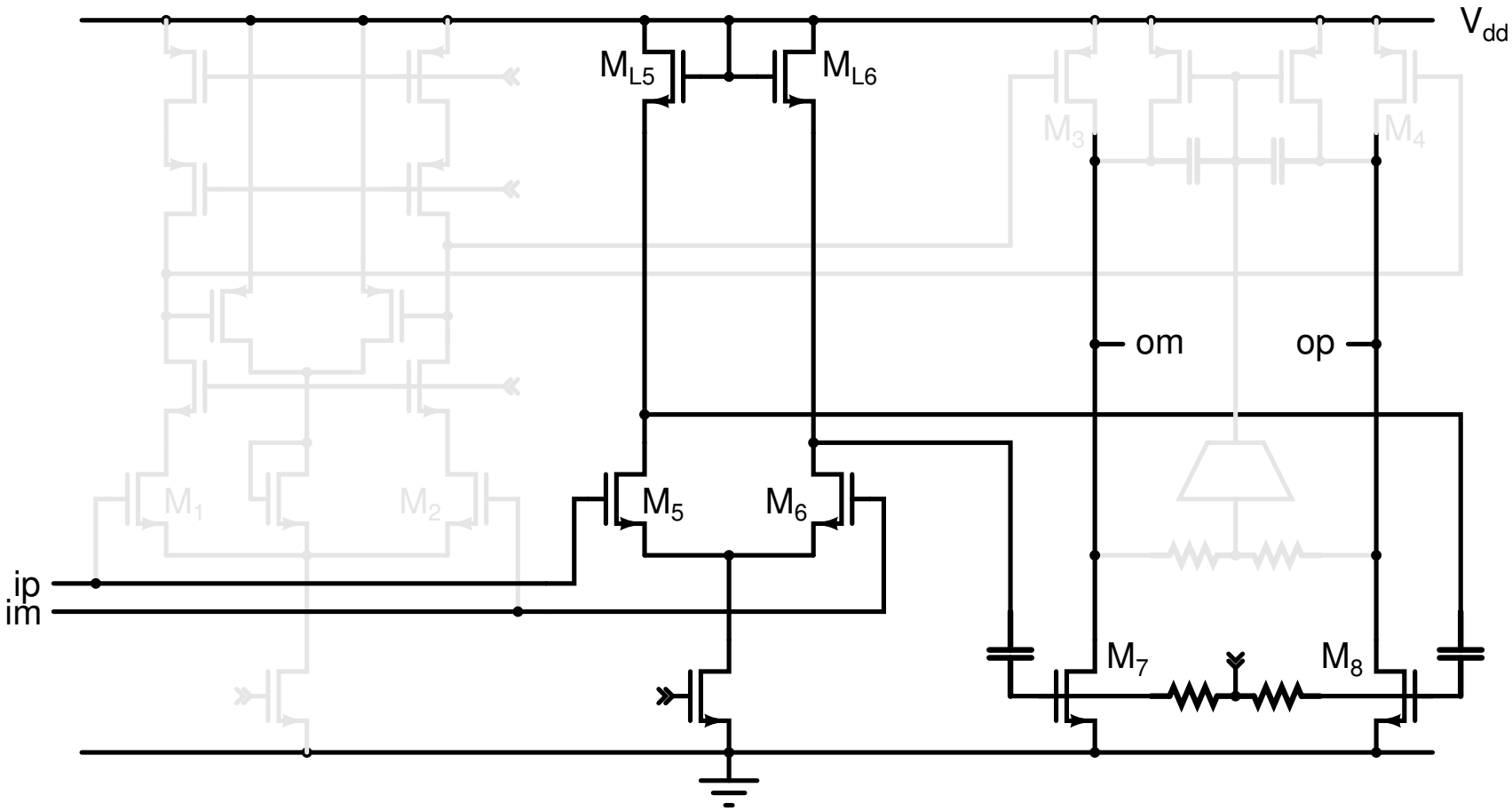
Summing opamp



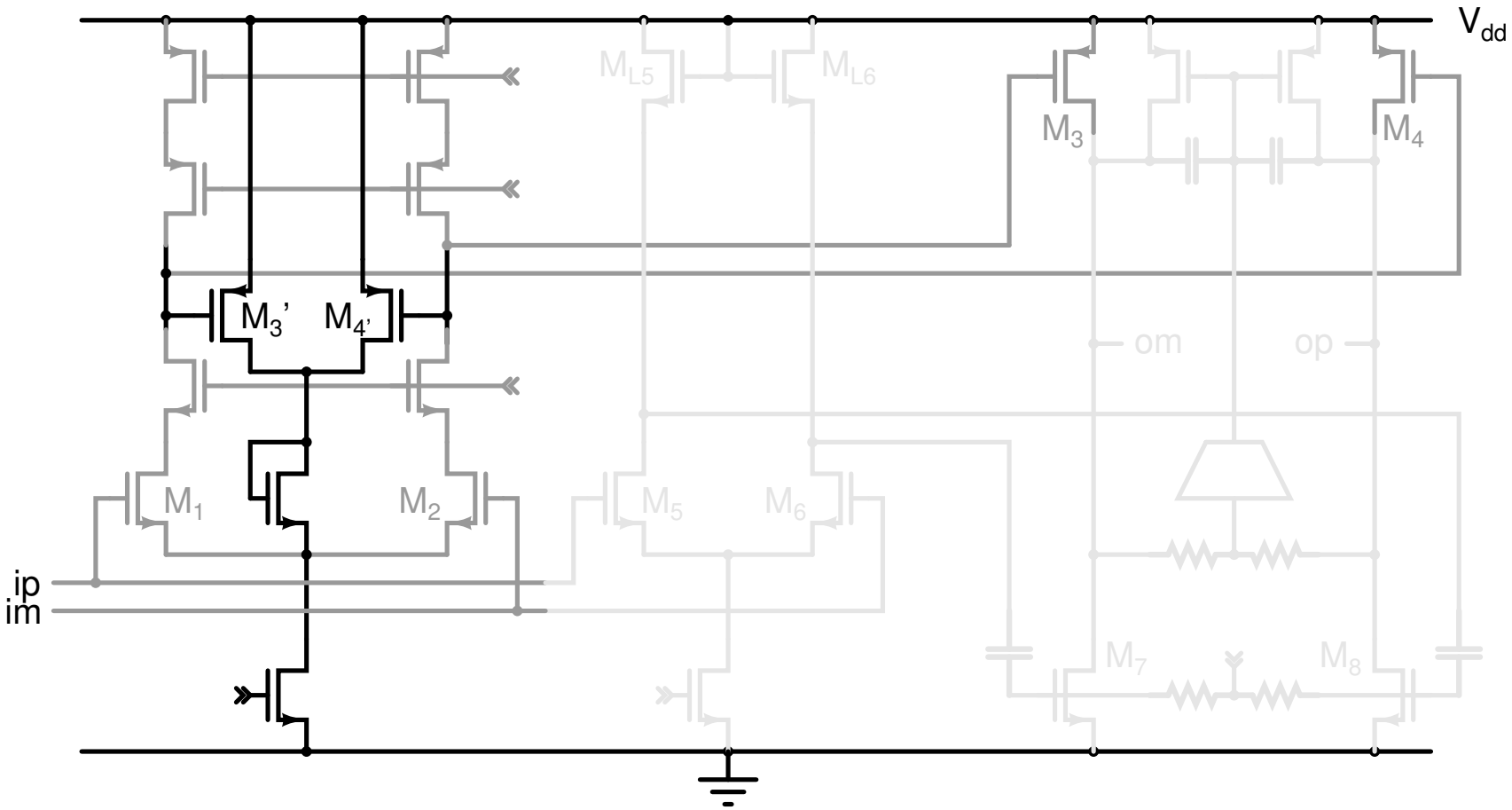
Summing opamp—Gain stages



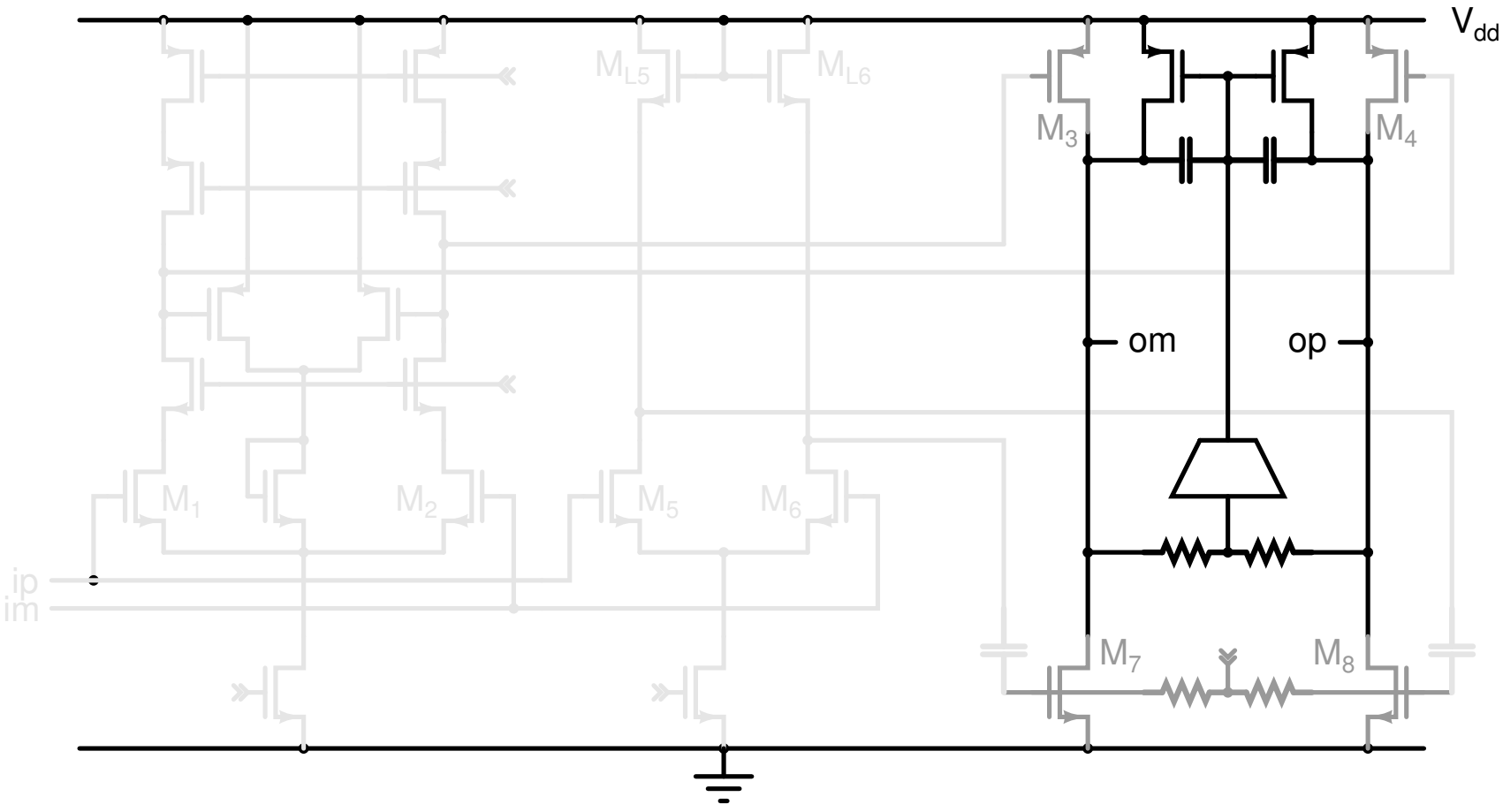
Summing opamp—Feedforward stage



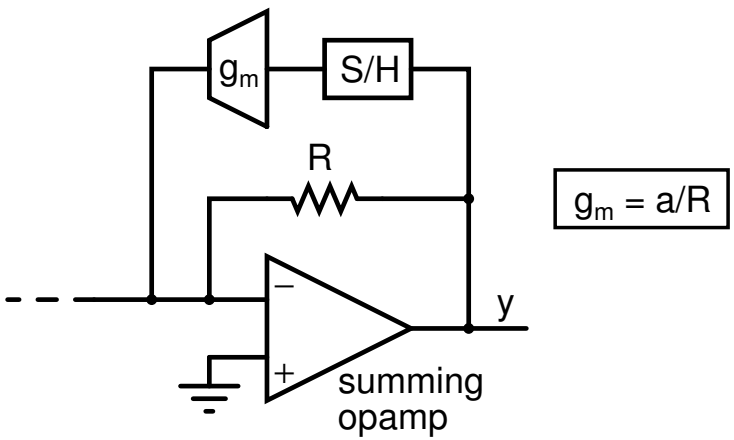
Summing opamp—First stage CMFB



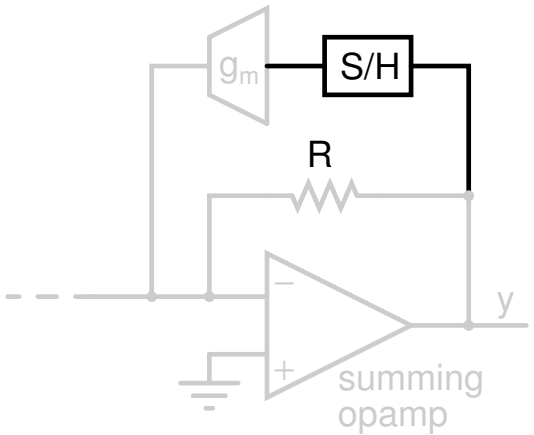
Summing opamp—Second stage CMFB



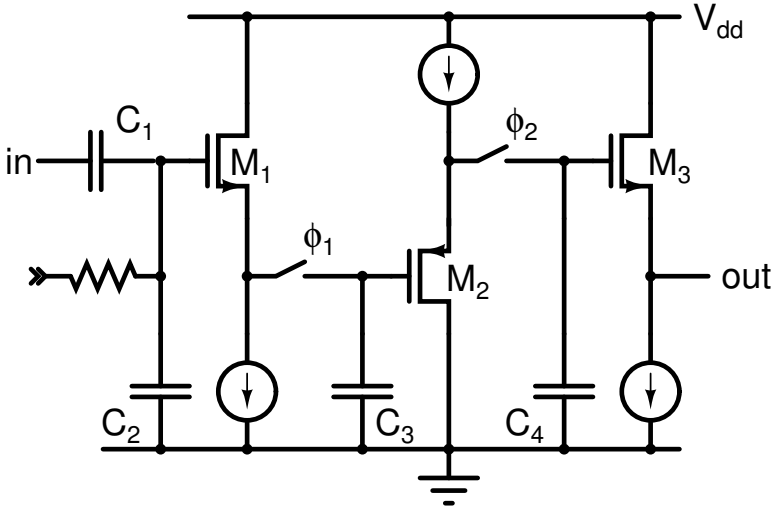
Fast path



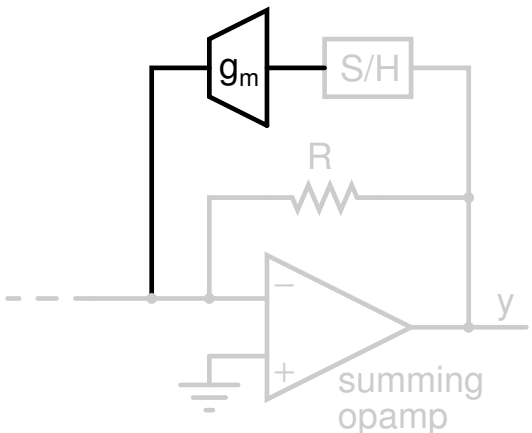
Fast path—Sample and hold



$g_m = a/R$



Fast path—g_m



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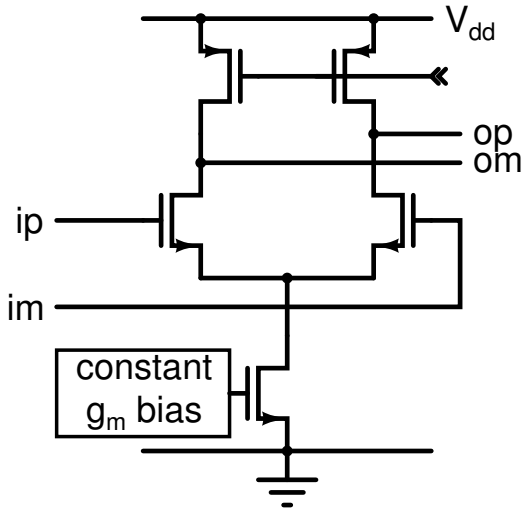
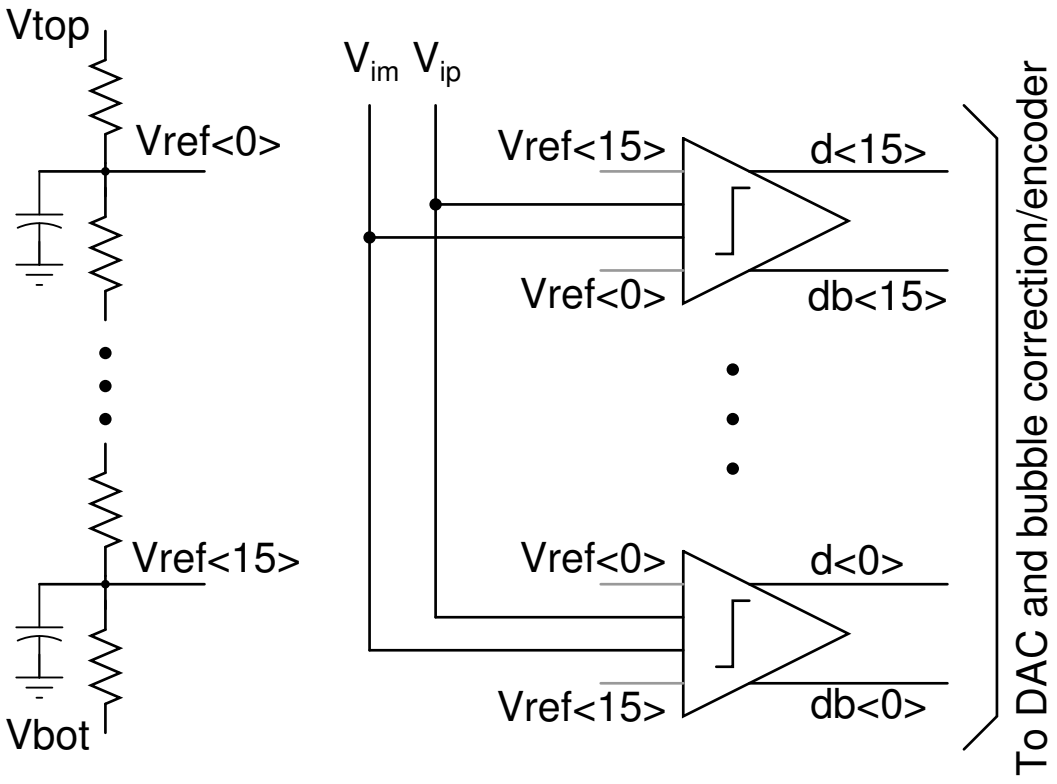
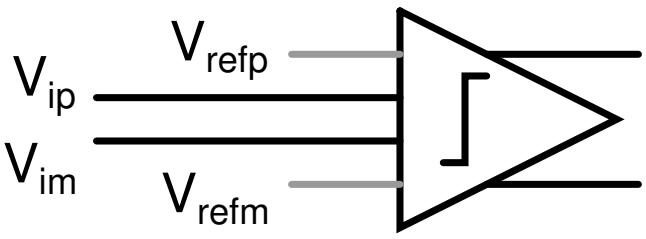
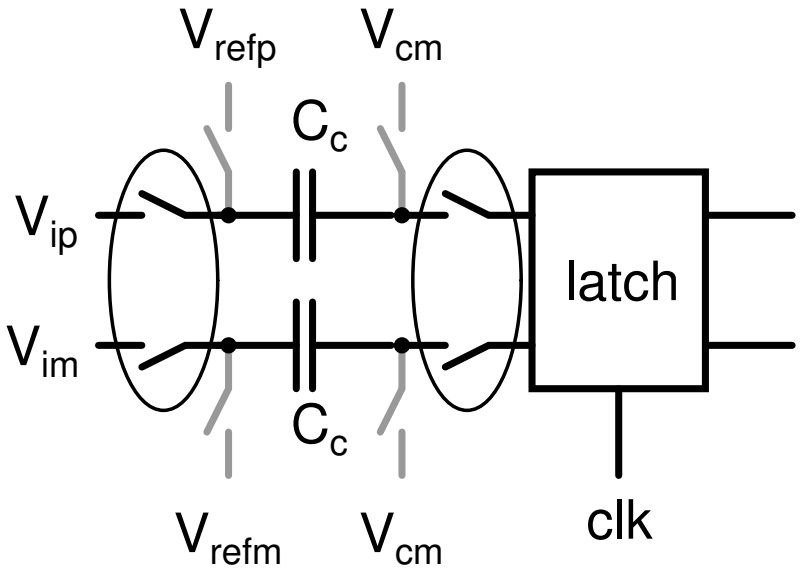


Flash ADC

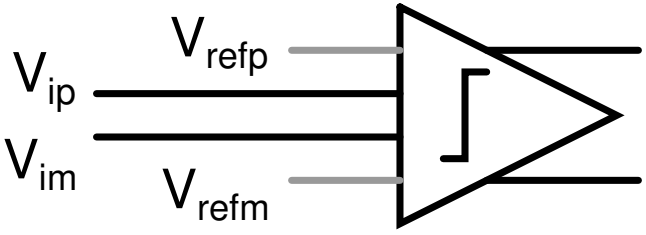

Vtop
Vref<0>
Vref<15>
Vbot
V_{im} V_{ip}
Vref<15>
d<15>
Vref<0>
db<15>
Vref<0>
d<0>
Vref<15>
db<0>
To DAC and bubble correction/encoder

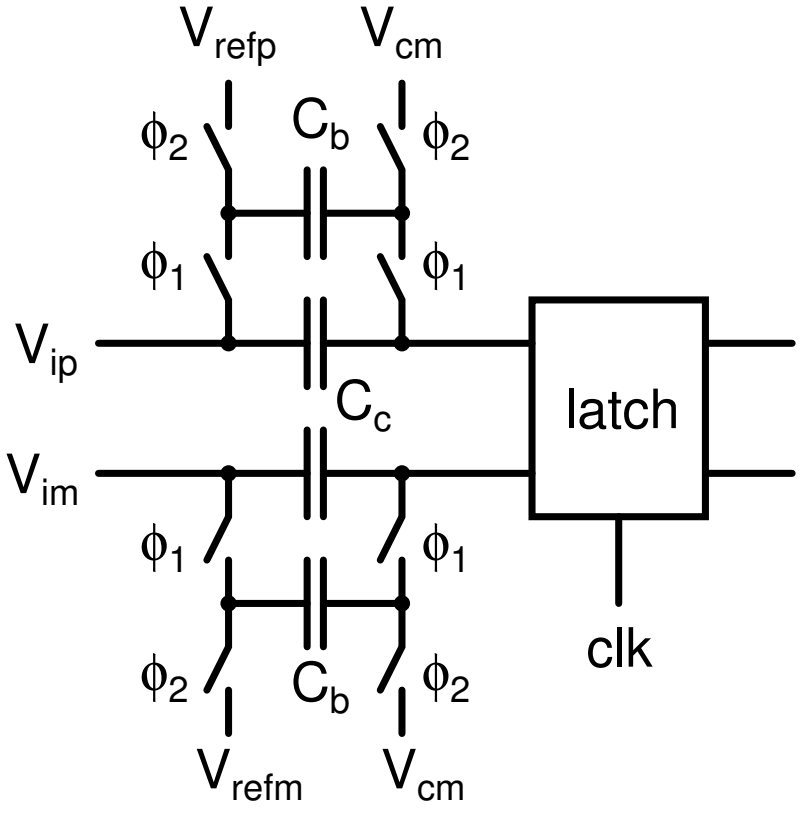
Flash ADC—reference subtraction



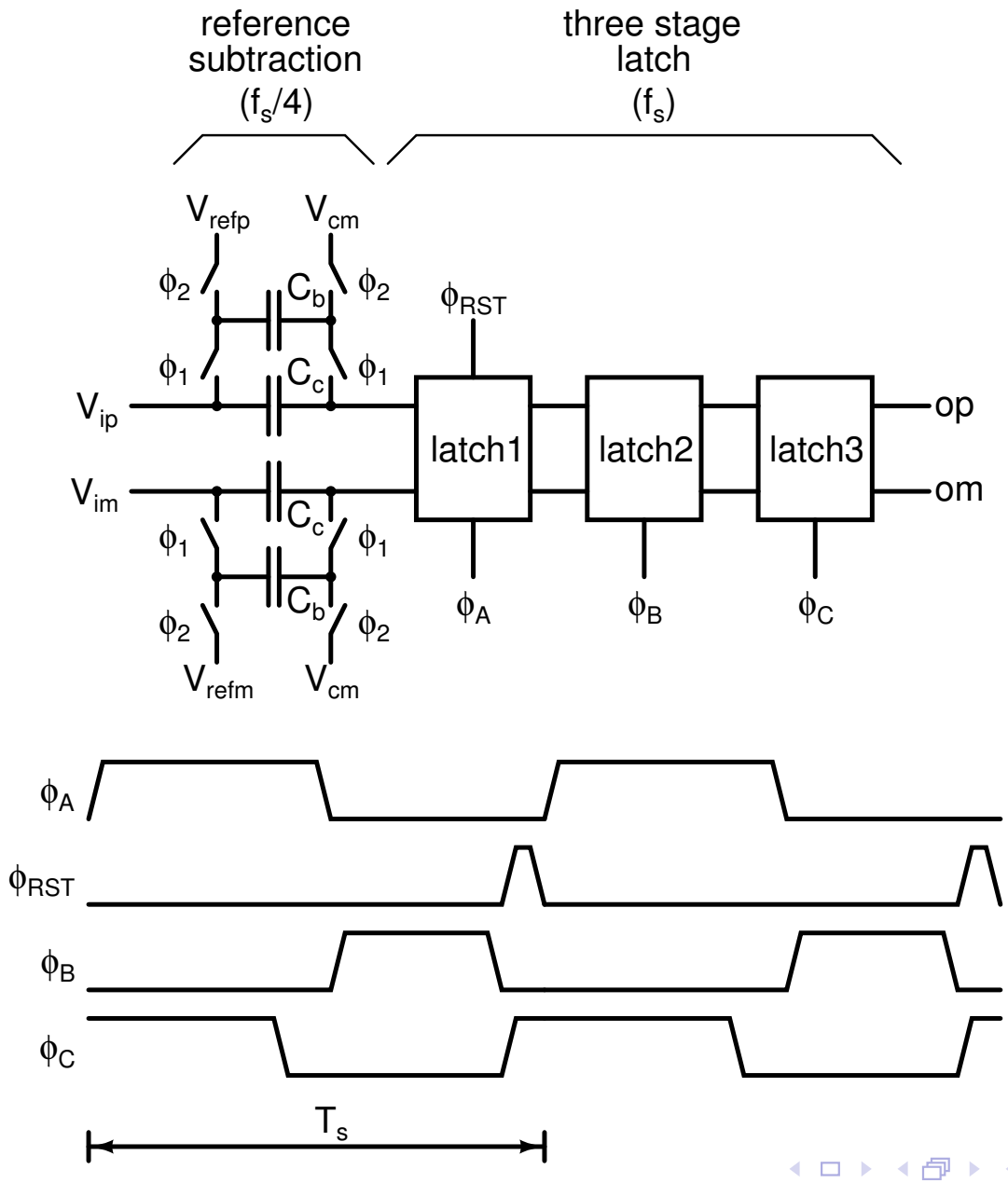


Flash ADC—reference subtraction

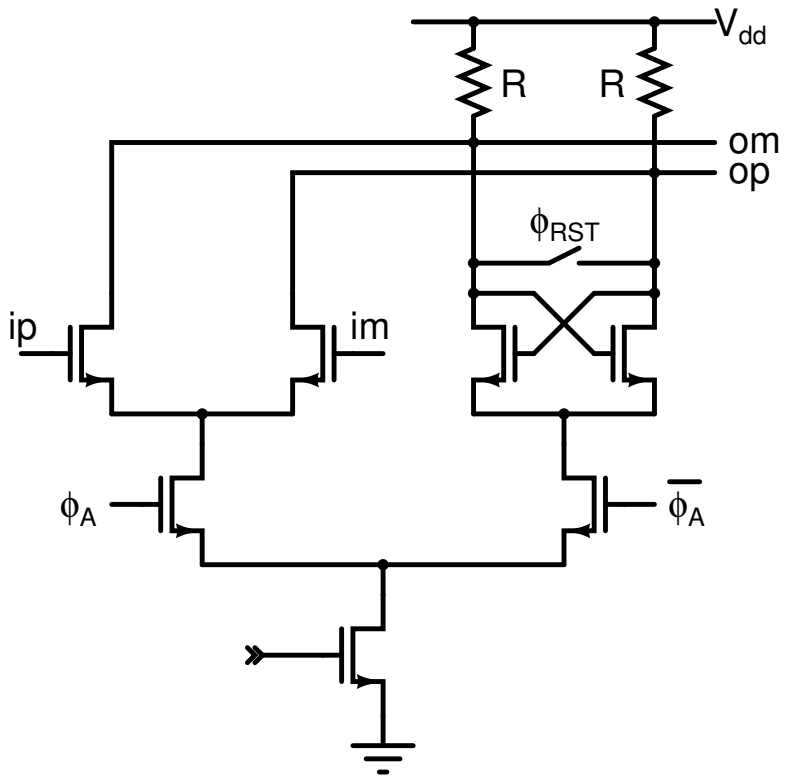




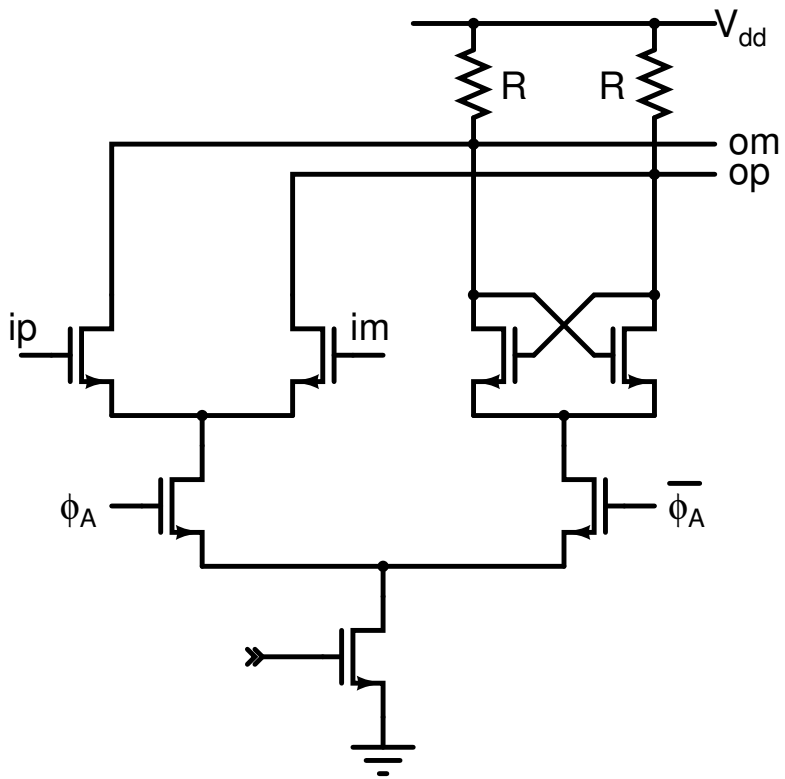
Flash ADC


reference
subtraction
(f_s/4)
three stage
latch
(f_s)
V_{refp}
V_{cm}
ϕ_2
C_b
ϕ_2
ϕ_1
C_c
ϕ_1
V_{ip}
V_{im}
C_c
ϕ_1
ϕ_1
C_b
ϕ_2
ϕ_2
V_{refm}
V_{cm}
ϕ_{RST}
latch1
latch2
latch3
op
om
ϕ_A
ϕ_B
ϕ_C
ϕ_A
ϕ_{RST}
ϕ_B
ϕ_C
T_s

Latch 1



Latch 2, 3



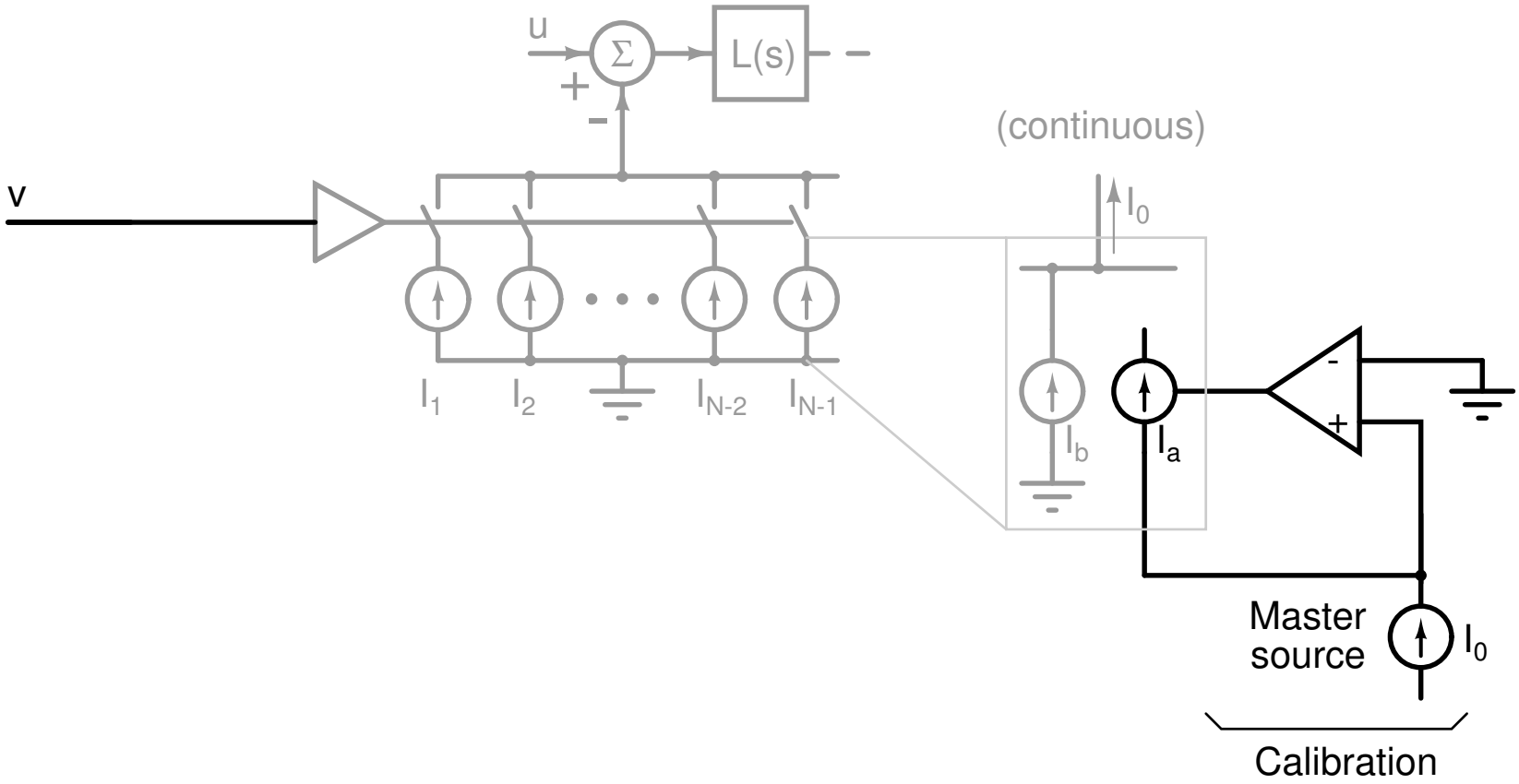
Multi bit DAC

Multi bit DAC suffers from mismatch/nonlinearity

- Dynamic element matching
  - Input switching circuitry for element mapping
- Calibration
  - Input switching circuitry for choosing active sources

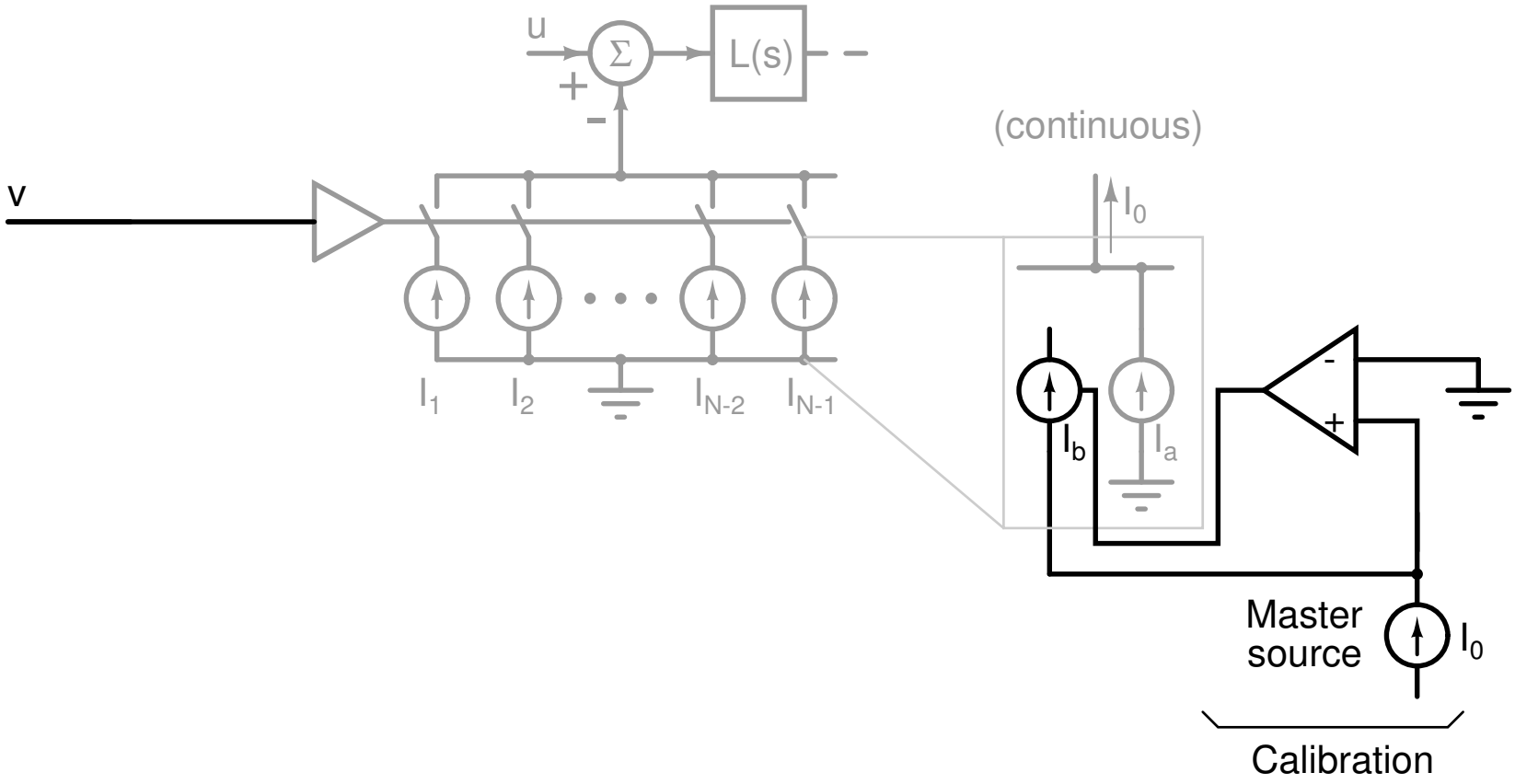
Switching circuitry in the signal path contributes to delay

New delay-free calibration technique



- Each unit has two current sources calibrated alternately
- Each unit provides a continuous output
- No switching in the signal path

New delay-free calibration technique



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- Each unit provides a continuous output
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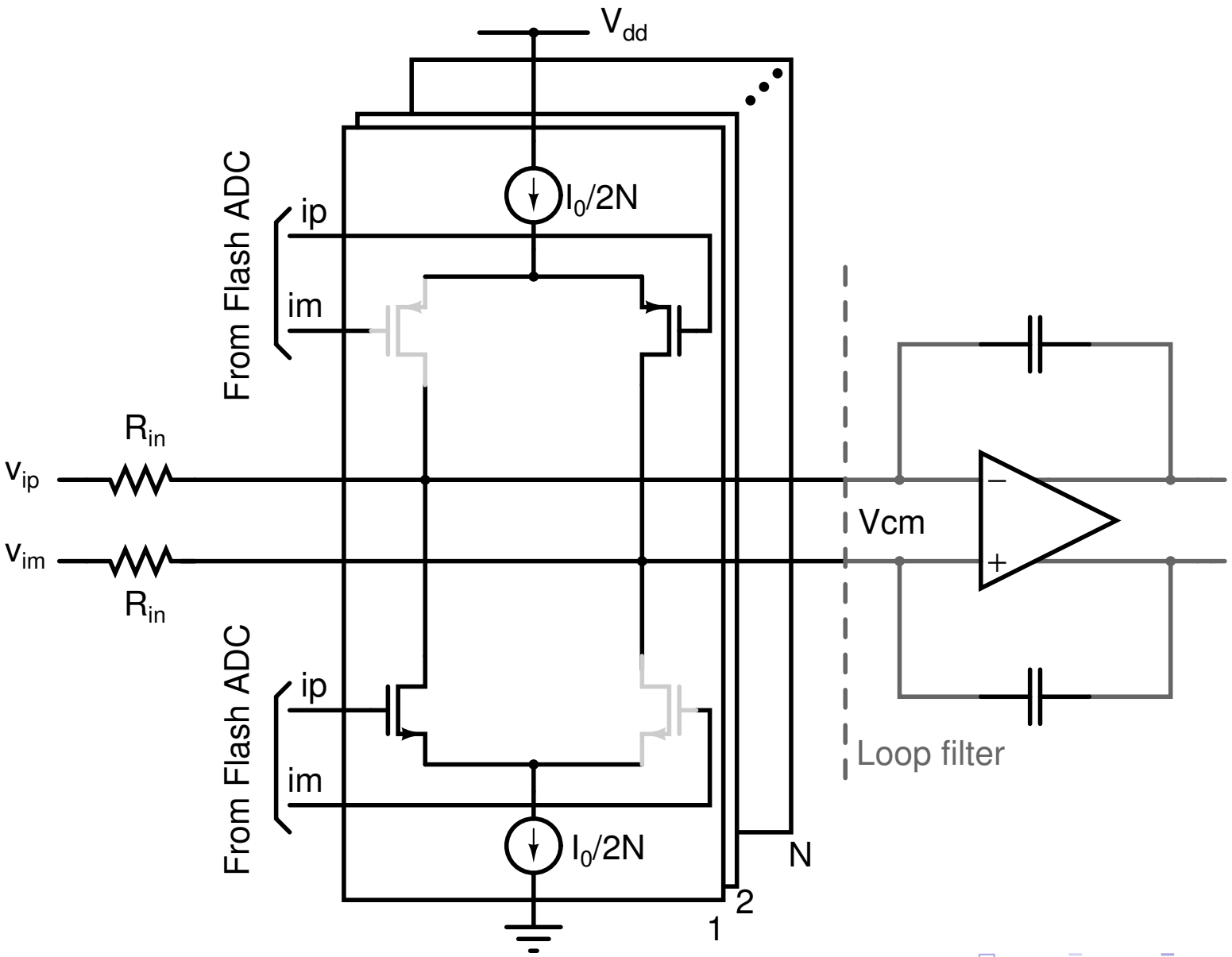
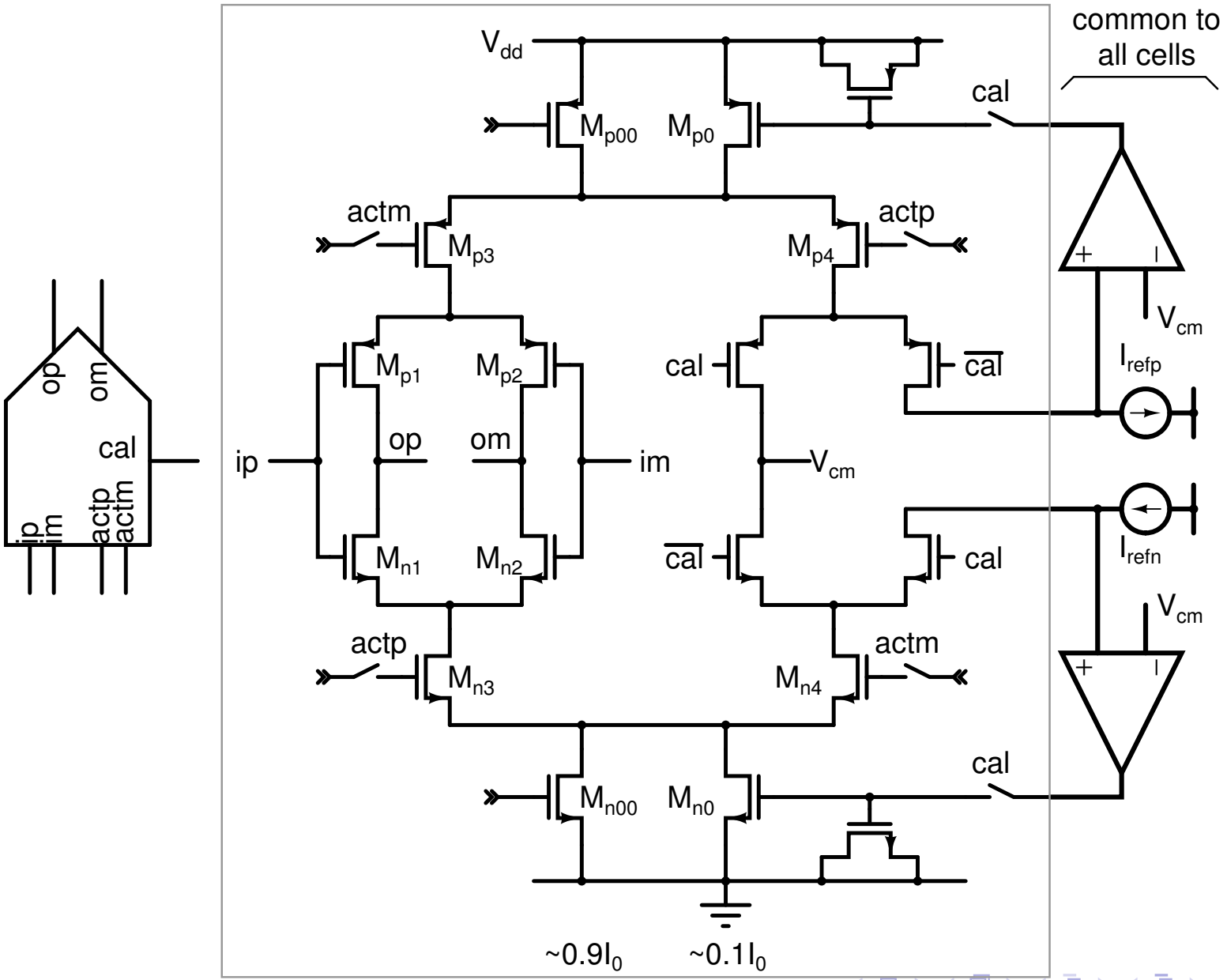
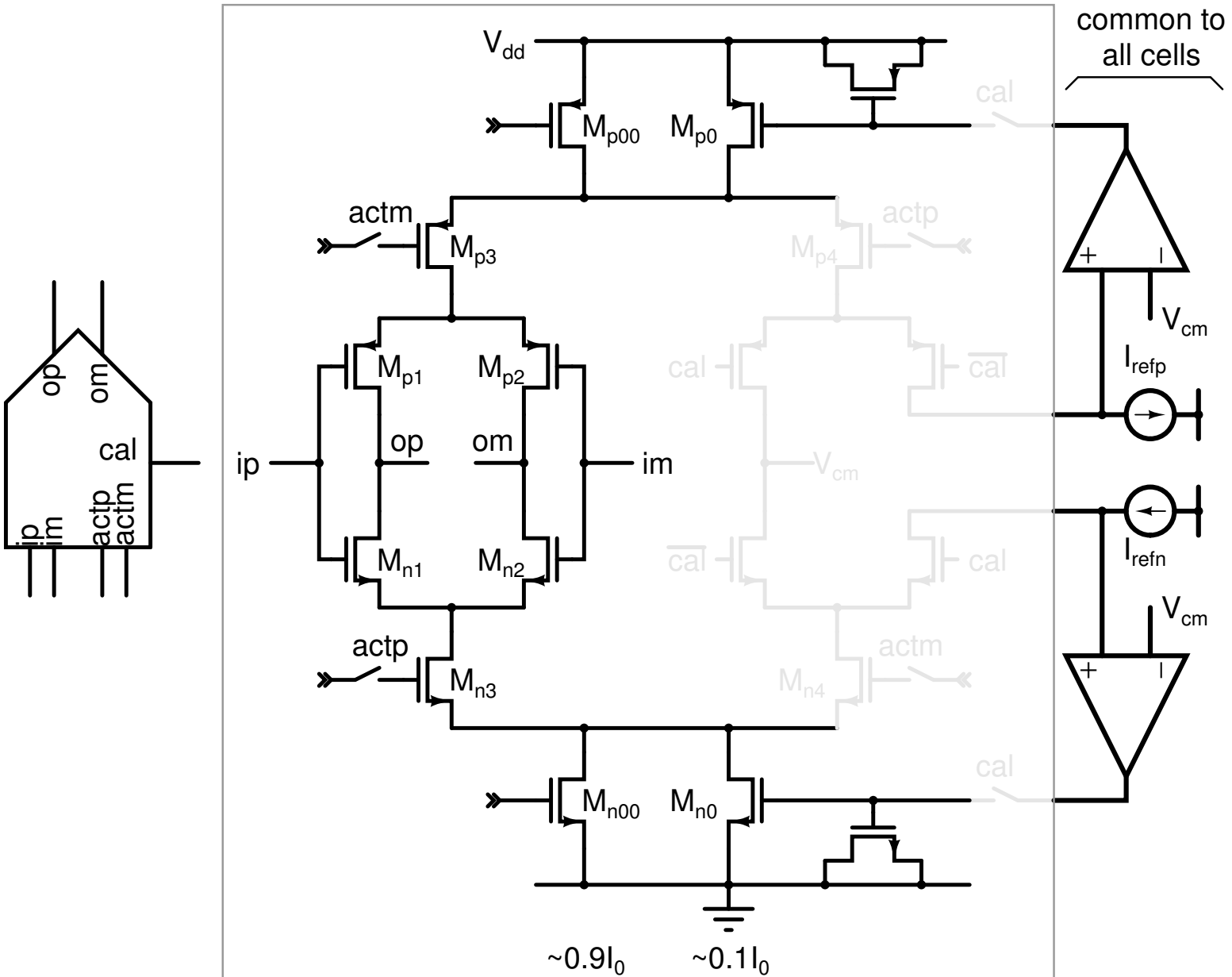
DAC—nMOS and pMOS sources



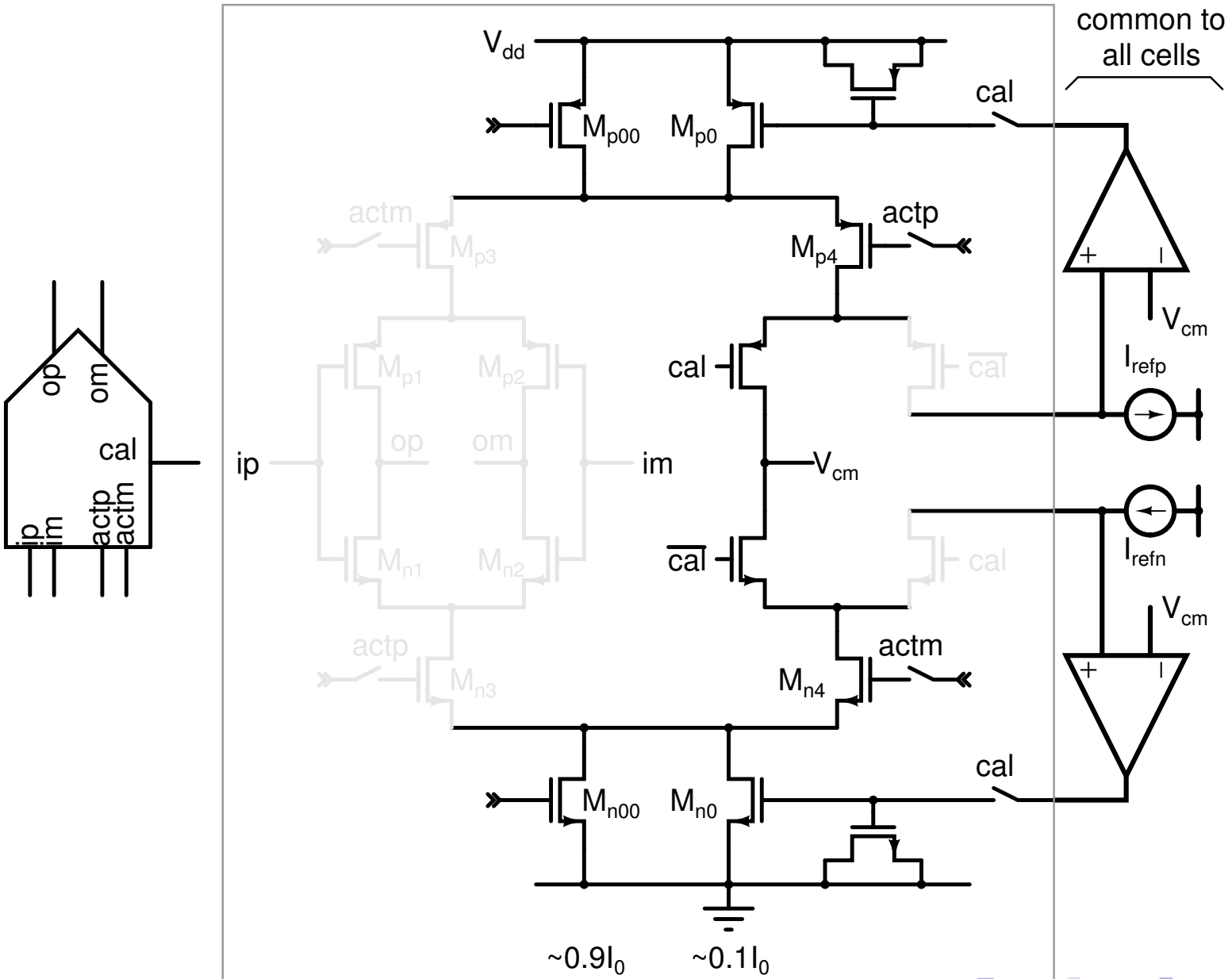
DAC Cell


common to all cells
V_{dd}
M_{p00}
M_{p0}
cal
actm
actp
M_{p3}
M_{p4}
M_{p1}
M_{p2}
op
om
ip
im
V_{cm}
$\overline{cal}$
I_{refp}
I_{refn}
M_{n1}
M_{n2}
M_{n3}
M_{n4}
M_{n00}
M_{n0}
$\sim 0.9I_0$
$\sim 0.1I_0$
ip
im
actp
actm

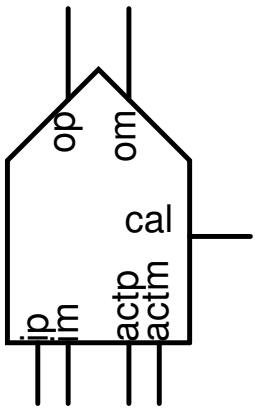
DAC Cell—active

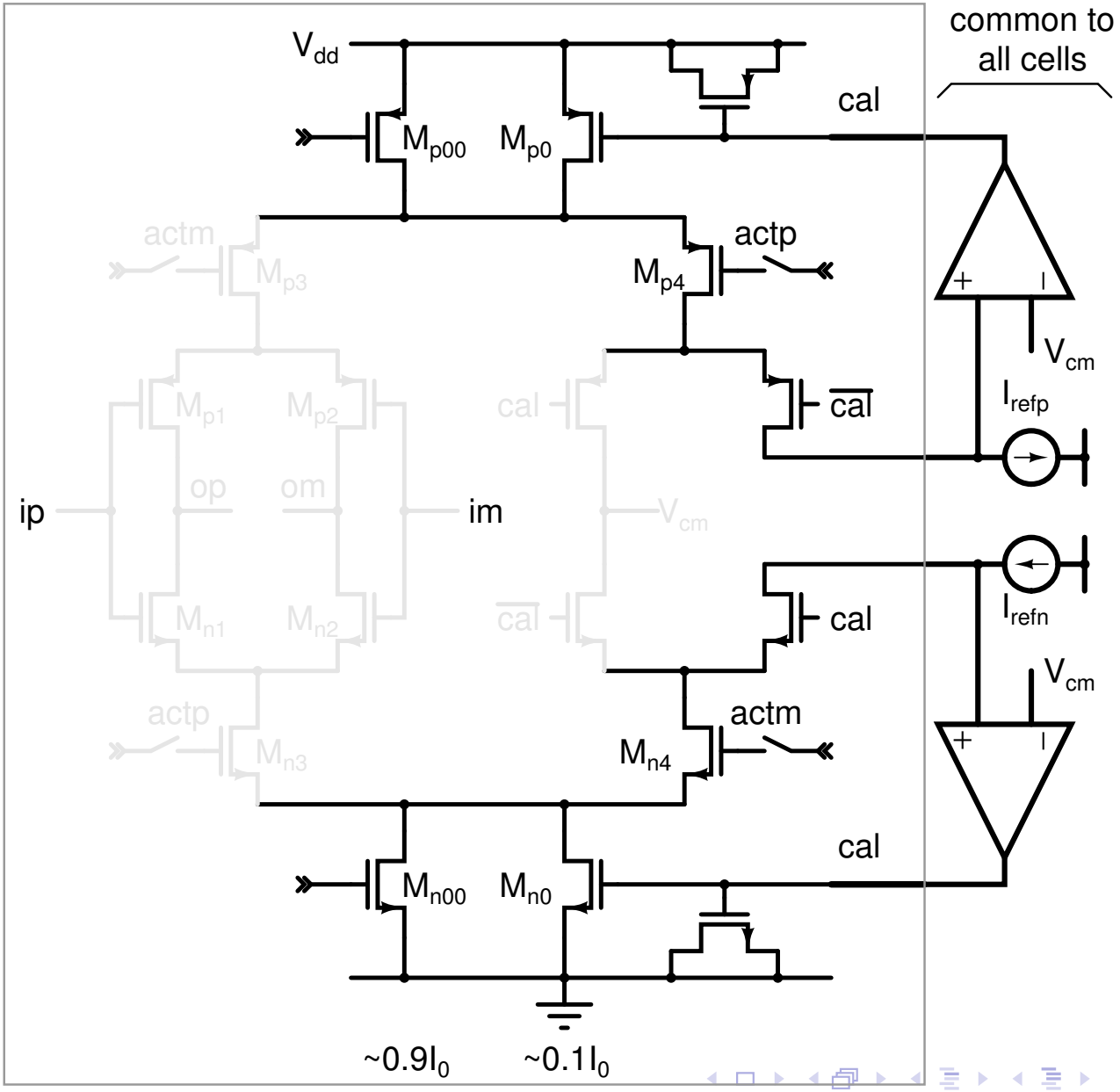


DAC Cell—inactive



DAC Cell—being calibrated

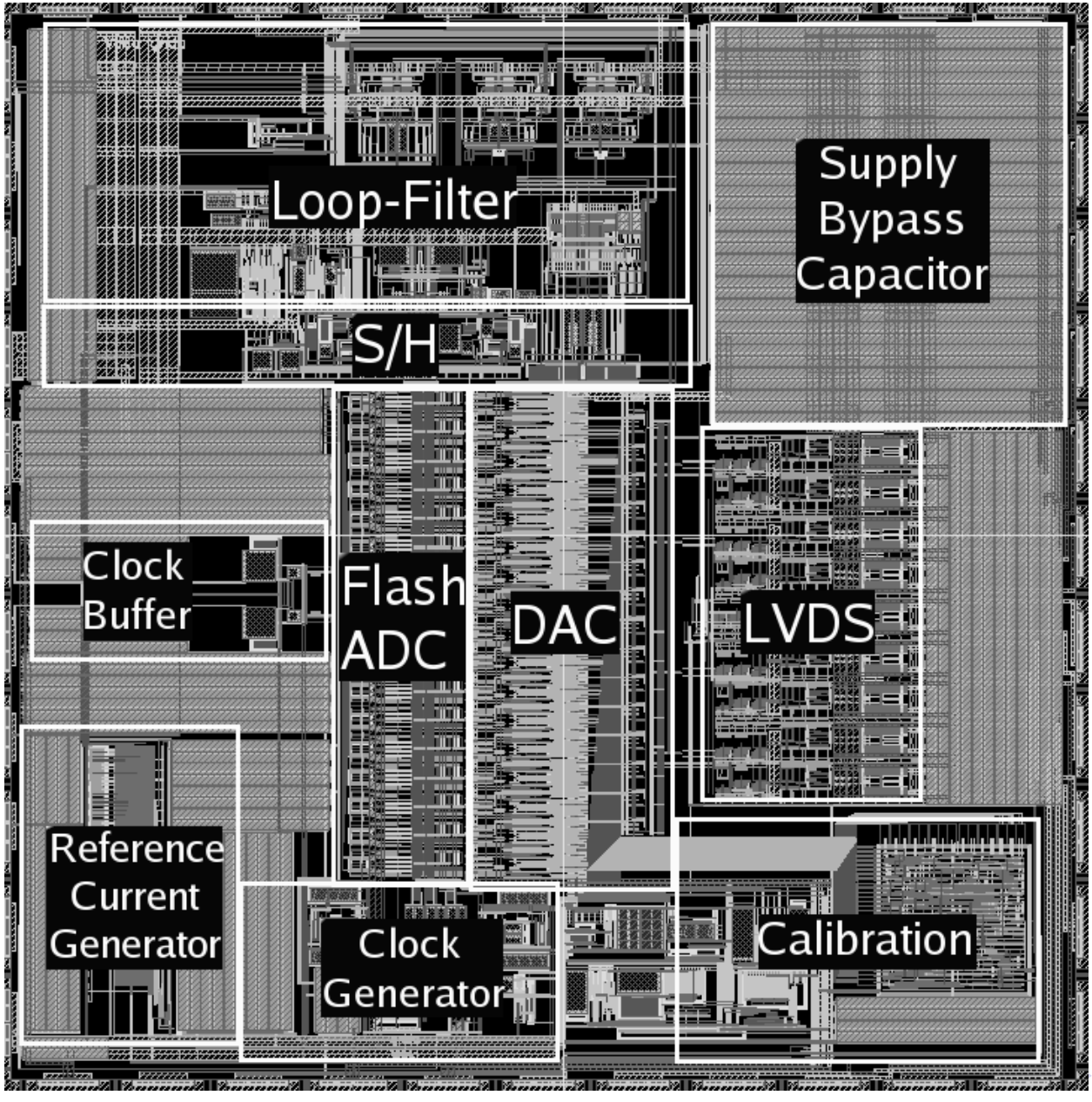




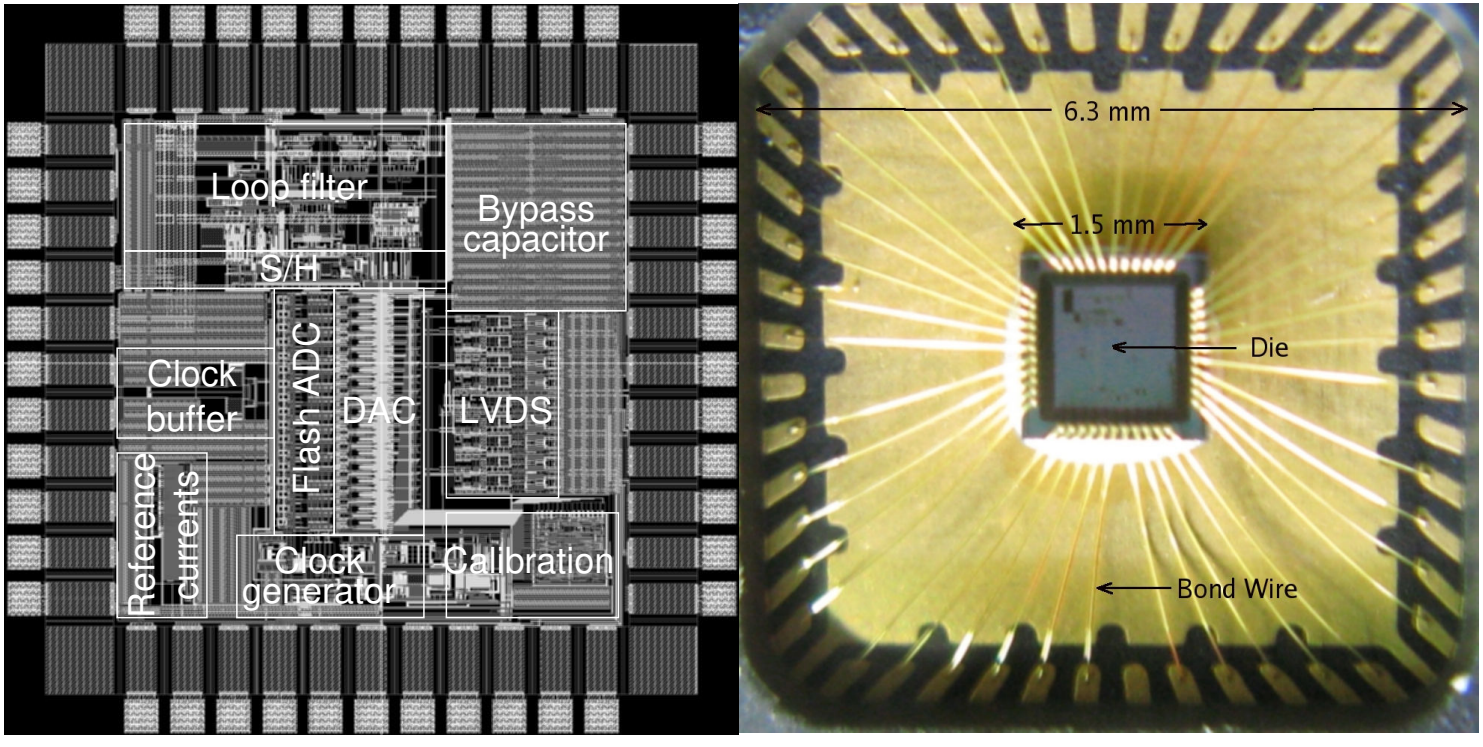
Simulated performance

Sampling Frequency	800 MHz
Input Bandwidth	16 MHz
Quantizer Range	3 $V_{pp,diff}$
SQNR	88 dB
Inband Thermal Noise	84 dB
Net DR	82.5 dB
Power dissipation	
Loop filter	17 mW (1.8 V)
Fast loop	2.4 mW (1.8 V)
Flash ADC	15.2 mW (1.8 V)
DAC (+driver)	8.6 mW (1.8 V)
Clock buffer	2.6 mW (1.8 V)
Total	45.8 mW (1.8 V)

Prototype chip



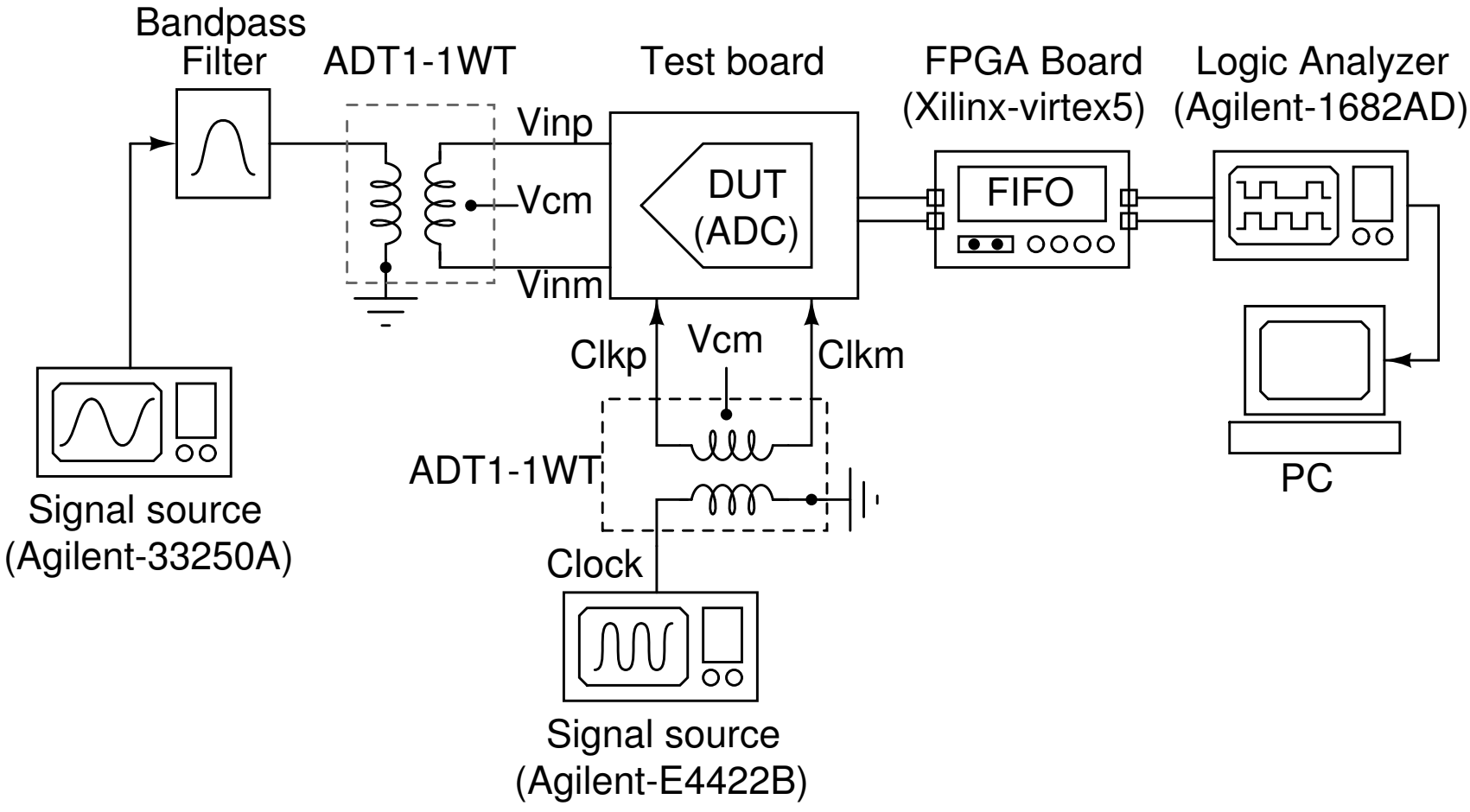
Prototype chip



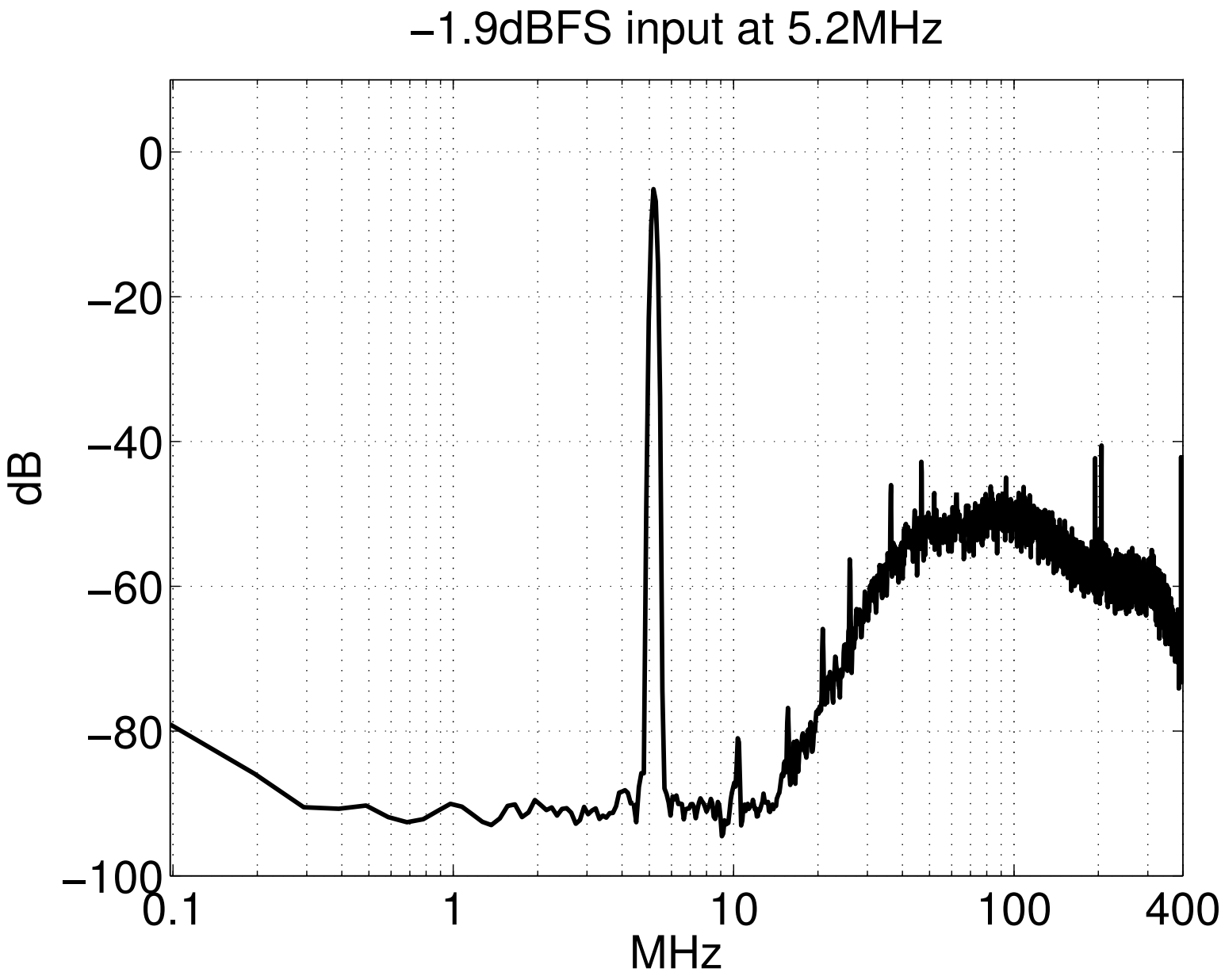
(a) (b)

- 0.18 μm CMOS; 1.8 V supply; 0.68 mm^2; QFN48 package

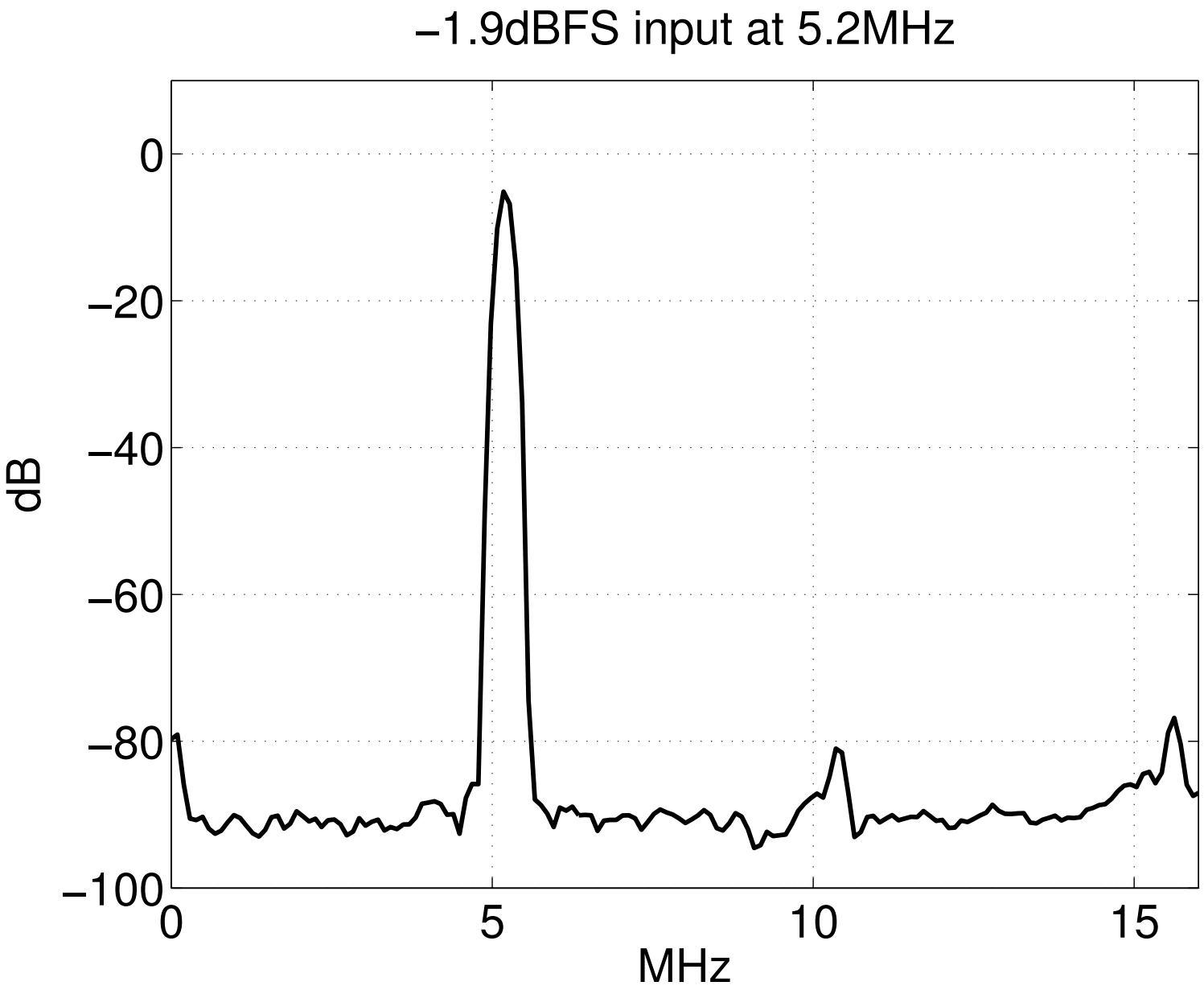
Test setup


Bandpass
Filter
ADT1-1WT
Test board
FPGA Board
(Xilinx-virtex5)
Logic Analyzer
(Agilent-1682AD)
Vinp
Vcm
Vinm
DUT
(ADC)
FIFO
Clkp
Vcm
Clkm
ADT1-1WT
Clock
PC
Signal source
(Agilent-33250A)
Signal source
(Agilent-E4422B)

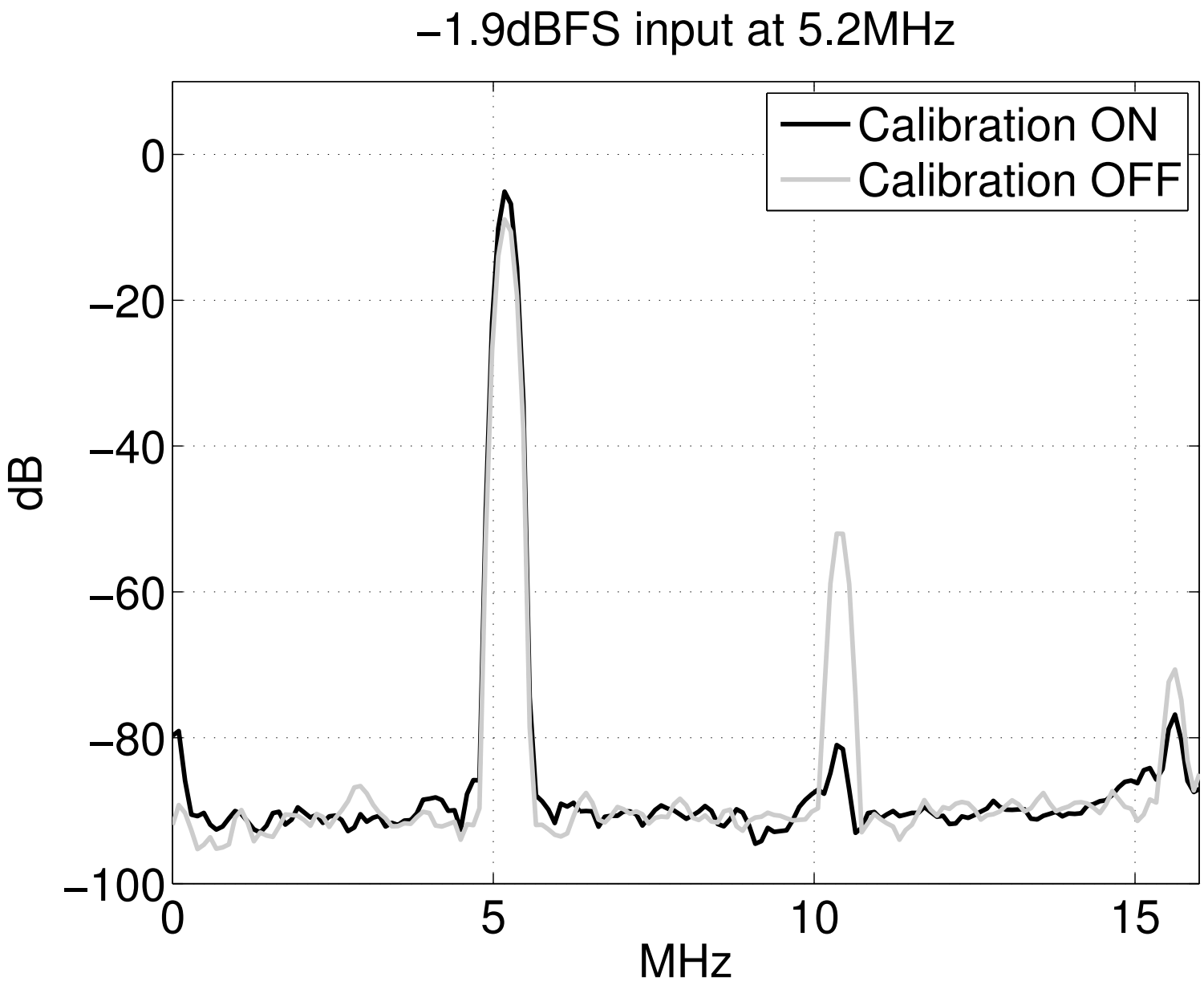
Output spectrum



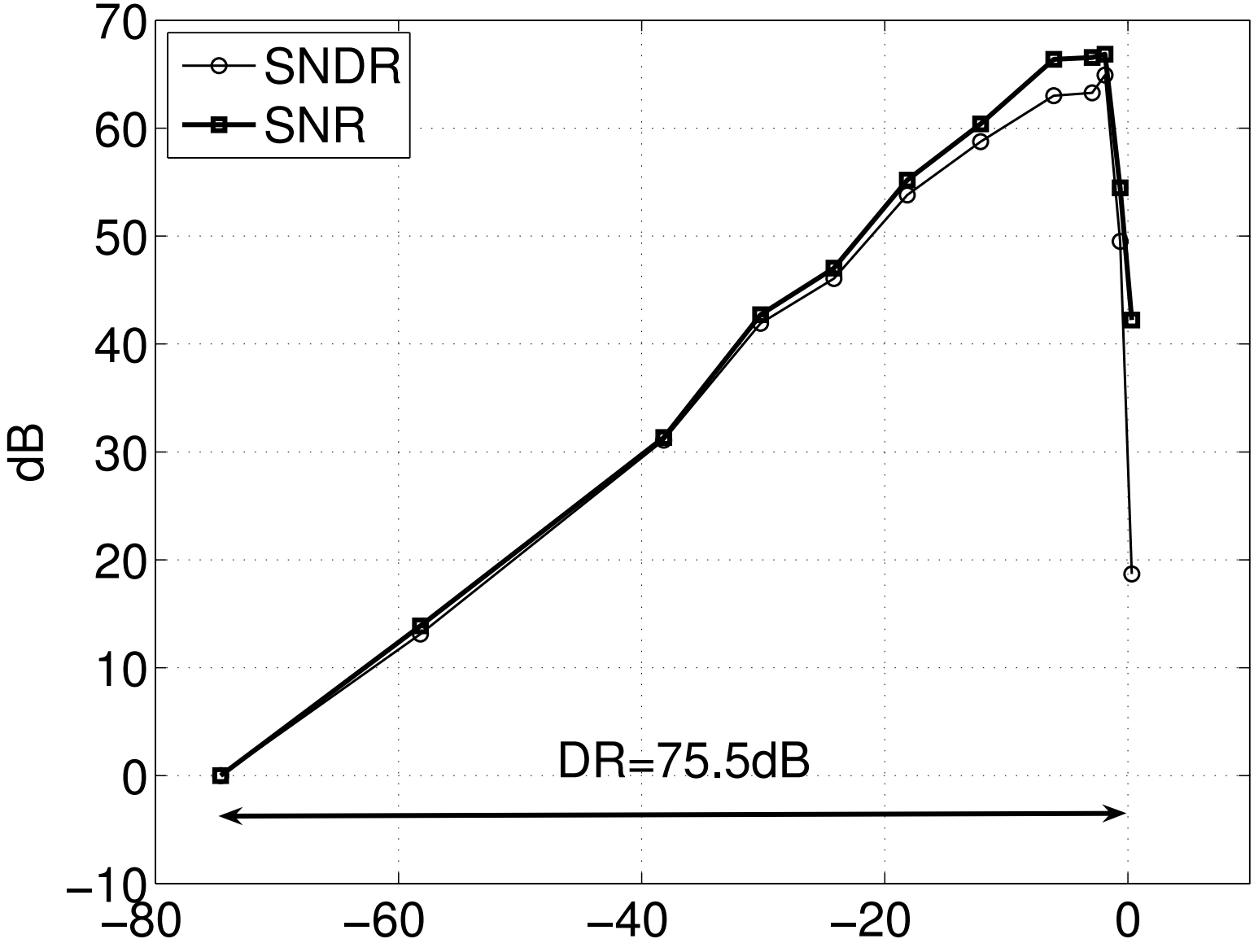
Output spectrum; $HD_2 = -76\,dB$ $HD_3 = -72\,dB$



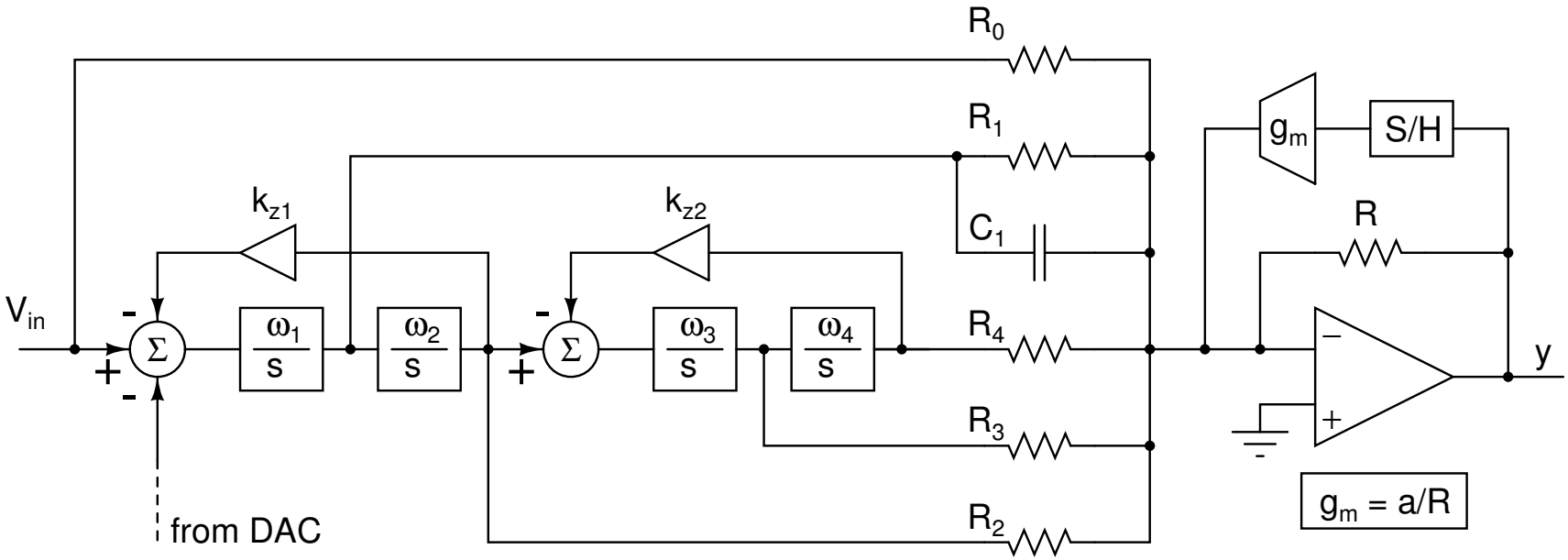
Effectiveness of DAC calibration



Dynamic range

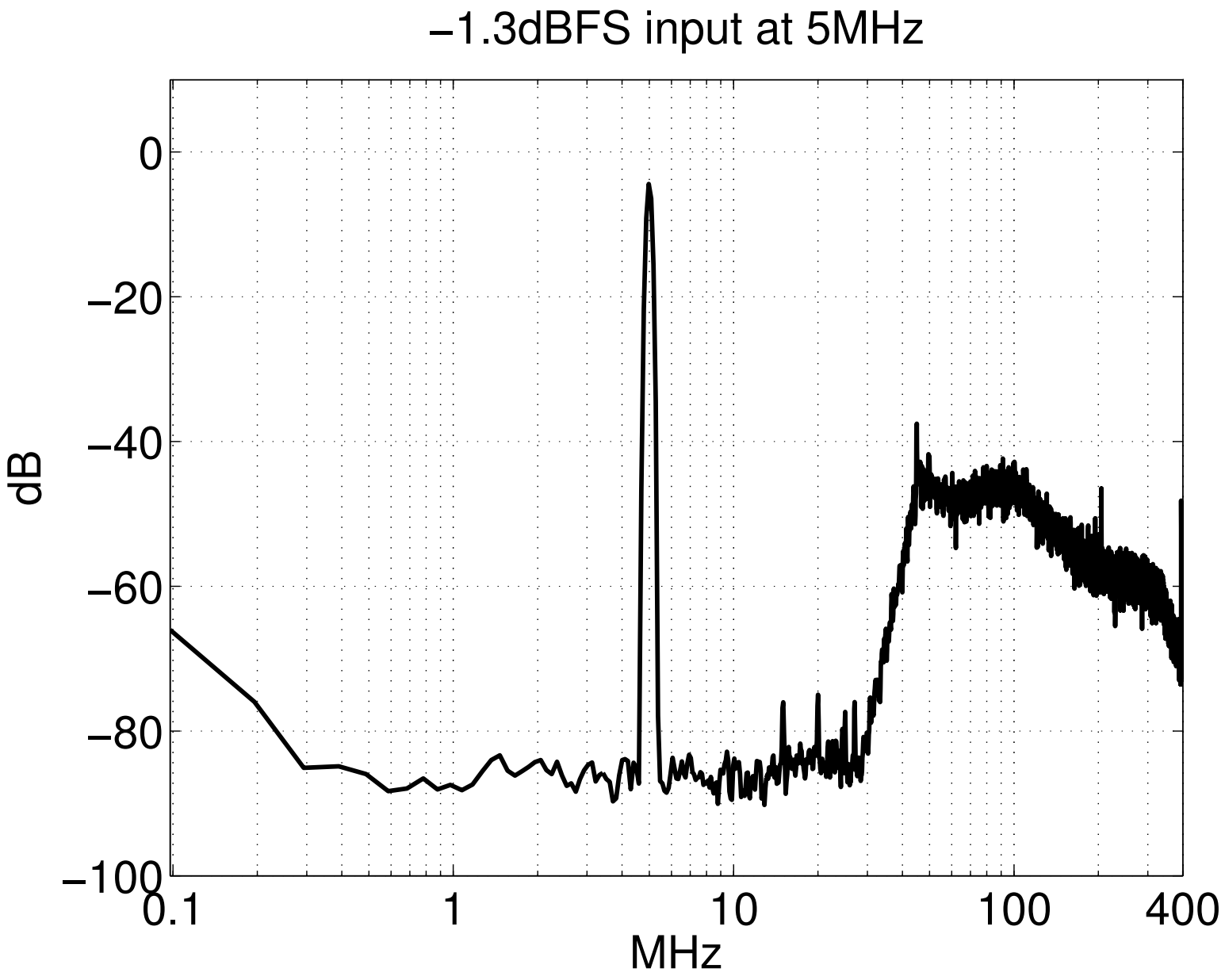


OSR = 12.5 (BW = 32 MHz)

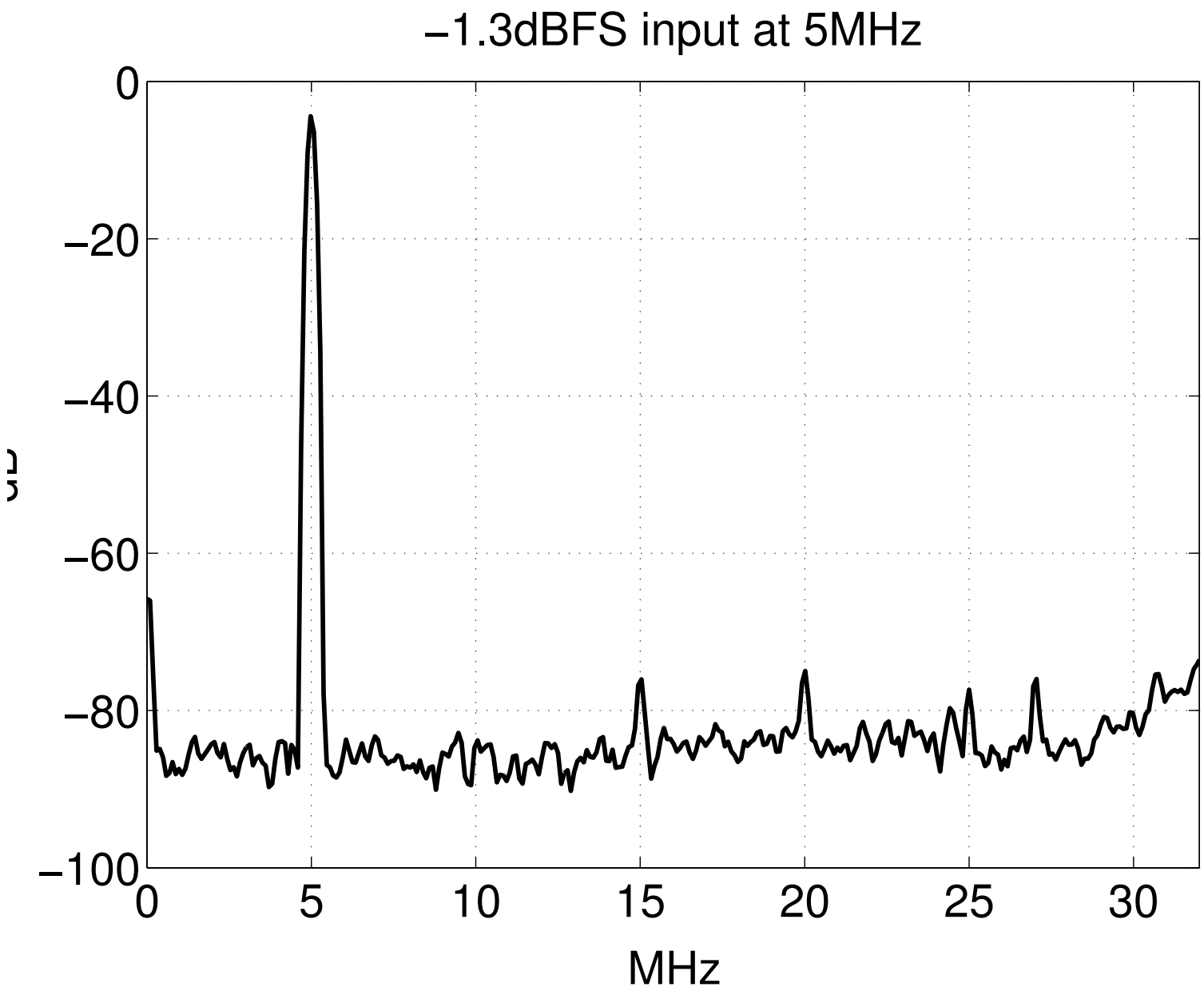


- k_{z1} and k_{z2} modified to optimize the zeros for OSR = 12.5

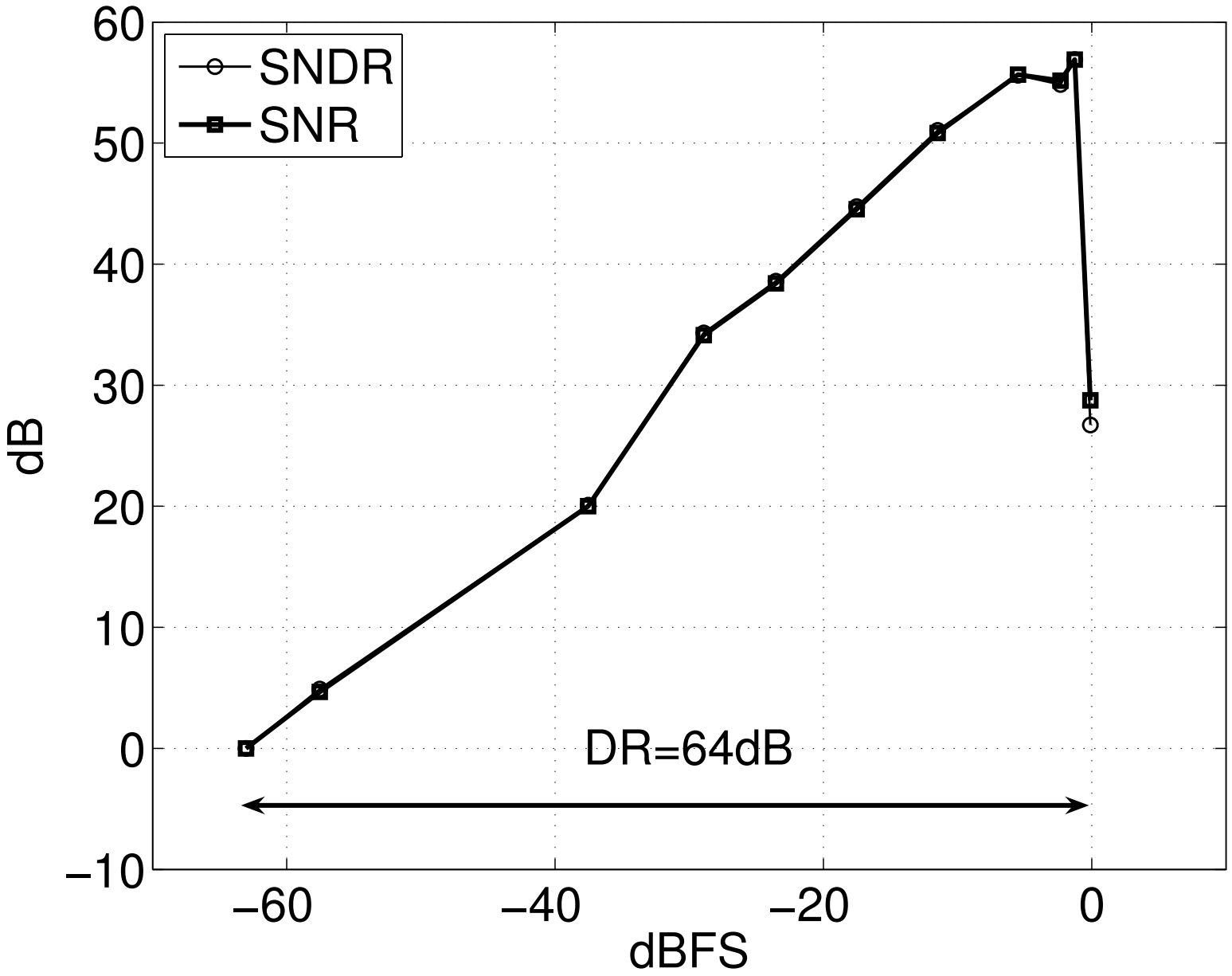
OSR = 12.5 (BW = 32 MHz): Output spectrum



OSR = 12.5 (BW = 32 MHz): Output spectrum



OSR = 12.5 (BW = 32 MHz): Dynamic range



Performance summary

Process	0.18 μm	
Active area	0.68 mm^2	
Supply voltage	1.8 V	
Sampling rate	800 MHz	
Full scale	3 Vppd	
P_d	47.6 mW	
BW (MHz)	16	32
DR (dB)	75	64
SNR_{max} (dB)	67	57
$SNDR_{max}$ (dB)	65	57
HD_2 dB	-76	—
HD_3 dB	-72	-72

Figures of merit

$$FOM_1\,[XX] = \frac{P_d}{2\mathrm{BW} \cdot 2^{(\mathrm{XX}-1.76)/6.02}}$$

- Power dissipation normalized to number of resolved levels and sampling rate of an equivalent Nyquist rate ADC
- *XX*: Dynamic range, $\mathrm{SNR}_{\max}$, or $\mathrm{SNDR}_{\max}$

$$FOM_2 = \mathrm{DR} + 10\log_{10}\frac{\mathrm{BW}}{P_d}$$

- Dynamic range normalized to bandwidth and power dissipation

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P_d	47.6 mW	
BW (MHz)	16	32
DR (dB)	75	64
SNR_{max} (dB)	67	57
SNDR_{max} (dB)	65	57
FOM_1 [DR] (pJ)	0.32	0.57
FOM_1 [SNR_{max}] (pJ)	0.81	1.29
FOM_1 [SNDR_{max}] (pJ)	1.02	1.29
FOM_2 (dB)	160.3	152.3

Comparison with other designs

		f_s (MHz)	f_b (MHz)	DR/SNR$_{max}$/SNDR$_{max}$ (dB)	P_d (mW)	FOM_1 (pJ)	FOM_2 (dB)
This work	**0.18 μm**	**800**	**16**	**75/67/65**	**47.6**	**0.32/0.81/1.02**	**160.3**
This work	**0.18 μm**	**800**	**32**	**64/57/57**	**47.6**	**0.57/1.3/1.3**	**152.3**
[9]	0.18 μm	400	25	69/68.5/67.7	48	0.42/0.44/0.48	156.2
[1]	0.18 μm	240	7.5	77/71/67	89	1.03/2.05/3.24	156.3
[2]	0.18 μm	200	20	55.2/49.7/48.8	103	5.48/10.32/11.44	138.1
[3]	0.18 μm	100	10	60.8/58.4/57.2	101	5.64/7.43/8.53	140.8
[3]	0.18 μm	160	10	67/63/—	122.4	3.35/5.3/—	146.1
[4]	0.18 μm	640	10	87/84/82	100	0.27/0.39/0.49	167.0
[3]	0.18 μm	300	15	70/67.2/64.2	20.7	0.27/0.37/0.52	158.6
[5]	0.18 μm	96	6	—/60.7/—	6.18	—/0.58/—	89.9
[8]	0.13 μm	900	20	80/81/78	87	0.27/0.24/0.34	163.6
[6]	0.13 μm	404	17	63.4/59.4/58.6	25.2	0.61/0.97/1.07	151.7
[7]	0.13 μm	950	10	86/86/72	40	0.12/0.12/0.61	170.0
[7]	0.13 μm	950	10	75/75/67	40	0.22/0.22/0.55	162.0
[2]	0.13 μm	640	20	80/76/74	20	0.06/0.1/0.12	170.0
[8]	0.13 μm	300	20	67/64.6/63.7	70	0.96/1.3/1.4	151.6
[9]	0.13 μm	240	10	67/63/63	20.5	0.56/0.89/0.89	153.9
[1]	0.11 μm	300	10	70/68.2/62.5	5.32	0.1/0.13/0.24	162.9
[2]	90 nm	640	10	67/—/65	6.8	0.19/—/0.23	158.7
[3]	90 nm	340	20	77/71/69	56	0.24/0.48/0.61	162.5
[4]	90 nm	420	20	72/72/70	27.7	0.21/0.21/0.27	160.6
[5]	90 nm	400	10	52/—/—	7	1.08/—/—	143.5
[6]	65 nm	1152	18	67/70/67	17	0.26/0.18/0.26	157.2
[6]	65 nm	1152	9	75/76/72	17	0.21/0.18/0.29	162.2
[7]	65 nm	950	20	69/62/60	10.5	0.11/0.26/0.32	161.8
[8]	65 nm	256	8	81/76/70	50	0.34/0.61/1.21	163.0

Conclusions

- Compensate ELD $> T_s$ in a CT $\Delta\Sigma$ modulator
  - Use a fast loop outside the flash ADC
  - Non-minimum phase NTF
  - $f_{s,max}$ increases by $2\times$ to $3\times$ in a given process technology
- Low latency flash ADC
  - Series switches eliminated from reference subtraction
- Delay free calibrated DAC
  - Alternately calibrated unit current sources for each unit
- Highest sampling rate in a 0.18 μm CMOS process
- Highest signal bandwidth in a 0.18 μm CMOS process

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