

Fig. 2. Compensating  $ELD > T_s$  using a fast loop outside the flash ADC (The dashed path from the input to the loop filter is used to reduce the internal swings and has no effect on the NTF and loop stability.).

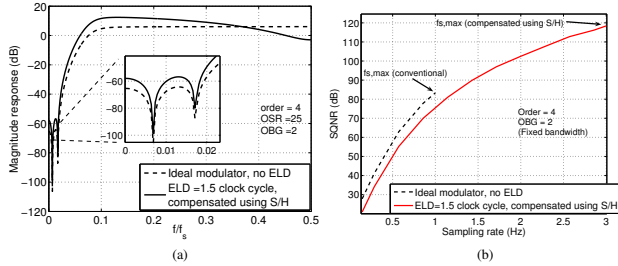


Fig. 3. (a) NTF with ELD compensation using the fast loop in Fig. 2, (b) SQNR versus sampling rate for Fig. 1 and Fig. 2.

$T_s$  and the path  $k_0$  compensates for any ELD in excess of that. As before, the delay that can be compensated by  $k_0$  is limited to  $T_s/2$  and the total delay that can be compensated using the technique in Fig. 2 is  $3T_s/2$  as opposed to  $T_s/2$  in Fig. 1. Given a minimum flash ADC delay  $\tau_{ADC,min}$  in a given process, the highest sampling rate achievable in Fig. 2 is about  $3/2\tau_{ADC,min}$  as opposed to  $1/2\tau_{ADC,min}$  in Fig. 1, implying a  $3\times$  faster CTDSM in a given process.

Fig. 3(a) shows the NTF magnitude responses of Fig. 1 and Fig. 2 for a fourth order modulator with an out of band gain (OBG) of 2 and optimized zeros for  $OSR=25$ . The drooping out of band magnitude is typical of the nonminimum phase NTF realized in Fig. 2. Fig. 3(b) shows the SQNR versus sampling rate in the two techniques for a fixed signal bandwidth of  $1/50$  Hz. 1 Hz corresponds to the maximum sampling rate possible with conventional techniques. The higher OSR possible in Fig. 2 can be used to increase SQNR or signal bandwidth.

### III. MODULATOR ARCHITECTURE

Fig. 2 shows the block diagram of the  $\Delta\Sigma$  modulator designed in this work. A CIFF structure is used in order to avoid multiple DACs loading the high speed flash ADC. A fourth order NTF with optimized zeros and  $OBG=2$  along with the fast feedback loop described in the previous section is used in the modulator. With a four bit quantizer and an over-sampling ratio (OSR) of 25, the SQNR is 96 dB. Feedforward summation of input signal at the loop filter output (dashed path in Fig. 2) eliminates signal contributions from the third and fourth integrators. This reduces the gains for these signals in the summing amplifier, thereby increasing the feedback

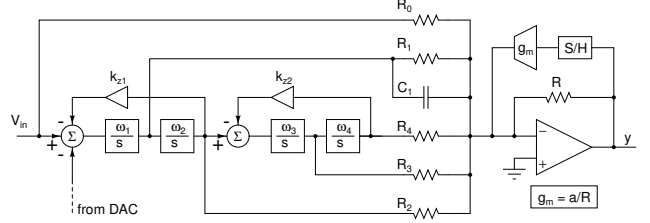


Fig. 4. Fourth order loop filter.

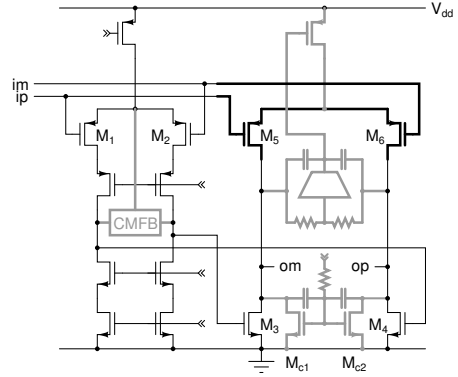


Fig. 5. Feedforward compensated opamp used in the first integrator. Feedforward path is shown in bold, and CMFB paths are shown in gray.

fraction and reducing the delay of the latter. As shown in [7], this does not compromise the antialias property of continuous-time  $\Delta\Sigma$  ADCs. A four bit flash ADC with 3 Vppd full scale follows the loop filter. The loop filter is scaled such that the maximum outputs of the integrators are 1.5 Vppd and only the summing amplifier operates with full output swing. A calibrated four bit DAC completes the feedback loop.

### IV. LOOP FILTER

Fig. 4 shows the loop filter. It consists of four active RC integrators whose outputs are added with appropriate weights through  $R_{1-4}$ . Feedback paths  $k_{z1}$  and  $k_{z2}$  are used to realize the optimized zeros in the NTF. The NTF zeros can be tuned for  $OSR=25$  (16 MHz BW) or  $OSR=12.5$  (32 MHz BW). The input  $V_{in}$  is added at the output of the summing amplifier through  $R_0$  (dashed path in Fig. 2). The output of the first integrator is differentiated using  $C_1$  and added to the output to realize  $k_0$  in Fig. 2. For implementing the fast loop, the output of the loop filter is sampled using an S/H and the sampled output is added to the input of the summing amplifier using a transconductance.

In a CIFF  $\Delta\Sigma$  modulator, the noise and nonlinearity contributed by the loop filter are predominantly due to the opamp used in the first integrator. Therefore the first opamp is required to have a low input referred noise and a high unity gain frequency. Fig. 5 shows the first opamp used in our work. The first stage is a telescopic cascode stage with a pMOS differential pair  $M_{1,2}$ . nMOS common source amplifiers  $M_{3,4}$  form the second stage. The feedforward path is another pMOS differential pair  $M_{5,6}$  which shares the bias current of  $M_{3,4}$ . Using a feedforward structure and sharing the bias current

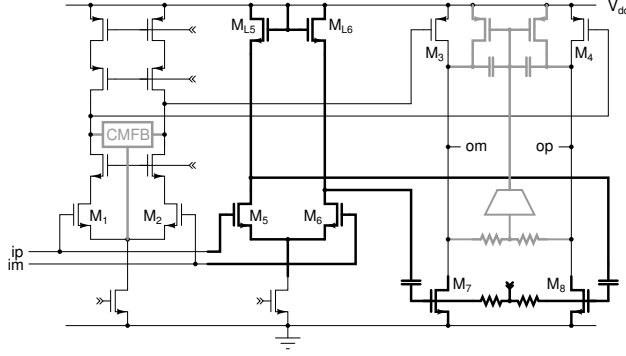


Fig. 6. Feedforward compensated opamp used in the summing amplifier. Feedforward path is shown in bold, and CMFB paths are shown in gray.

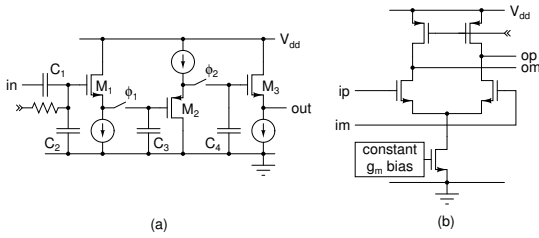


Fig. 7. Fast loop components: (a) One half of the pseudo-differential sample and hold, (b) Differential transconductor.

between  $M_{3,4}$  and  $M_{5,6}$  enable the realization of a high unity gain frequency with a low power consumption. Common mode feedback is provided to the tail current source of  $M_{5,6}$  and augmented for high frequencies through  $M_{c1,2}$ . The opamp consumes 5.5 mW. The opamp used in the second, third, and fourth integrators are scaled down versions of Fig. 5.

The summing amplifier needs to drive the flash ADC with a 3 Vppd output swing. Fig. 6 shows the opamp used in the summing amplifier. The feedforward stage is modified to have two stages—a low gain high speed stage  $M_{5,6}$  followed by common source amplifiers  $M_{7,8}$ —in order to support a high output swing. The latter permit a high output swing while the former provide common mode rejection. For high speed, nMOS transistors are used in both stages of the feedforward path and ac coupling is used between them. The opamp consumes 8.5 mW and has a unity gain frequency of 4.3 GHz while driving the flash ADC.

Fig 7(a) the sample and hold circuit used in the fast loop. The input (3Vppd max) is attenuated by the capacitive divider  $C_{1,2}$ , buffered by M1 and sampled by two buffered track and hold (T/H) stages. The transconductor following the S/H is a differential pair with a fixed-gm-bias (Fig 7(b)).

## V. FLASH ADC AND CALIBRATED DAC

Fig. 8(a) shows the flash ADC. The reference storage capacitors  $C_c$  are refreshed at a rate  $f_s/4$  from capacitors  $C_b$ . A differential resistor ladder is used to generate the references. Absence of switches in the signal path ensures a low latency and capacitive subtraction of references accommodates a large input swing. A cascade of three latches resolves the analog

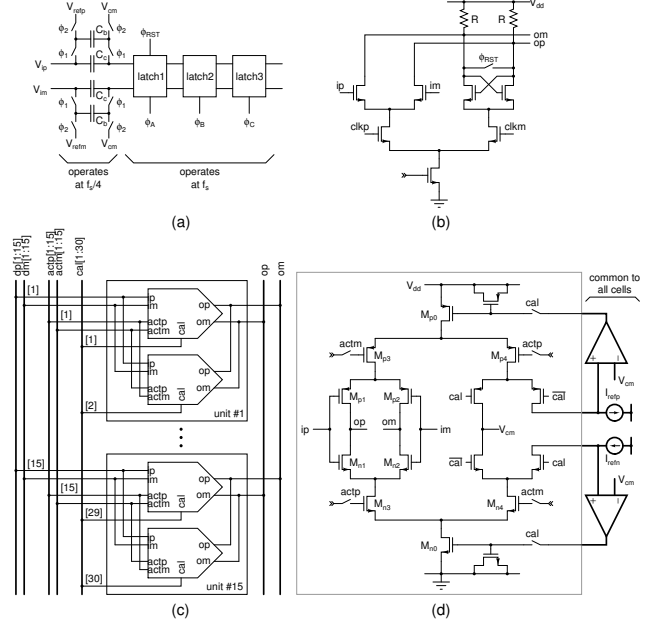


Fig. 8. (a) Flash ADC architecture, (b) CML latch used in the flash ADC, (c) Low latency calibrated DAC architecture, (d) Calibrated current steering cell.

difference into logic levels. Fig. 8(b) shows the first latch. It is a conventional CML latch with reset. The second and third latches are similar, except that they are not reset.

DEM and calibration are commonly used techniques to mitigate the effects of mismatch between DAC elements in multibit  $\Delta\Sigma$  ADCs. Hitherto published topologies for either of these techniques include logic circuits between the flash output and the DAC input, adding significant ELD. To eliminate this ELD, a new calibrated current steering DAC topology (Fig. 8(c)) is proposed. Each of the 15 units of the 4 bit DAC consists of two current steering cells driven by the retimed input. At any instant, only one of these two, activated by actp/actm, contributes to the output. The inactive cell is calibrated during that time. After calibration the cell is activated. The inactive cells in all 15 units are calibrated in succession. The cycle then repeats for the other cell in each unit. Since the digital inputs are directly connected to the DAC cells, ELD due to DEM/calibration logic circuits is eliminated at the expense of twice the power dissipation in the DAC current cells. Fig. 3(b) shows the schematic of each cell. Use of both pMOS and nMOS current sources ( $M_{p0}$  and  $M_{n0}$ ) switched in a complementary fashion reduces the thermal noise for a given full scale current.  $M_{n3,4}$  and  $M_{p3,4}$  are used as cascode devices by tying their gates to appropriate bias voltages. During the inactive period, for 1/15th of the time, the current sources are being calibrated against  $I_{refp}/I_{refn}$ , and for the rest, they are terminated by  $V_{cm}$ .

## VI. MEASURED RESULTS

The design is implemented in a 0.18  $\mu\text{m}$  CMOS process. Fig. 9 shows the layout and chip photograph. It consumes 47.6 mW from a 1.8 V supply. Fig. 10(a,b) show the output

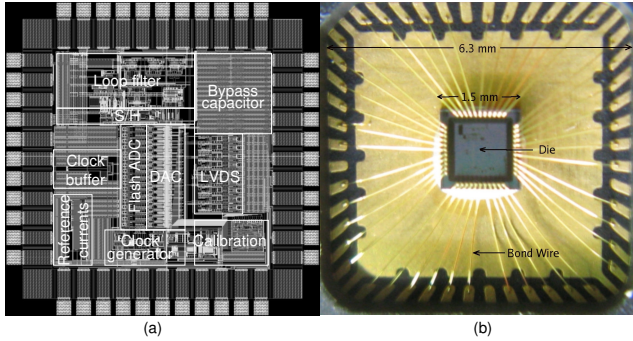


Fig. 9. (a) Chip layout, (b) Packaged chip.

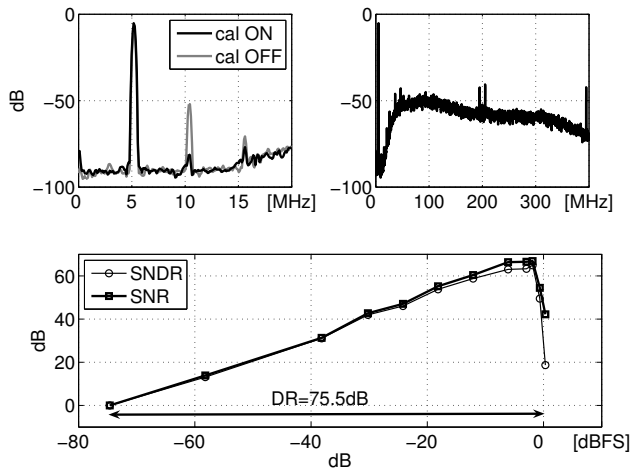


Fig. 10. Measured performance at 800 MS/s and OSR=25 (16 MHz bandwidth).

spectrum with  $f_s = 800$  MS/s,  $OSR = 25$ , and a  $-1.9$  dBFS input at 5.2 MHz. With DAC calibration turned on, the second and third harmonics are more than 70 dB below the signal. Fig. 10(c) shows the SNR and SNDR as a function of the input signal amplitude. The modulator is stable up to  $-1.8$  dBFS inputs.  $DR$ ,  $SNR_{max}$ , and  $SNDR_{max}$  are 75 dB, 67 dB, and 65 dB respectively. Fig. 11(a,b) show the output spectrum with  $f_s = 800$  MS/s,  $OSR = 12.5$ , and a  $-1.3$  dBFS input at 5 MHz. In this mode, the  $DR$ ,  $SNR_{max}$ , and  $SNDR_{max}$  are 64 dB, 57 dB, and 57 dB respectively. Table I summarizes the performance and compares it to other wideband  $\Delta\Sigma$  ADCs.

## VII. CONCLUSIONS

ELD compensation using a fast loop outside the ADC, a low latency flash ADC, and a delay free calibrated DAC topology enable  $\Delta\Sigma$  ADCs with much higher sampling rates than conventional architectures. The 800 MHz sampling rate and 32 MHz signal bandwidth of the ADC presented here are the highest reported in a  $0.18\mu\text{m}$  process.  $P_d/(2BW \cdot 2^{(SNR_{max}-1.76)/6.02})$  and  $DR + 10\log_{10}(BW/P_d)$ , commonly used FOMs for comparing ADCs, are 0.81 pJ and 160.3 dB respectively for the ADC presented here in the 16 MHz bandwidth mode, indicating a power efficiency close to the best among wideband  $\Delta\Sigma$  ADCs in this process.

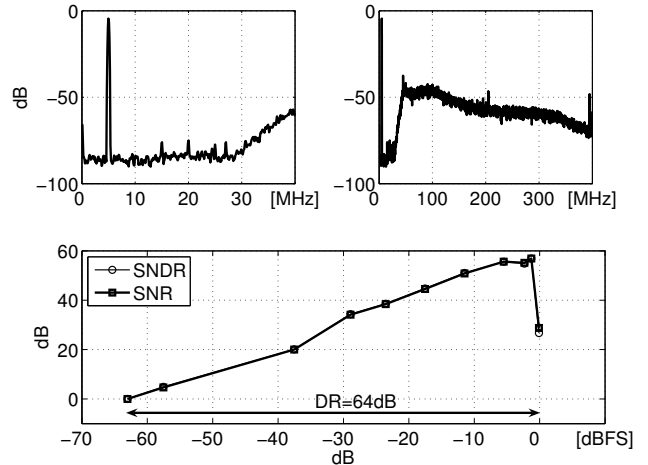


Fig. 11. Measured performance at 800 MS/s and OSR=12.5 (32 MHz bandwidth).

TABLE I  
PERFORMANCE SUMMARY

	This work	[2]	[3]	[8]	[9]
Process	0.18 $\mu\text{m}$	0.13 $\mu\text{m}$	0.18 $\mu\text{m}$	0.13 $\mu\text{m}$	0.18 $\mu\text{m}$
Active area	1 mm <sup>2</sup>	1.2 mm <sup>2</sup>	1 mm <sup>2</sup>	0.45 mm <sup>2</sup>	2.6 mm <sup>2</sup>
Supply voltage	1.8 V	1.2 V	1.8 V	1.5 V	1.8 V
Sampling rate (MHz)	800	640	300	950	400
Full scale	3Vppd				
$P_d$ (mW)	47.6	20	20.7	87	48
BW (MHz)	16	32	20	15	25
DR (dB)	75	64	80	70	69
SNR <sub>max</sub> (dB)	67	57	76	67.2	68.5
SNDR <sub>max</sub> (dB)	65	57	74	64.2	67.7
FOM1 [DR] (pJ)	0.32	0.57	0.06	0.27	0.42
FOM1 [SNR <sub>max</sub> ] (pJ)	0.81	1.29	0.1	0.37	0.24
FOM1 [SNDR <sub>max</sub> ] (pJ)	1.02	1.29	0.12	0.52	0.34
FOM2 (dB)	160.3	152.3	170	158.6	163.6

$$\text{FOM1 [XX]} = P_d / (2BW \cdot 2^{(XX-1.76)/6.02}); \text{FOM2} = DR + 10\log_{10}(BW/P_d)$$

## REFERENCES

- [1] M. Keller et al., "A comparative study on excess-loop-delay compensation techniques for continuous-time  $\Sigma\Delta$  modulators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 11, pp. 3480-3487, Dec. 2008.
- [2] G. Mitteregger et al., "A 20-mW 640-MHz CMOS continuous-time  $\Delta\Sigma$  ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB," *IEEE Journal of Solid State Circuits*, vol. 41, no. 12, pp. 2641-2649, Dec. 2006.
- [3] K. Reddy and S. Pavan, "A 20.7-mW continuous-time  $\Delta\Sigma$  modulator with 15-MHz bandwidth and 70-dB dynamic range," *Proc. 2008 ESS-CIRC*, Sep. 2008, pp. 210-213.
- [4] J. Harrison and N. Weste, "Analytic limitations on sigma-delta modulator performance," *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 3, 2000, pp. 746-749.
- [5] V. Singh et al., "Compensating for quantizer delay in excess of one clock cycle in Continuous-Time  $\Delta\Sigma$  Modulators," *IEEE Transactions on Circuits and Systems: Part II Express Briefs*, vol. 57, no. 9, pp. 676-680, Sep. 2010.
- [6] A. Yahia et al., "Bandpass delta-sigma modulators synthesis with high loop delay," *Proc. IEEE ISCAS*, vol. 1, 2001, pp. 344-347.
- [7] S. Pavan and P. Sankar, "Power reduction in continuous-time delta-sigma modulators using the assisted opamp," *IEEE Journal of Solid State Circuits*, vol. 45, no. 7, pp. 1365-1379 July 2010.
- [8] M. Park and M. Perrott, "A 78dB SNDR 87mW 20MHz Bandwidth continuous-time  $\Delta\Sigma$  ADC with VCO based integrator and quantizer implemented in 0.13 $\mu\text{m}$  CMOS", *IEEE Journal of Solid State Circuits*, vol. 44, no. 12, pp. 3344-3358 Dec. 2009.
- [9] C. Y. Lu et al., "A 25 MHz bandwidth 5th-order continuous-time low-pass sigma-delta modulator with 67.7 dB SNDR using time-domain quantization and feedback," *IEEE Journal of Solid State Circuits*, vol. 45, no. 9, pp. 1795-1807 July 2010.