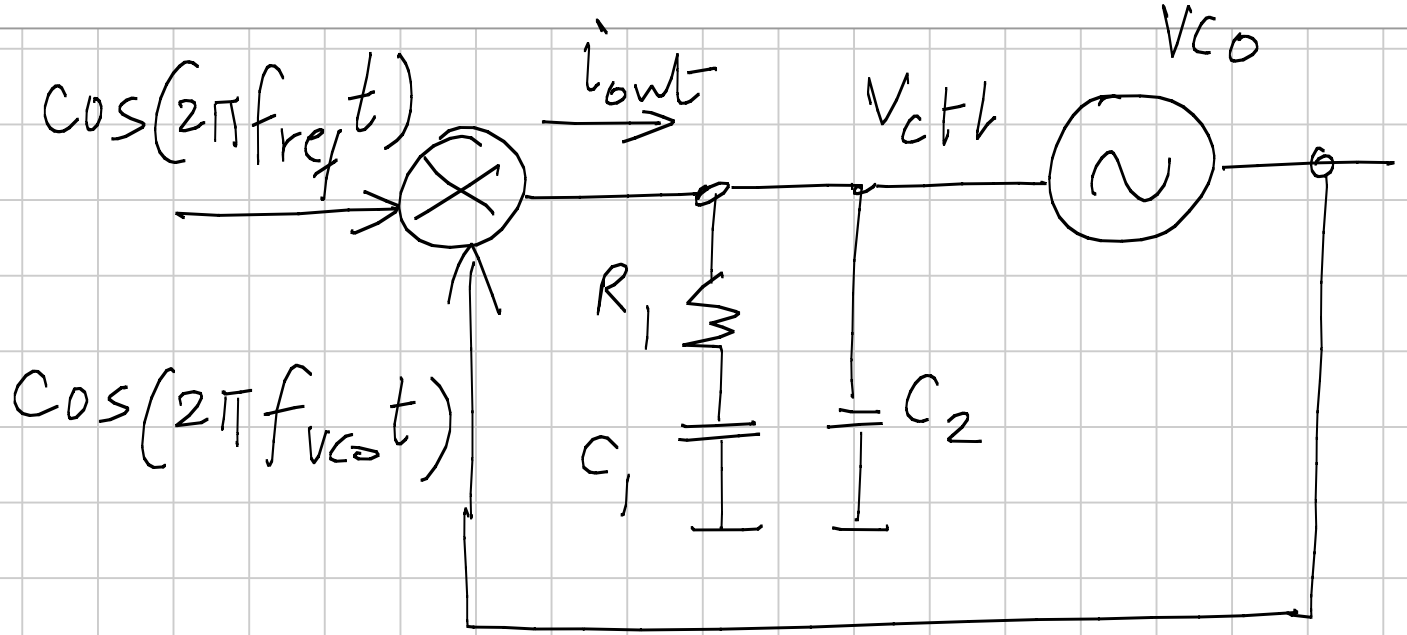
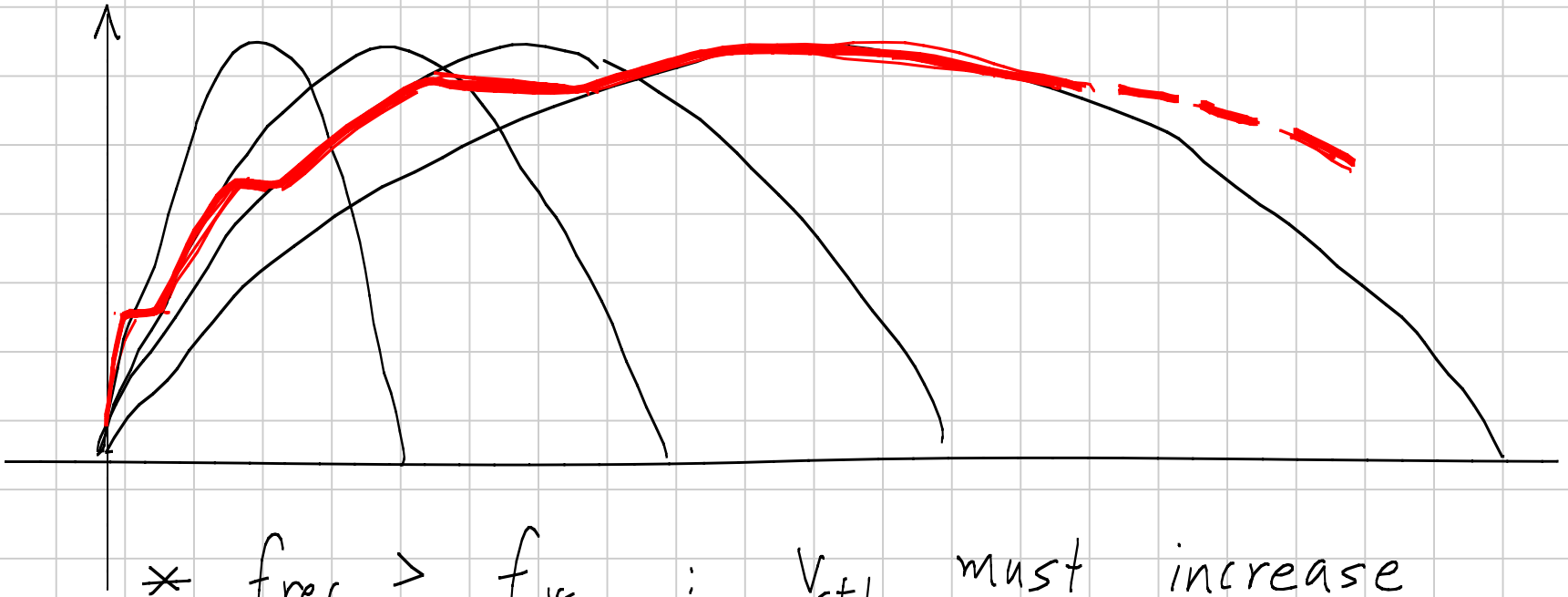
PLL capture process

Note Title 15-11-2007

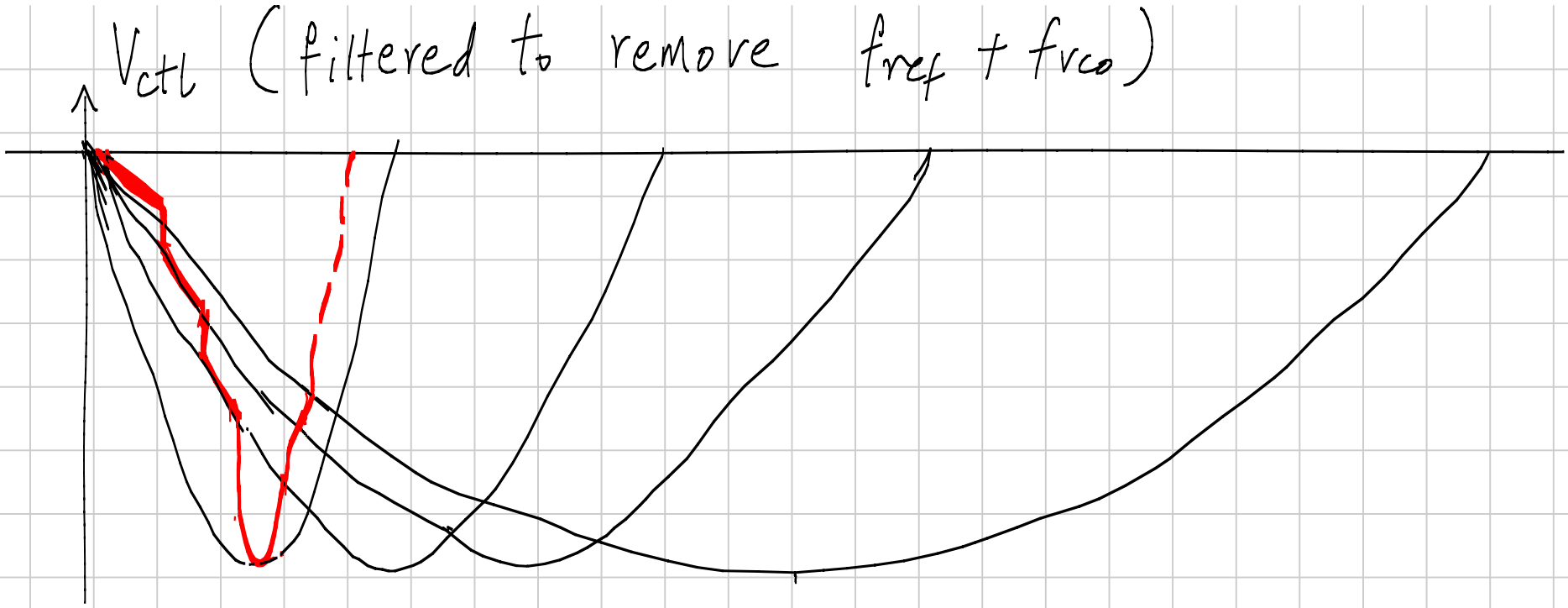


* $f_{ref} + f_{VCO}$ filtered out
* $|f_{ref} - f_{VCO}|$ not filtered out

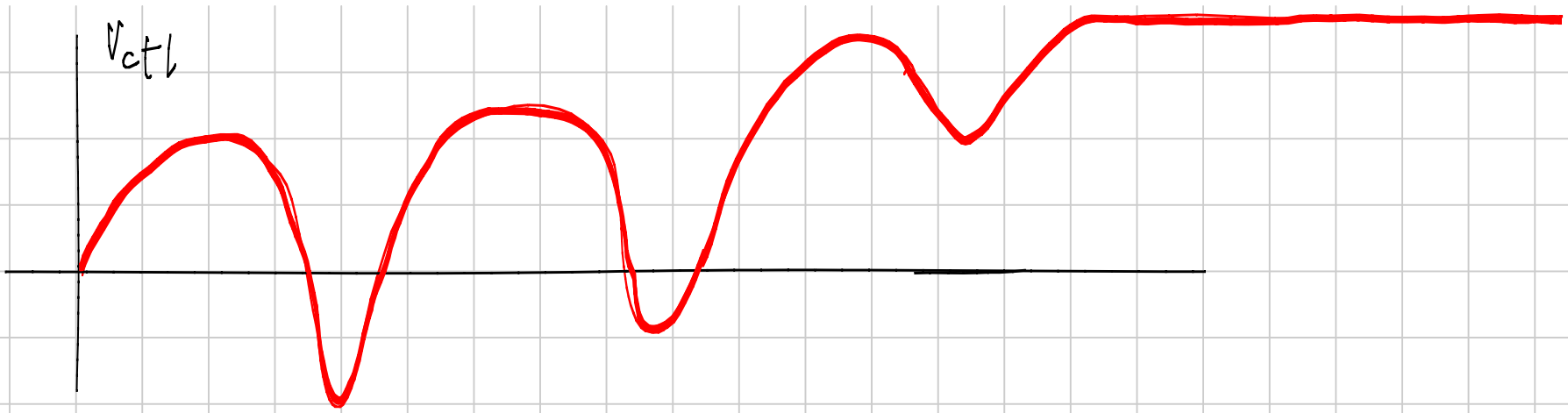
V_{ctl} (filtered to remove $f_{ref} + f_{vco}$)



* $f_{ref} > f_{vco}$: V_{ctl} must increase
* If V_{ctl} increases, it results in a progressively lower $|f_{ref} - f_{vco}|$ and a wider positive pulse

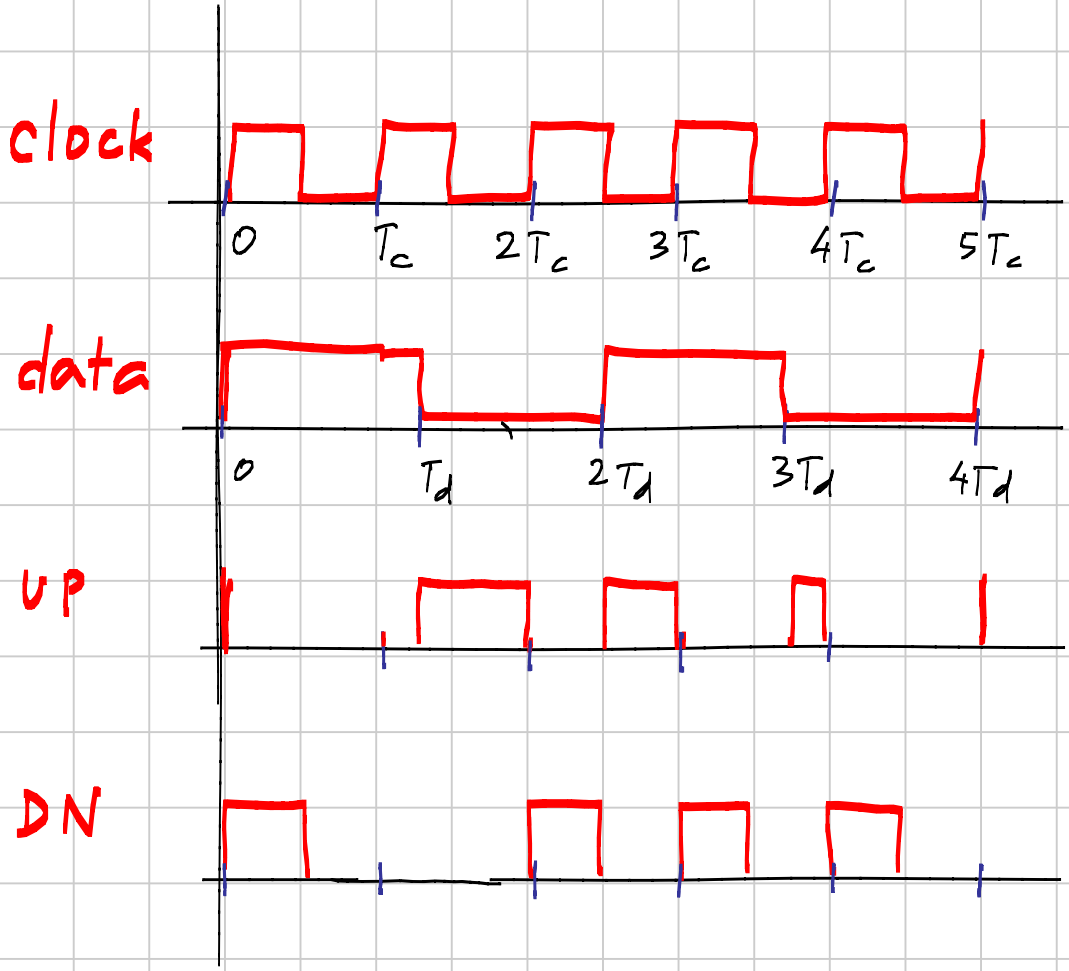


* $f_{ref} > f_{vco}$: V_{ctl} must increase
* If V_{ctl} decreases, $|f_{ref} - f_{vco}|$ progressively increases and results in a narrower negative pulse.



* Average V_{ctl} increases progressively, resulting in a higher average frequency, eventually resulting in capture
* If $|f_{ref} - f_{vco}|$ is also attenuated by the loop filter, capture may not occur (or occur very slowly)

Hogge phase detector with frequency difference between clock and data



* Pattern repeats after $5T_c$
* $5T_c = 4T_d$
* $f_c - f_d = \frac{1}{T_c} - \frac{1}{T_d}$

  $= \frac{1}{T_c} - \frac{4}{5}\frac{1}{T_c} = \frac{1}{5T_c}$
* UP − DN has a component at the difference frequency