Phase locked loop:

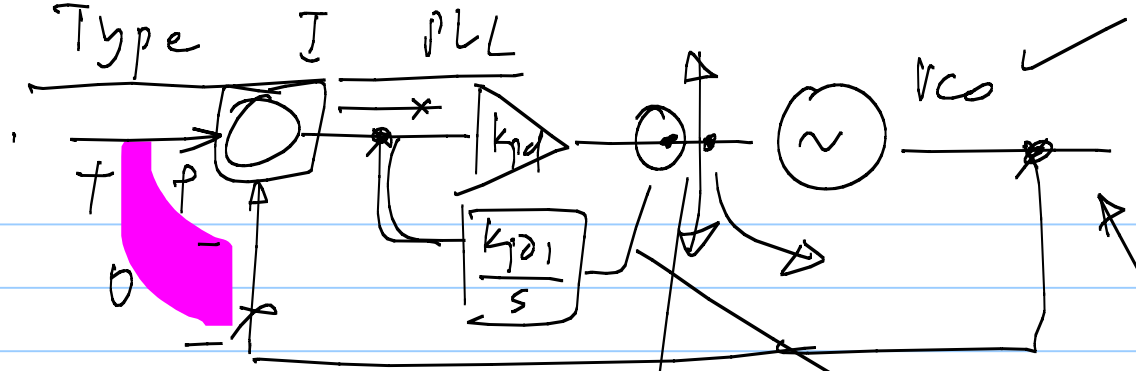
Note Title 02-11-2007

* Type II loop
  Loop filter ~ $\frac{1 + s/\omega_z}{s}$
* Extra poles to filter out ref. feedthrough
* BW: $\frac{2\pi \cdot K_{pd} \cdot K_{vco}}{N}$ rad/s
* Low pass : Input phase to o/p phase
  high pass : Vco phase to o/p phase
  Band pass : control node to o/p phase

C D R

* Hogge phase detector (in place of 3-state PD)
* Loop gain $\propto$ transition density
* Limit on # CID
* Recovered clock & data.
* No divider in the feedback path

Type I PLL



$(\pm\pi)$

$\pm\pi \cdot K_{pd}$

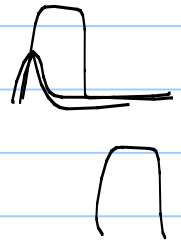
$f_0 \pm \pi \cdot K_{pd} \cdot K_{vco}$

f_0

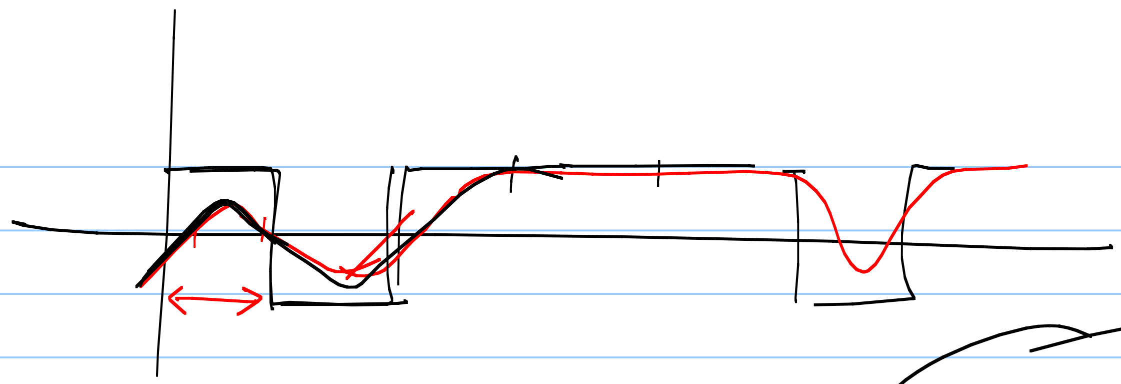
$f_0 + \Delta f$

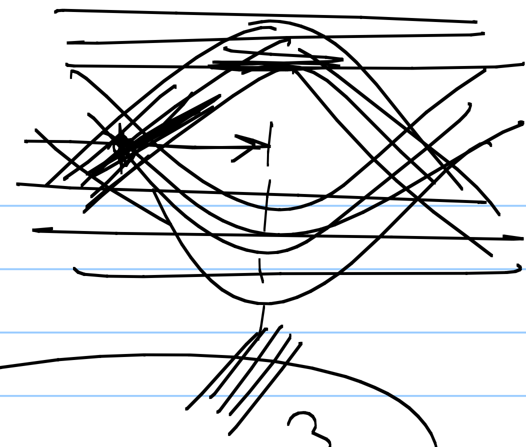
Type II PLL

* Voltage limitation
* VCO range limit
* PFD/CP : freq. limitations



cos(
N
A
B



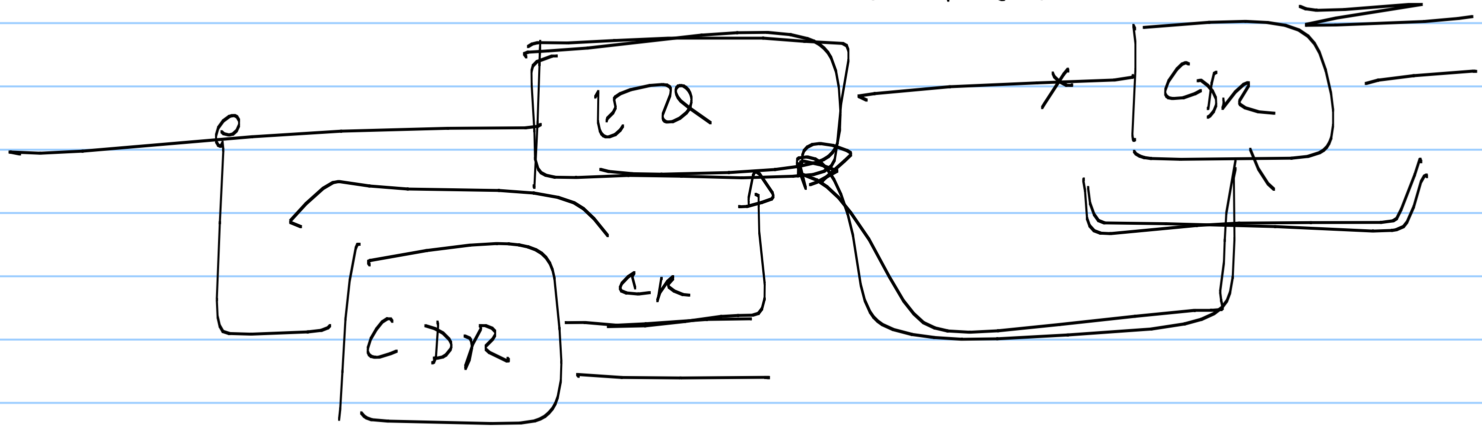


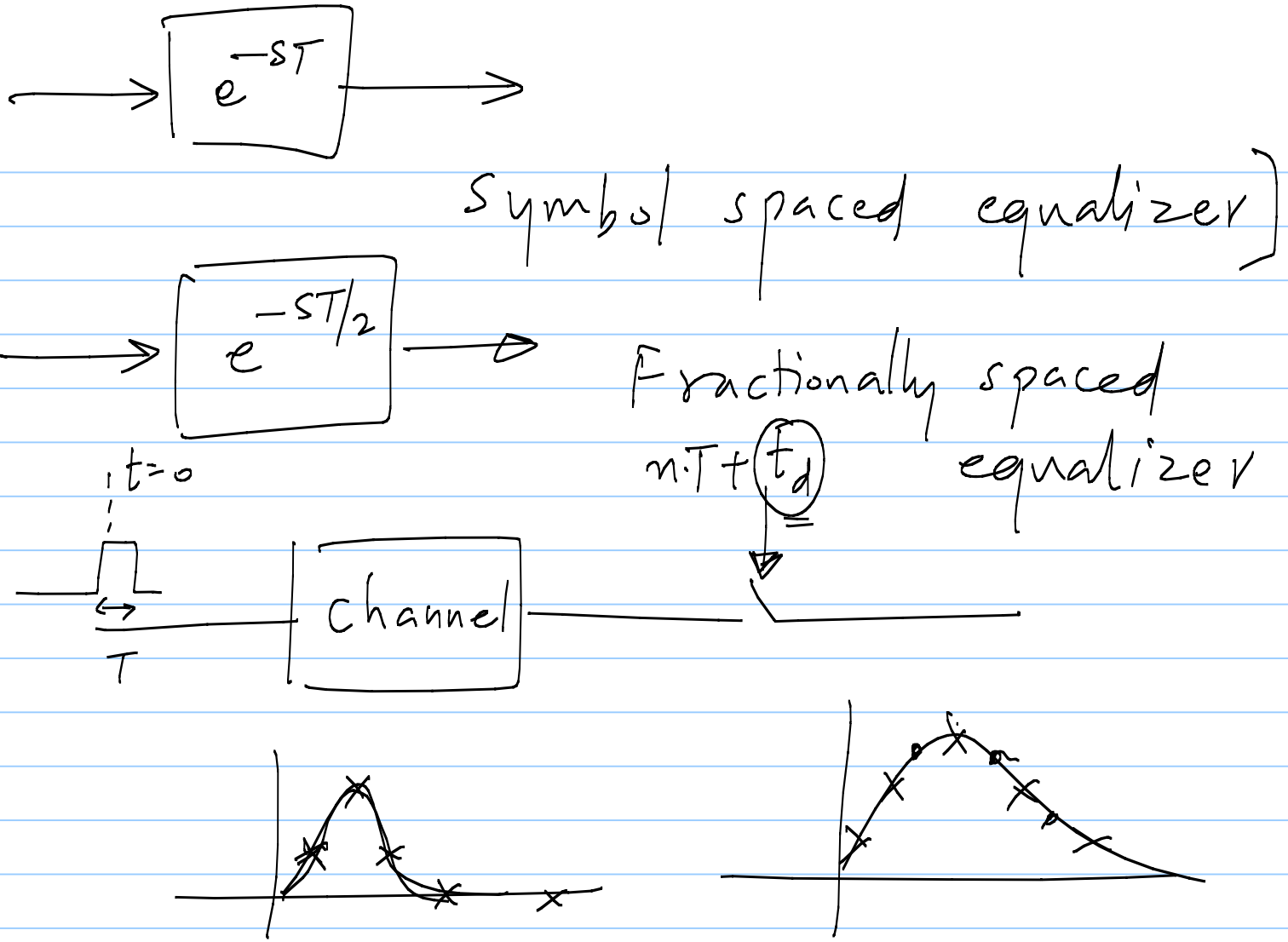
$\frac{S}{N}$

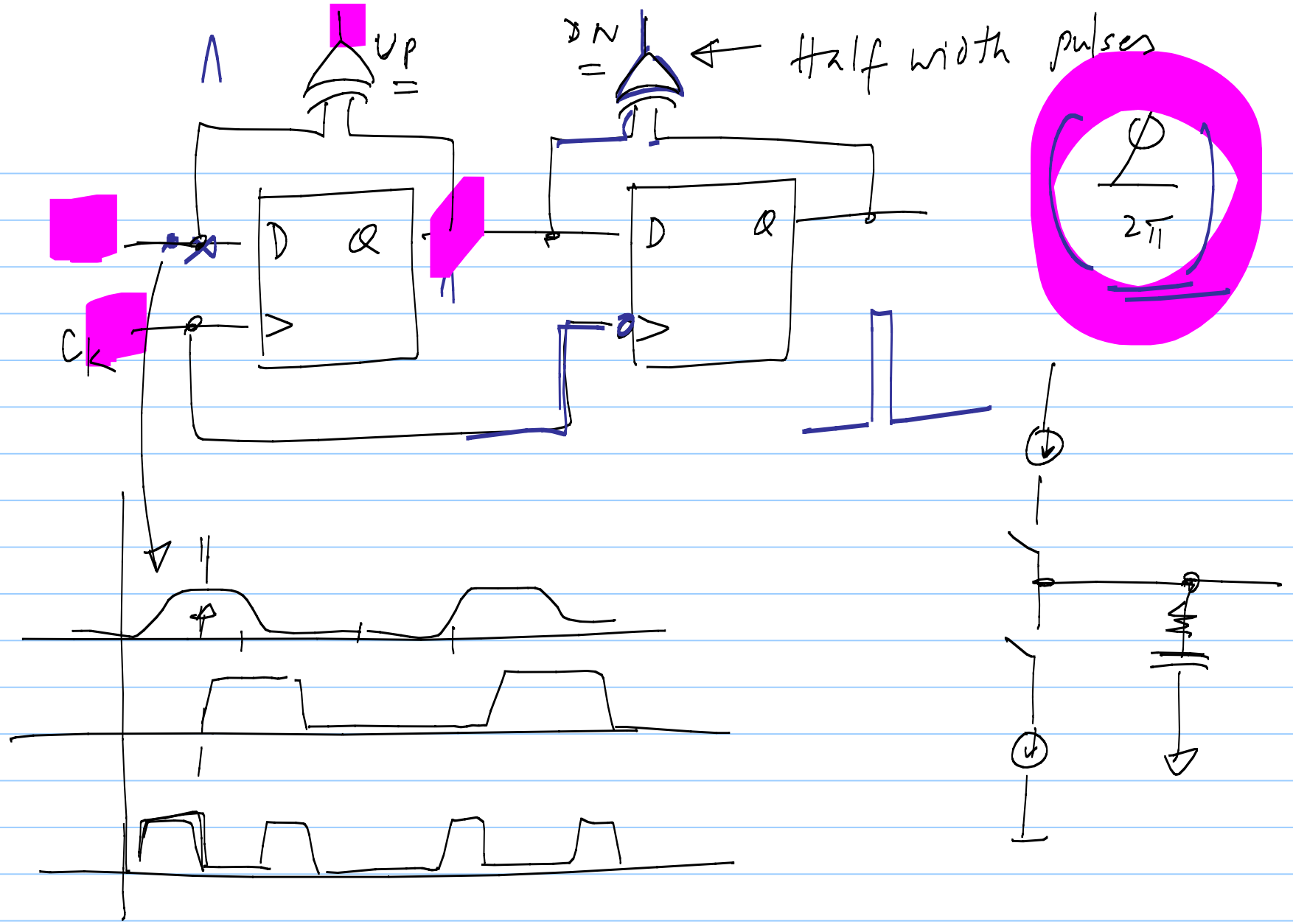
BER $\sim 10^{-3}$

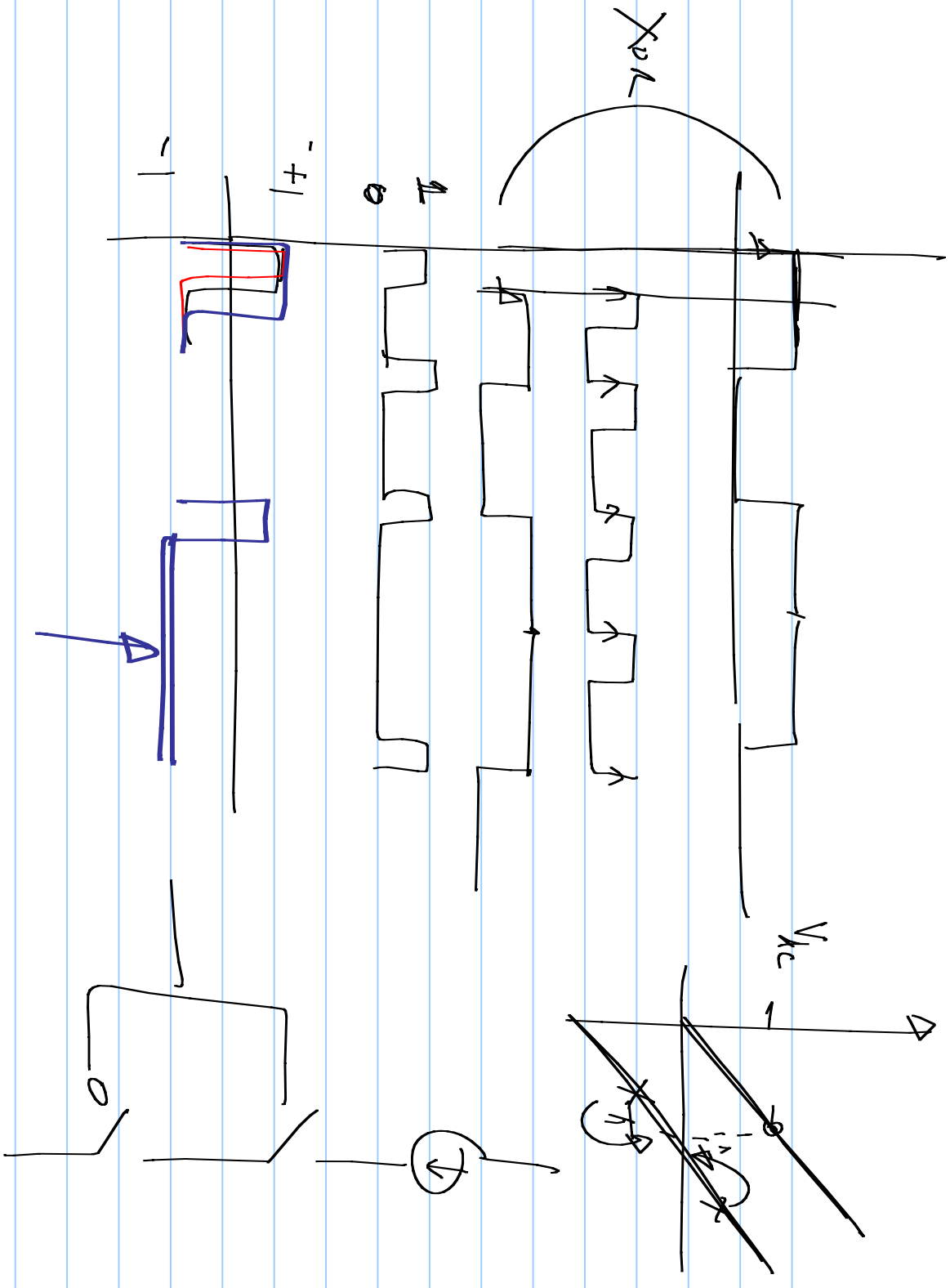
Data:

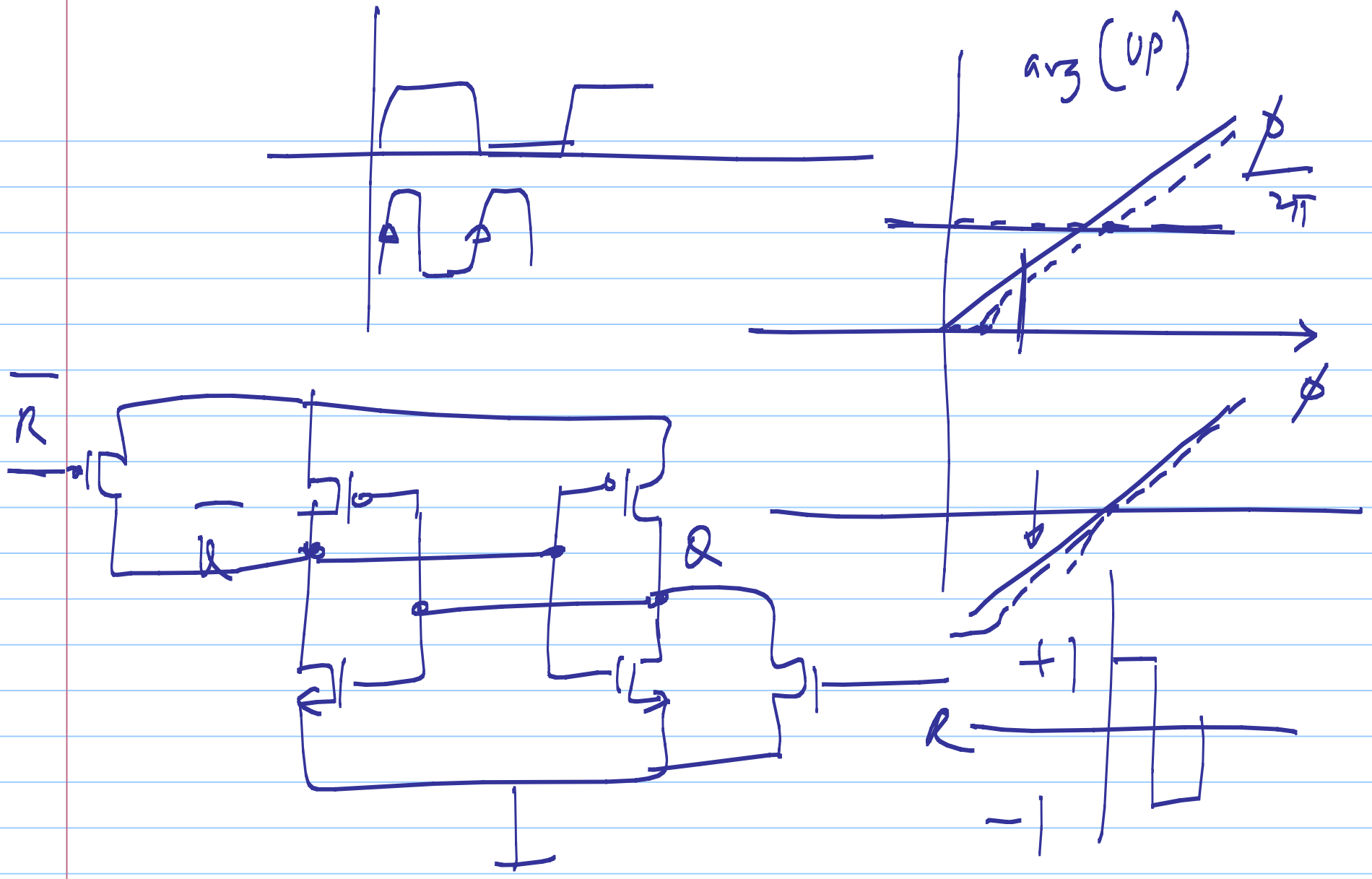
10^{-12}

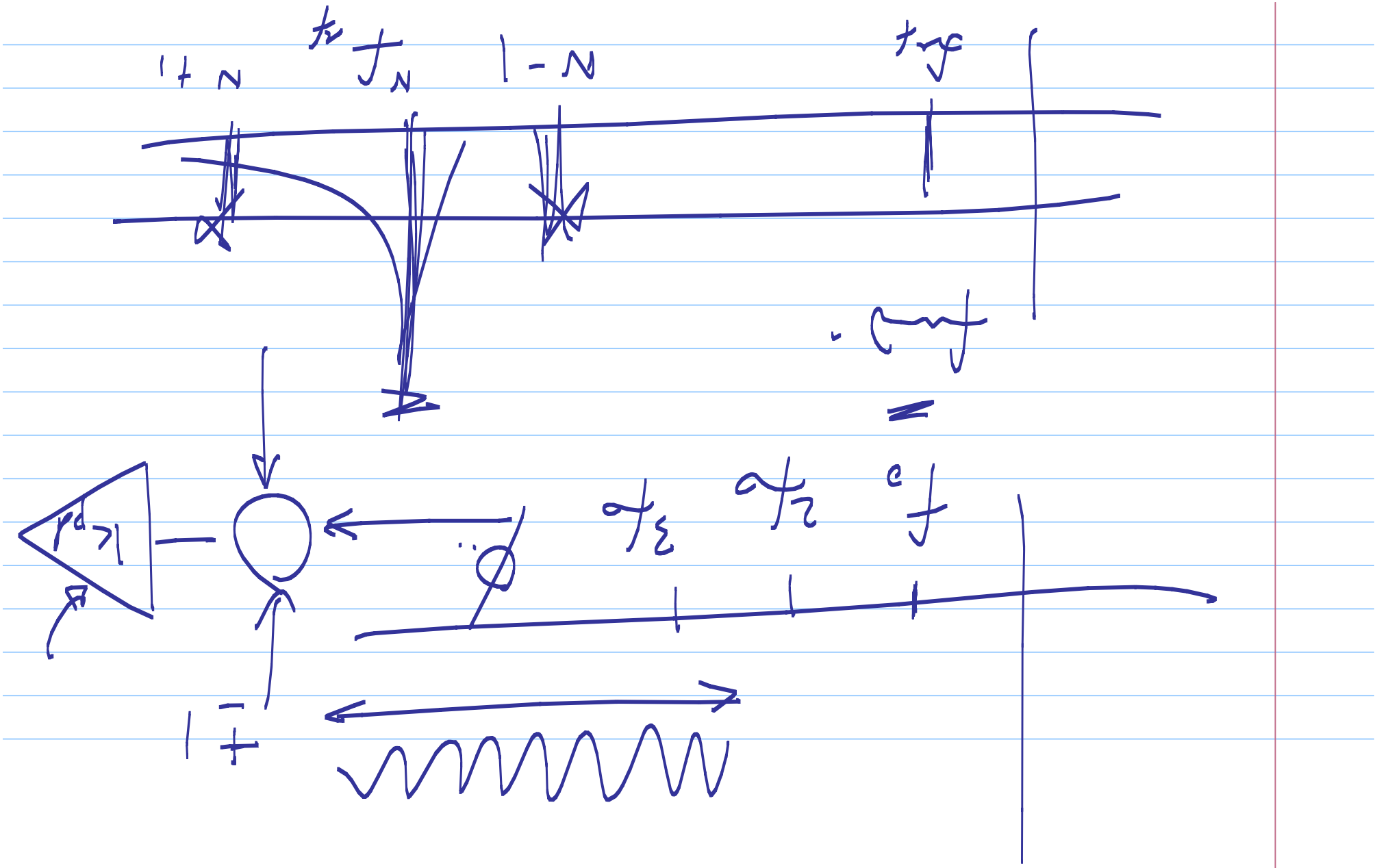


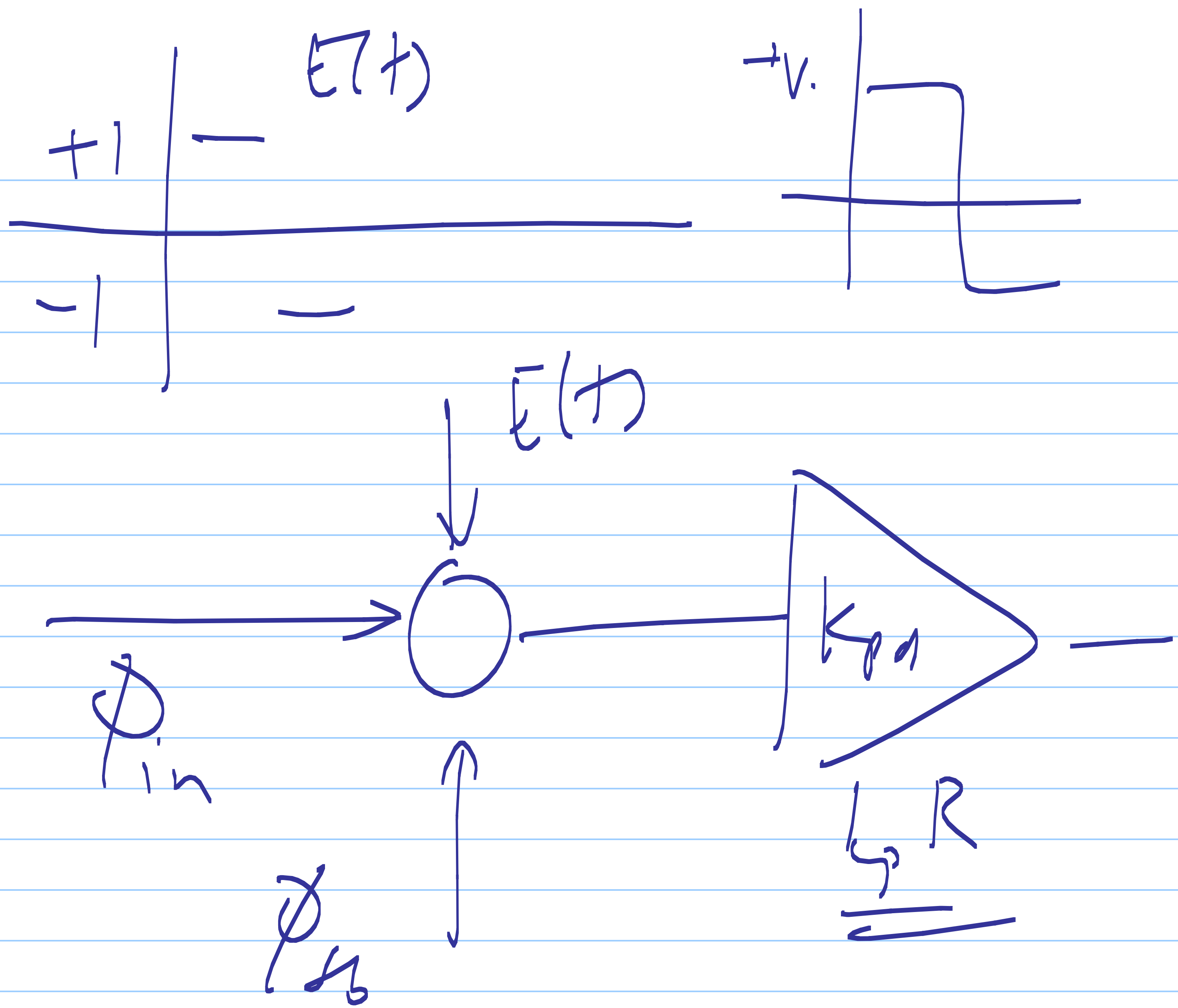

e^{-sT}
Symbol spaced equalizer
$e^{-sT/2}$
Fractionally spaced equalizer
$n \cdot T + t_d$
t=0
T
Channel


UP
DN
Half width pulses
D
Q
D
Q
CK
2π


-1
+1
0
1
0
1


avg (up)
$\frac{\phi}{2\pi}$
ϕ
$\bar{R}$
Q
+1
R
−1


1 + N
1 - N



E(t)
+1
-1
+V.
E(t)
Kpd
φin
φfb
R