4) Bias current A Vref to make minimize ground node capacitance
3) Ref: Branch current limited
2) Fail currents are tuned
1) If pairs in parallel switch merits:
- Receiver biasing:
  - More headroom
  - Cascode: Better accuracy, needs
  - Bias accuracy.
  - Variations.

- Swing independent of resistor
  - $R$
  - Bias current $V_{BE}$ to make
    - $I_{min}$ of final node (capacitance)
  - $I_{ref}$ branch current limited
  - Tail currents are fixed

1. Diff pairs in parallel
2. Transmitter: