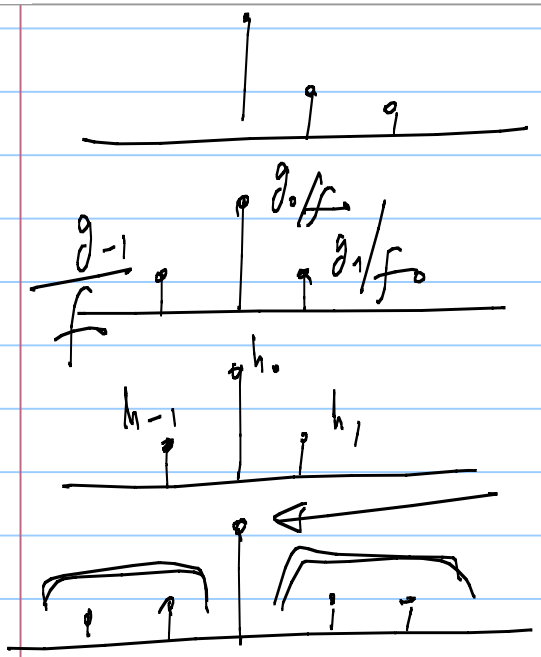
Equalizer design

Note Title 04-09-2007

① $g_0 = 1$ → g_{-1}, g_1

② g_0 : cursor in the equalized channel is 1

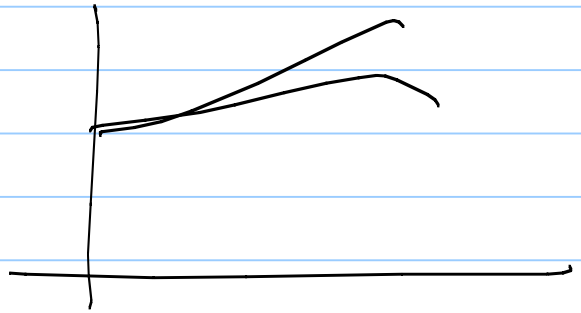
$g_0 = 2$ → g_{-1}, g_1



$\frac{g_{-1}}{g_0}, \frac{g_1}{g_0}$

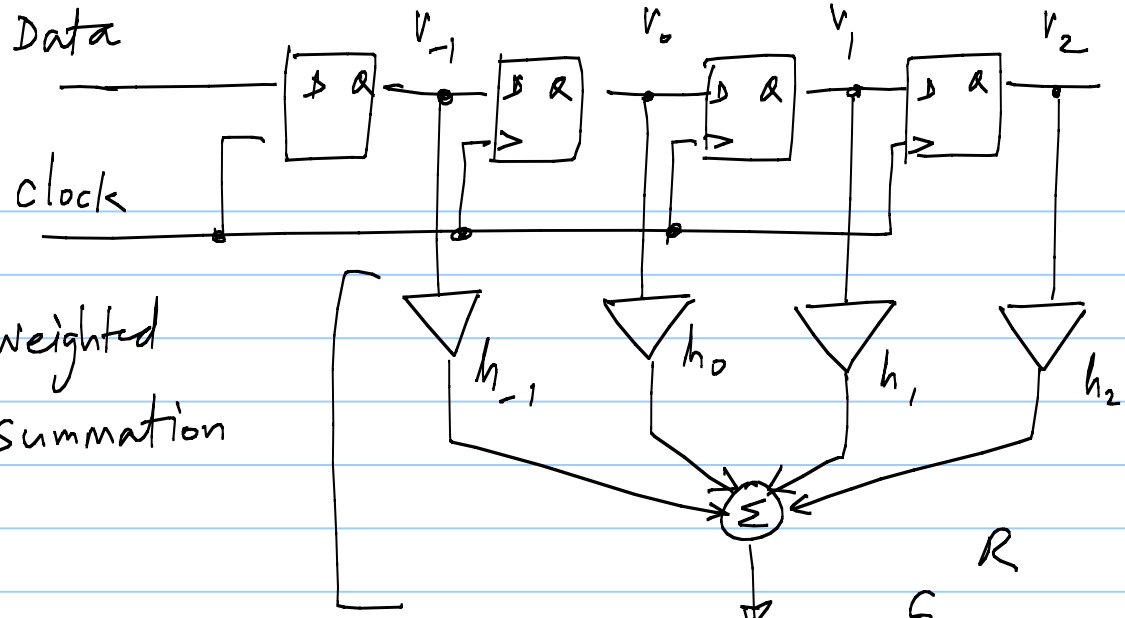
$g_0 h_0 + g_{-1} h_1 + g_1 h_{-1} = f_0$

$(g_{-1} \quad g_0 \quad g_{+1})\ \alpha$



Tx FIR equalizer

* Inputs: digital
* Can use FF's to delay the data



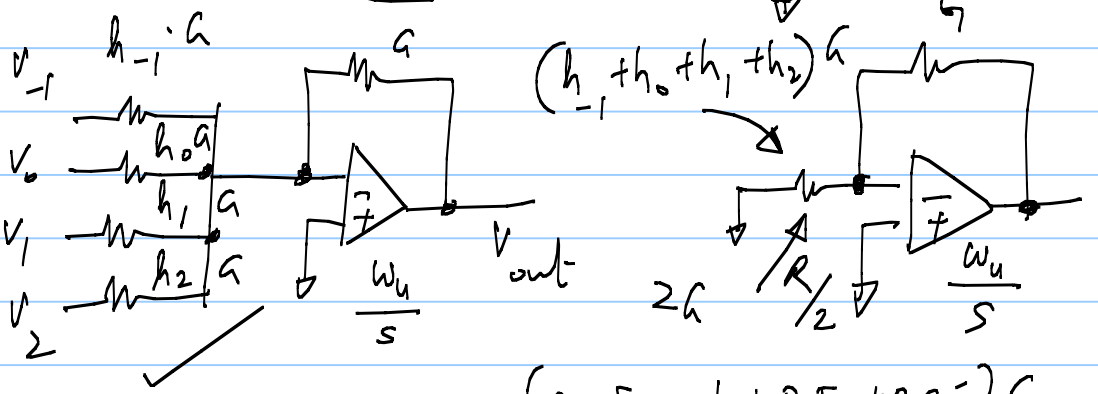
Loop gain $= \frac{w_u}{3s}$

$$e^{-\frac{w_u}{3}t}$$

$$e^{-\frac{w_u}{3}\cdot T_s} = 0.01$$

$$\frac{w_u}{3}\cdot T_s = 5$$

$$w_u = 15\, f_s = 15\ \text{Grad/s} \quad \text{for} \quad f_s = 1\ \text{Gb/s}$$



$(0.25 + 1 + 0.5 + 0.25)G$

$= 2G$

* Feed back circuits - difficult at high frequencies
* Open loop circuits

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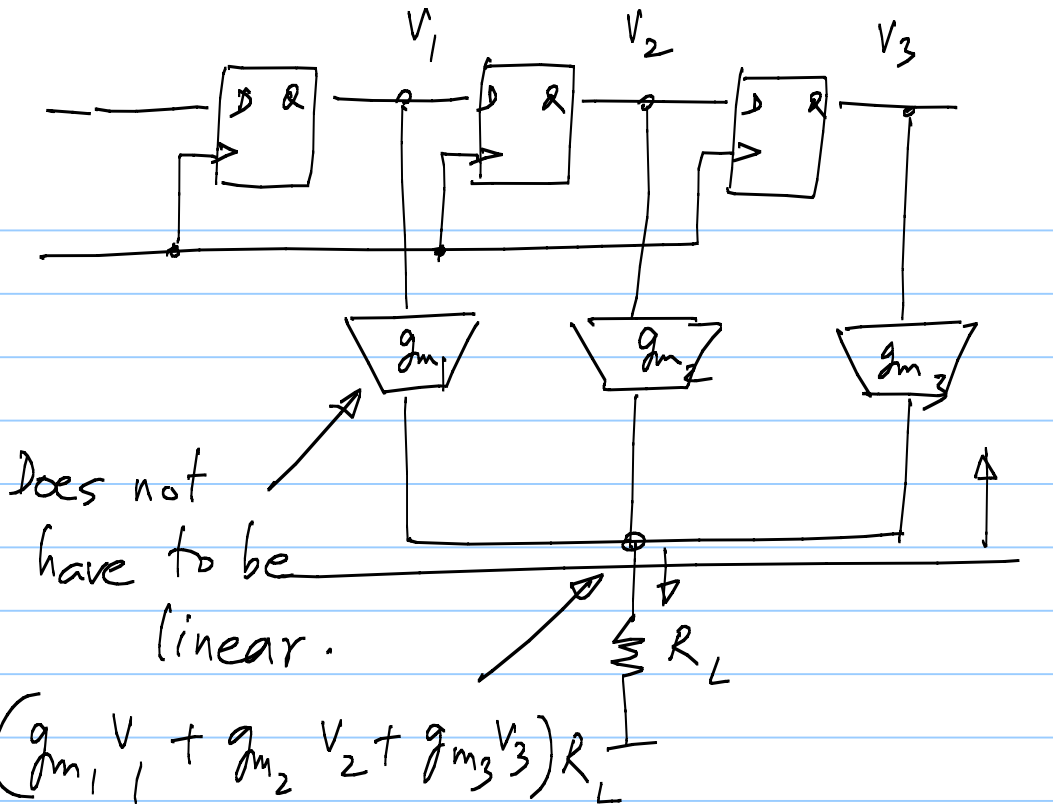
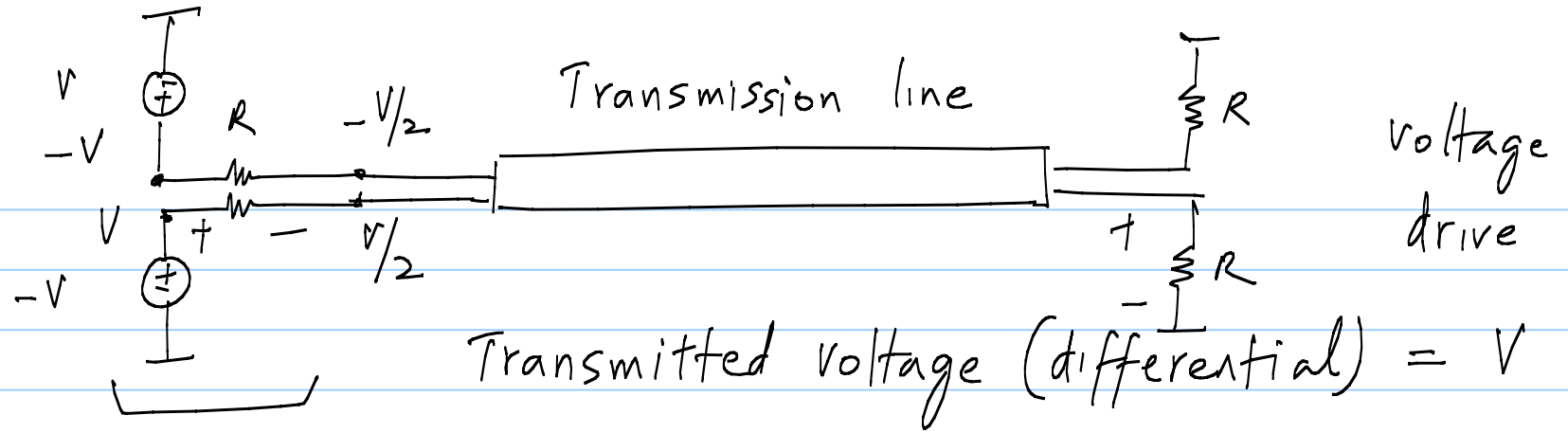
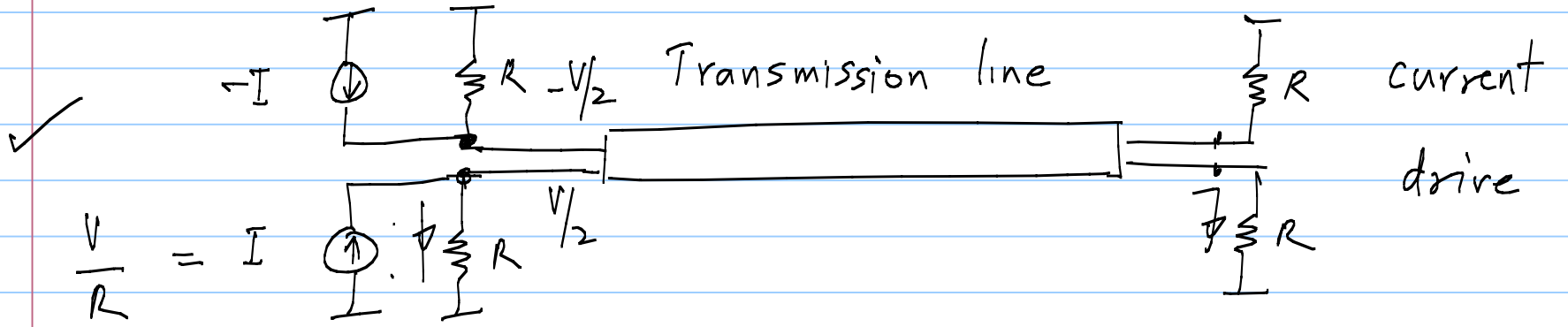
* Weighted summation using transconductors
* Input: binary data

Transconductors don't have to be linear





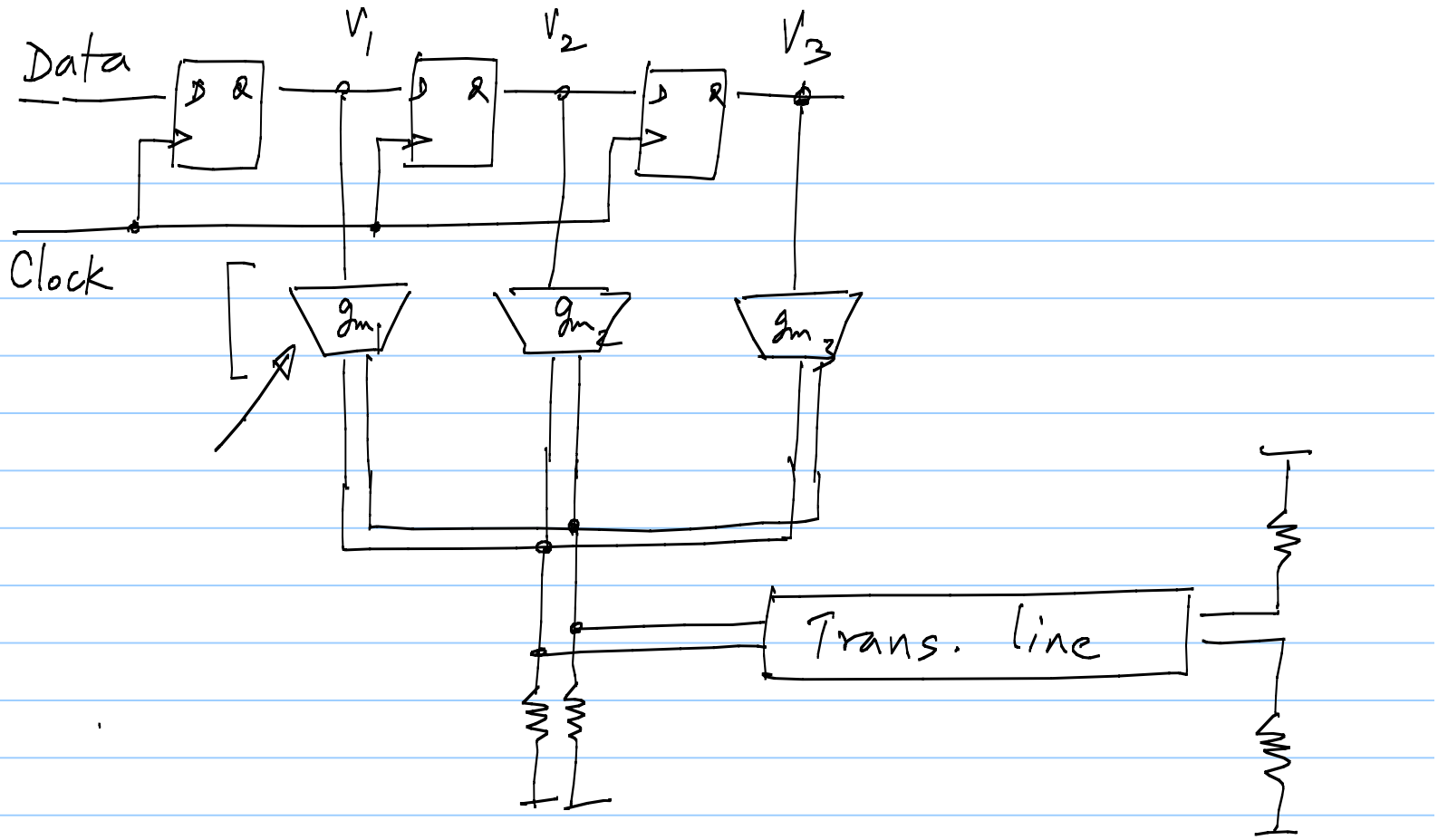
Transmitted voltage (differential) = V



$\frac{V}{R} = I$

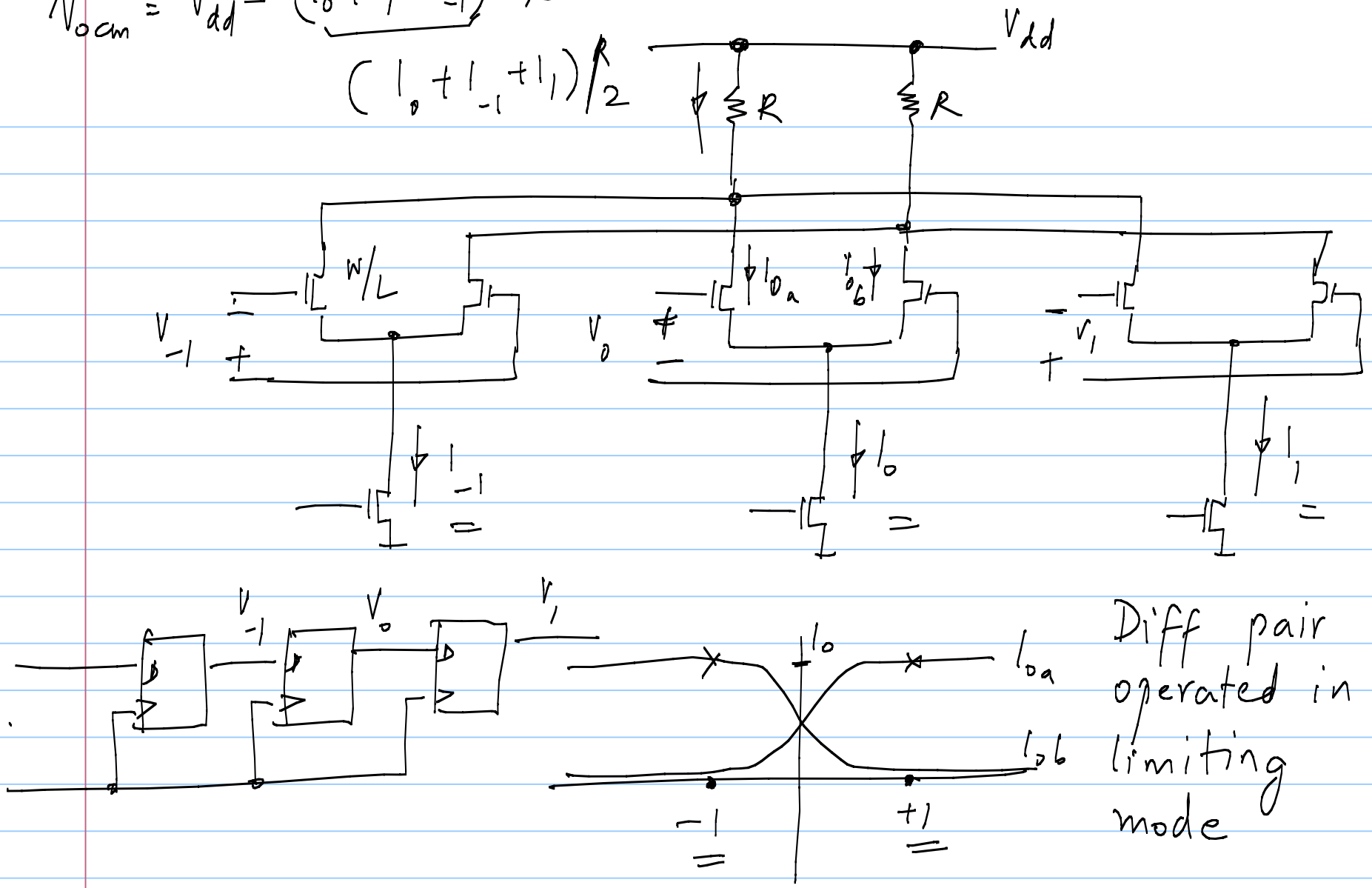
Current drive preferable

* Easier to make current sources than voltage sources
* Largest voltage with voltage drive = 2× " " " current drive.


Data
D
Q
V_1
V_2
V_3
Clock
g_{m_1}
g_{m_2}
g_{m_3}
Trans. line

$$V_{ocm} = V_{dd} - (I_0 + I_1 + I_{-1})R/2$$

$$(I_0 + I_{-1} + I_1)R/2$$



Diff pair operated in limiting mode

Tx linear equalizer

* Chain of FFs to delay the signal
* Differential pairs for each tap
* Tap weights are set by tail currents.

Cursor: +1 $-(0 : 0.125 : 0.5)$

Pre-cursor & post cursor: 0 to -0.5 =