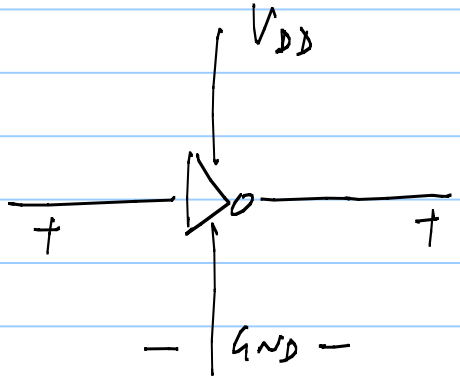
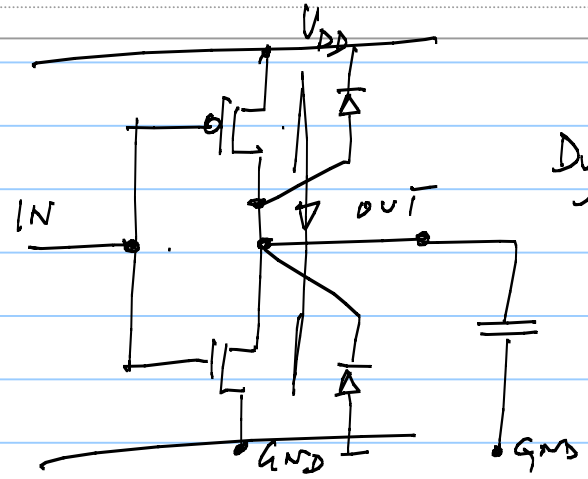
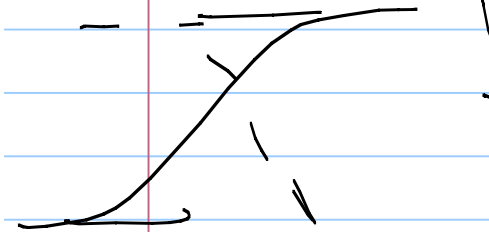
CMOS logic

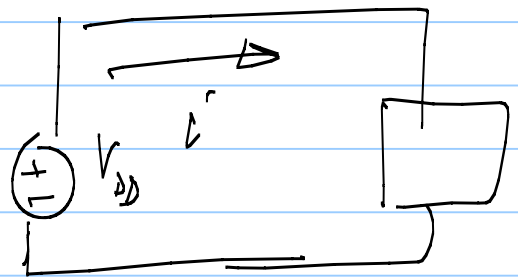
Note Title 06-08-2007







$V_{Th} < V_{in} < V_{DD} - V_{Tp}$

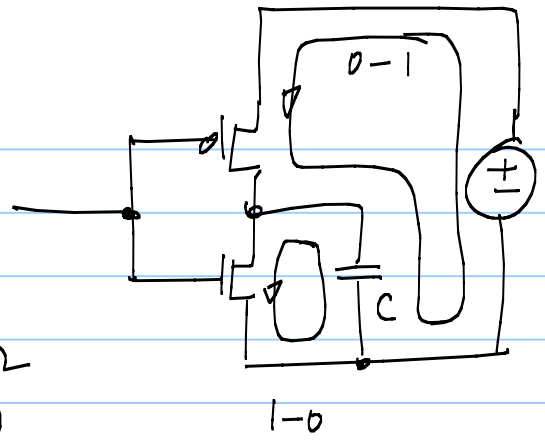


static: leakage
- diode
- subthreshold conduction

Dynamic power
- charging the load capacitor

Crowbar current
- nMOS & pMOS on
- steeper signals at the input

$P = C \cdot V_{DD}^2 \cdot f$ → # 0 → 1 transitions in a second



$$i = \frac{C \cdot dV_{out}}{dt}$$

$$P = C \cdot V_{DD}^2 \cdot f$$

$$E = \int_0^\infty V_{DD} \cdot i(t)\, dt$$

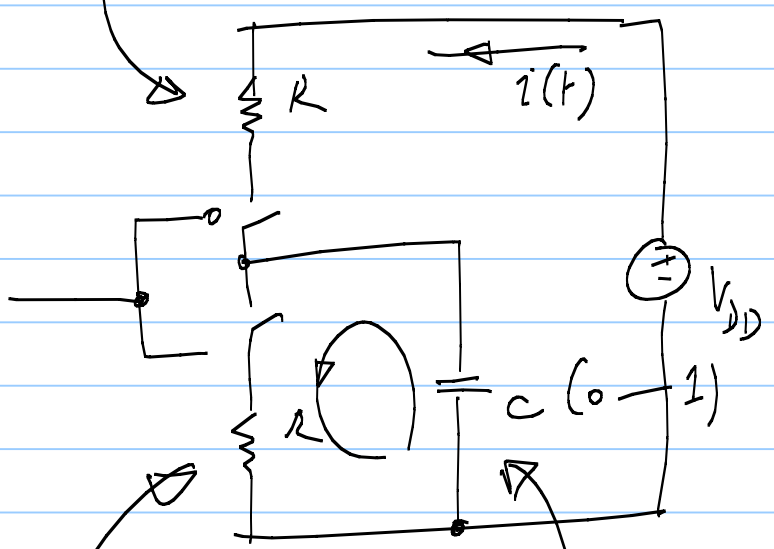
$$(0 \to 1) = \int_0^{(V_{DD})} V_{DD} \cdot C \cdot \frac{dV_{out}}{dt} \cdot dt$$

$$= \int_0^\infty V_{DD} \cdot \frac{V_{DD}}{R} e^{-t/RC} \cdot (0)$$

$$= C \cdot V_{DD}^2$$

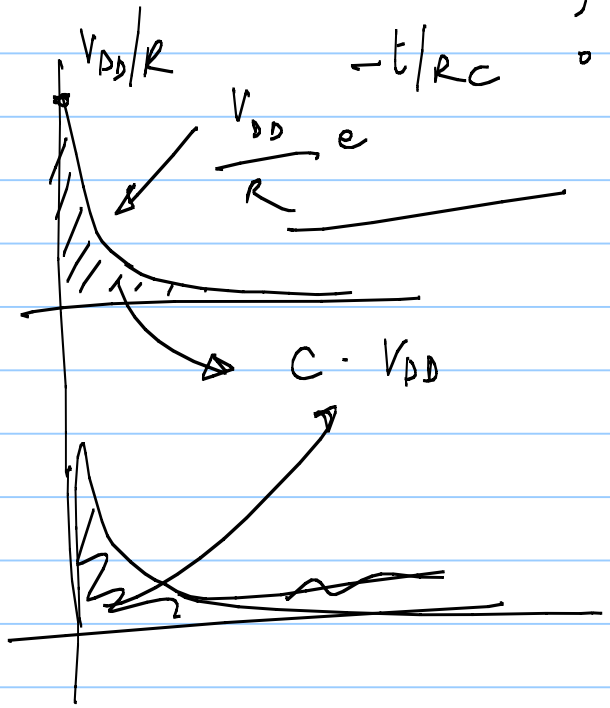
$C \cdot V_{DD}$

$\frac{1}{2} C V_{DD}^2$

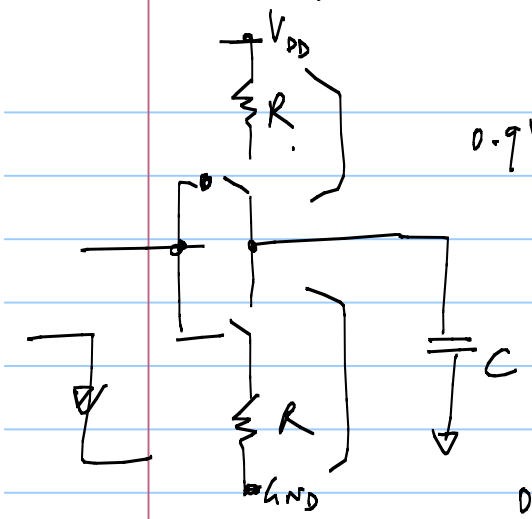


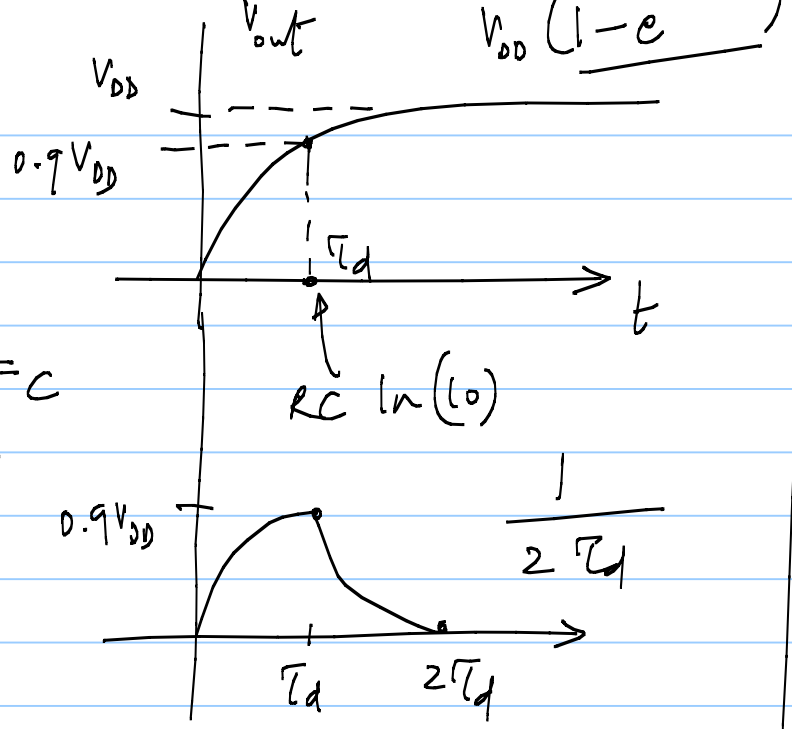
$\frac{1}{2} C V_{DD}^2$ (1→0)

$\frac{1}{2} C V_{DD}^2$



$P = C \cdot V_{DD}^2 \cdot f$



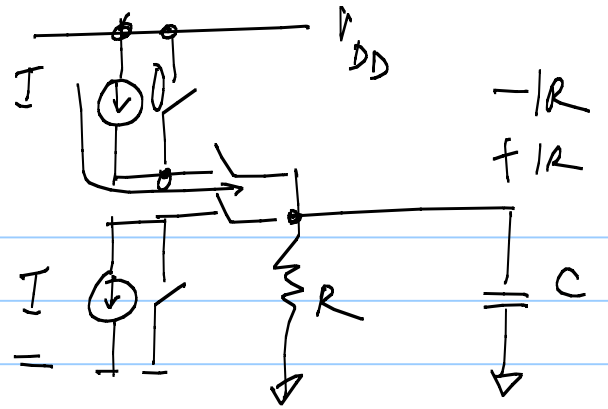


$f_{max} = \frac{1}{2\tau_d}$

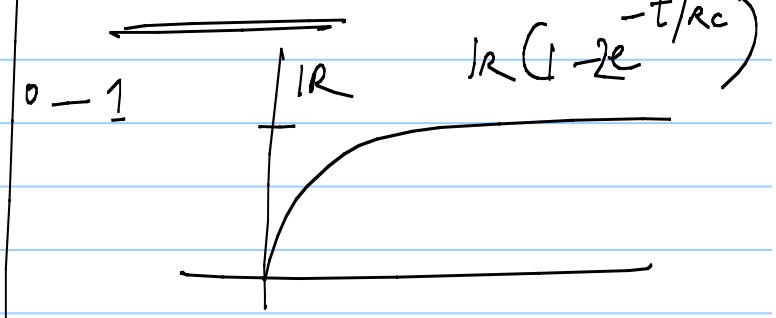
$\frac{1}{2\tau_d}$

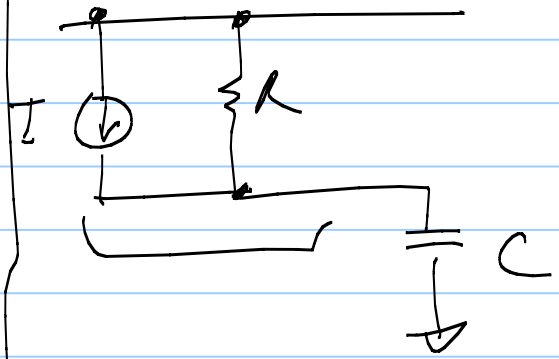
$P = C \cdot V_{DD}^2 \cdot \frac{1}{2\tau_d}$

$P \cdot \tau_d = \frac{C \cdot V_{DD}^2}{2} = \frac{V_{DD}(CV_{DD})}{2}$



$I \cdot V_{DD} \cdot \alpha$





$$V_{out} = (1 - 2e^{-t/RC}) \cdot IR$$

$$1 - 2e^{-t/RC} = 0.9$$

$$e^{-t/RC} = 0.05$$

$$T_d = RC \ln(20)$$

Reduce IR

$$P \cdot T_d = 1 \cdot V_{DD} \cdot \frac{1}{2} \cdot RC \ln(20) = \frac{C \cdot V_{DD} \overbrace{(IR)} \ln(20)}{2}$$

Current mode logic

$$P \cdot T_d = \frac{C \cdot V_{DD}^2}{2}$$ - CMOS $P = \frac{C V_{DD}^2}{2T_d}$

- [Noise margin is reduced [2 logic levels are closer to each other]]
- Static power - Same at LF & HF
- More elaborate circuitry.