VLSI Broadband Communication Circuits

Miscellaneous topics

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Outline

- Optimal equalizers
- LMS adaptation
- Validity of PLL linear model
- PLL lock and capture ranges
- Hogge phase detector offset correction
- Course summary

Intersymbol interference

- Channel response h of length $N \Rightarrow 2^N$ possible values
- Received values spread between $1 - \sum_{k \neq 0} |h_k|$ and $1 + \sum_{k \neq 0} |h_k|$

Maximum likelihood sequence estimation (MLSE)

- Given received values, estimate the most likely sequence of symbols that generated the value
- Minimizes bit error rate
- Exponential complexity with N

Zero forcing linear feedforward equalizer

- ISI can be eliminated using the inverse filter $H^{-1}(z)$
- Noise enhancement at frequencies where $|H(z)| \ll 1$
- Truncated inverse filter in practice
- Minimizes $\sum_{k \neq 0} |f_k|$ ($f = h \otimes g$, g is the equalizer's response) if $\sum_{k \neq 0} |f_k| \leq 1$
- Determine optimal coefficients by truncating $H^{-1}(z)$ to the desired length

Least mean square linear feedforward equalizer

- Minimizes $\sum_{k \neq 0} f_k^2$
- Very little boost at frequencies where $|H(z)| \ll 1$
- Optimal performance in presence of noise—reduced noise enhancement
- Optimal coefficients $\overline{c} = (A^T A)^{-1} A^T \overline{b}$ where columns of A are delayed versions of the input sequence $\overline{b}$ is $[0 \ldots 010 \ldots 0]$

LMS adaptation

$$
\begin{aligned}
y &= \overline{c}^T \overline{g} \\
e &= y - \mathrm{sgn}(y) \\
\overline{c}[k+1] &= \overline{c}[k] - \mu \overline{\nabla}_c E(e^2) \\
\overline{c}[k+1] &= \overline{c}[k] - \mu \overline{\nabla}_c e^2
\end{aligned}
$$

- Steepest descent algorithm to minimize $E(e^2)$
- Use instantaneous value of e^2 instead of expectations (Woodrow)

LMS adaptation

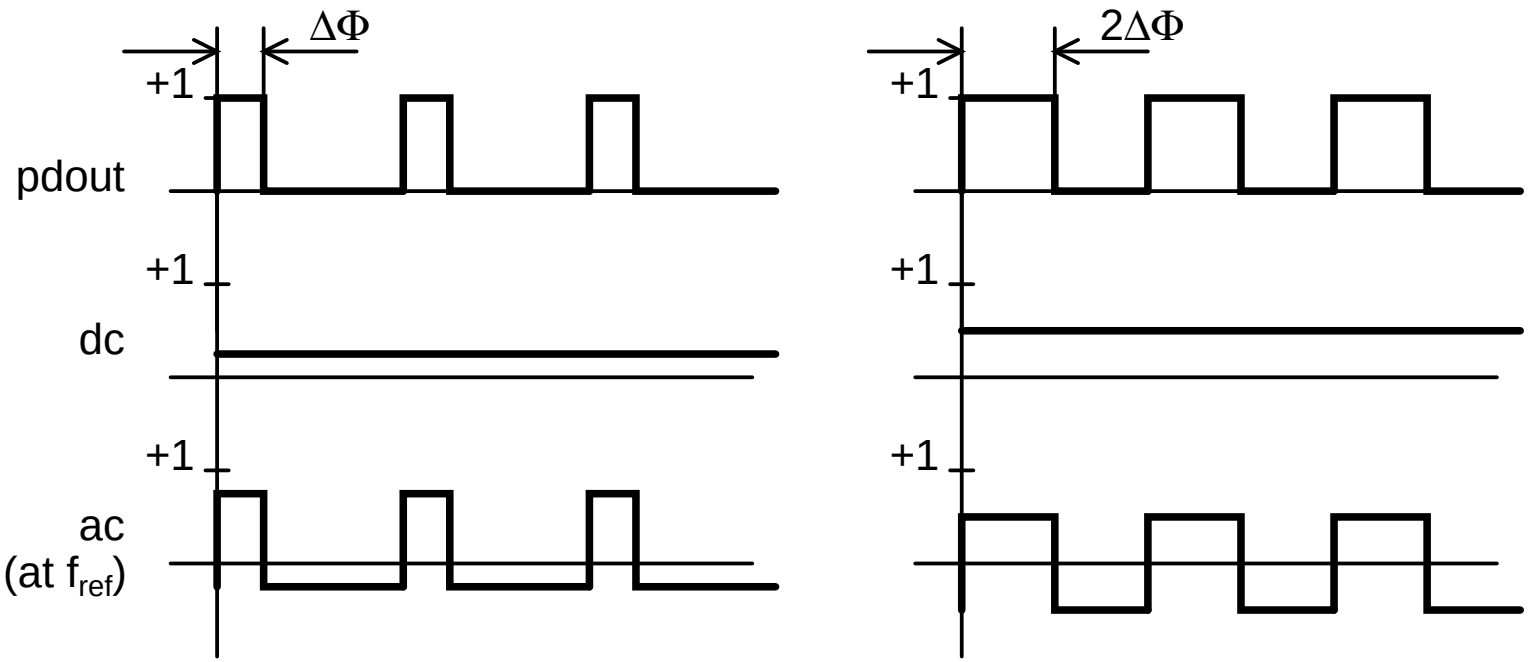
$$
\begin{aligned}
y &= \overline{c}^T \overline{g} \\
e &= y - \mathrm{sgn}(y) \\
\overline{c}[k+1] &= \overline{c}[k] - \mu e[n]\overline{g}[n] && \text{Full LMS} \\
\overline{c}[k+1] &= \overline{c}[k] - \mu e[n]\mathrm{sgn}(\overline{g}[n]) \\
\overline{c}[k+1] &= \overline{c}[k] - \mu \mathrm{sgn}(e[n])\overline{g}[n] \\
\overline{c}[k+1] &= \overline{c}[k] - \mu \mathrm{sgn}(e[n])\mathrm{sgn}(\overline{g}[n]) && \text{Sign-sign LMS}
\end{aligned}
$$

- Steepest descent algorithm
- Gradients are the outputs of FIR delay stages
- Very easy to realize for a DFE—gradients are delayed decisions

Decision feedback equalizer

- ISI subtraction based on past decisions
- Can eliminate post cursor ISI without noise enhancement
- Much lower high frequency boost from the linear feedforward equalizer
- Possibility of error propagation—But works well enough in practice
- Closing feedback loop in one cycle is the biggest challenge

Phase frequency detector nonlinearity



$$\frac{\phi_{div}}{\phi_{ref}-\phi_{div}} = \frac{2\pi K_{pd,I} K_{vco}}{Ns^2}\left(1 + sK_{pd}/K_{pd,I}\right) \qquad (1)$$

- When $\Delta\Phi$ doubles, average value doubles, ac part doesn't $\Rightarrow$ nonlinear
- If $\left|\frac{\phi_{div}}{\phi_{ref}-\phi_{div}}\right| \ll 1$ at $2\pi f_{ref}$, ac part is removed; approximately linear
- Linear analysis of the loop valid under this condition:

PLL lock and capture ranges

- Lock range: Range over which PLL can lock, given the right initial conditions—limited by the range of some component in the loop
  - Quasi-static operation
  - Start with a locked PLL
  - Sweep the input frequency *very slowly* until the PLL loses lock.
- Capture range: Largest frequency step that can be applied to a locked PLL such that it locks to the new frequency
  - Dynamic operation
  - Start with a locked PLL
  - Step the input frequency and see if the PLL acquires lock within a certain interval

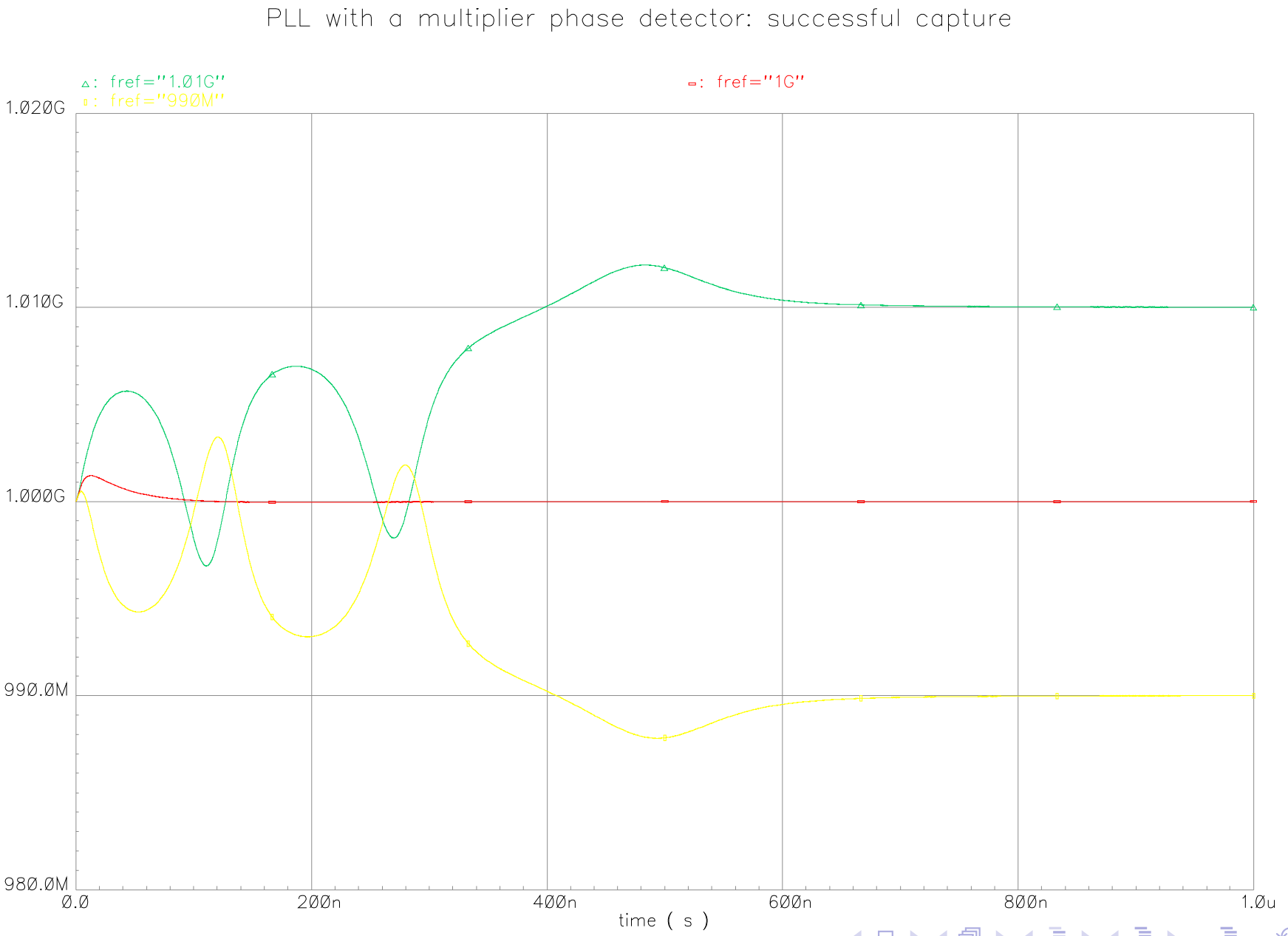
PLL lock range

- Type I PLL
  - May be limited by phase detector range
  - Build a type II PLL
- Type II PLL
  - Steady state phase error independent of frequency
  - Not limited by the phase detector
  - Limited by VCO range; loop fi lter output voltage range;
  - Increase these ranges to get rid of the limitation

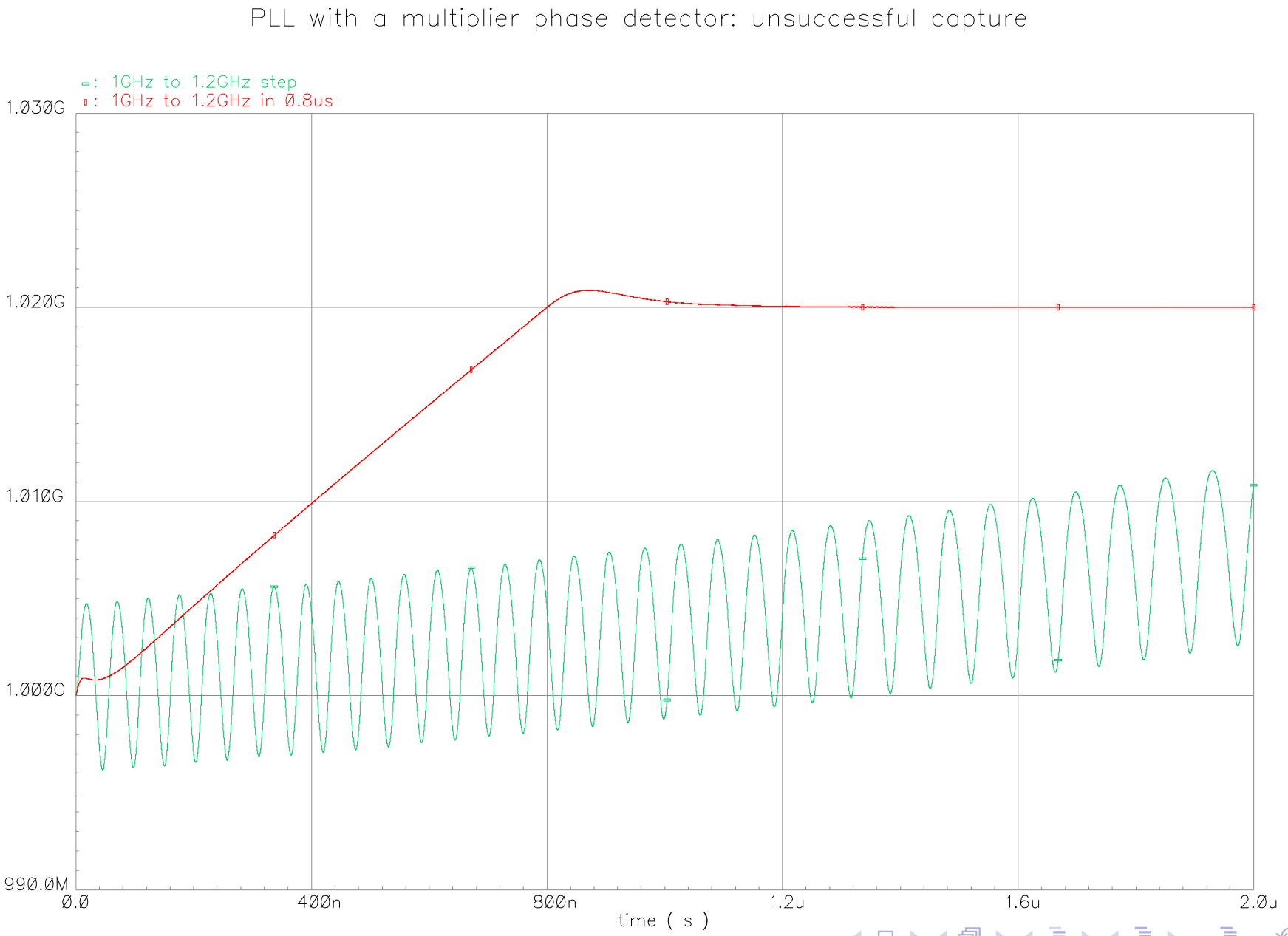
PLL capture range-Type II PLL

- Phase frequency detector
  - Non zero average output voltage in case of a frequency difference
  - This drives the VCO in the right direction
  - Capture range=lock range; But may take a very long time for a large frequency step
- Multiplier, XOR gate, Hogge phase detector, Alexander phase detector
  - Zero average output voltage in case of a frequency difference
  - Output contains difference frequency component which can drive the VCO in the right direction
  - If difference frequency component is severely attenuated by the loop, it may fail to capture
  - In practice, a frequency detector is used as an acquisition aid

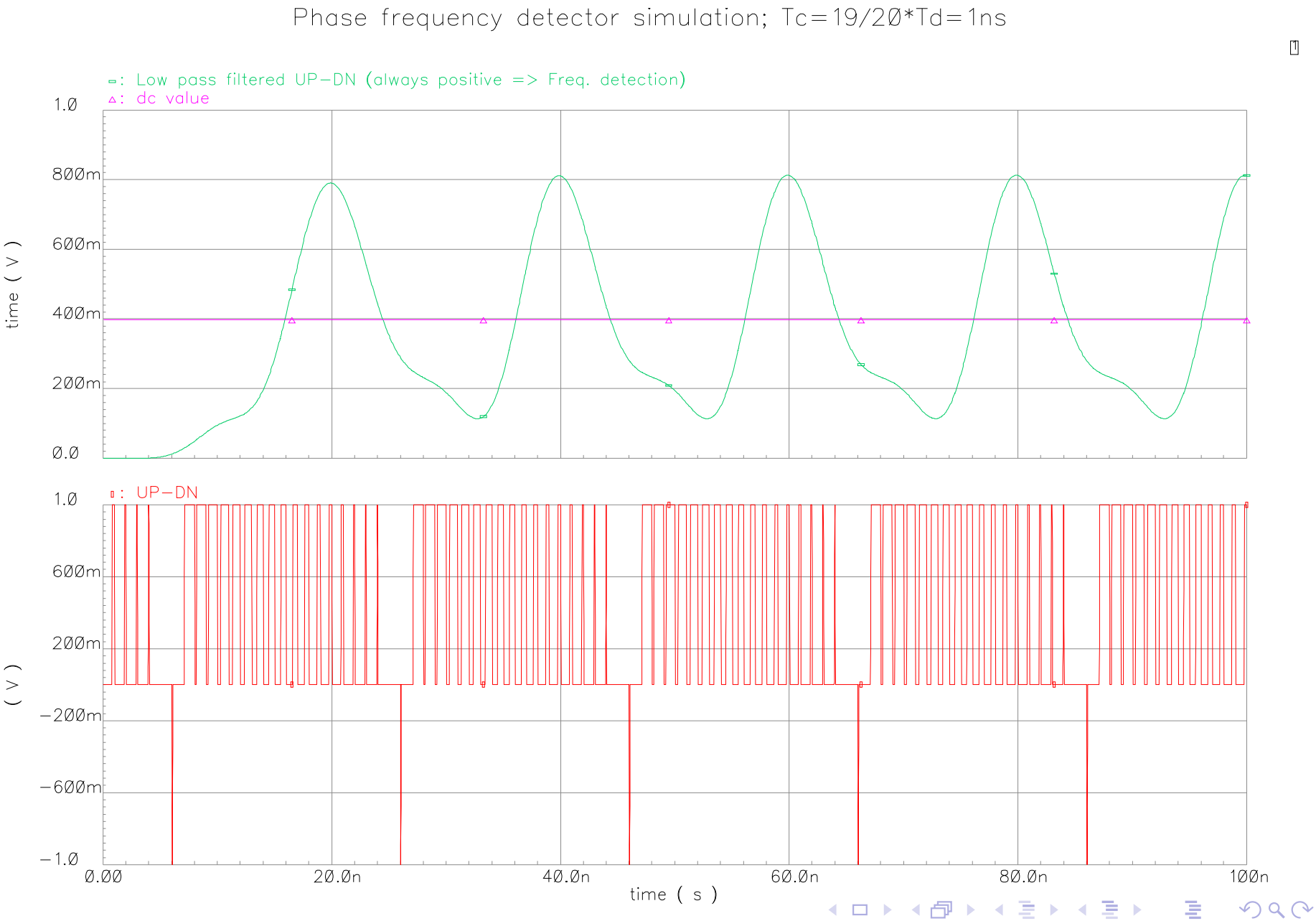
Successful capture



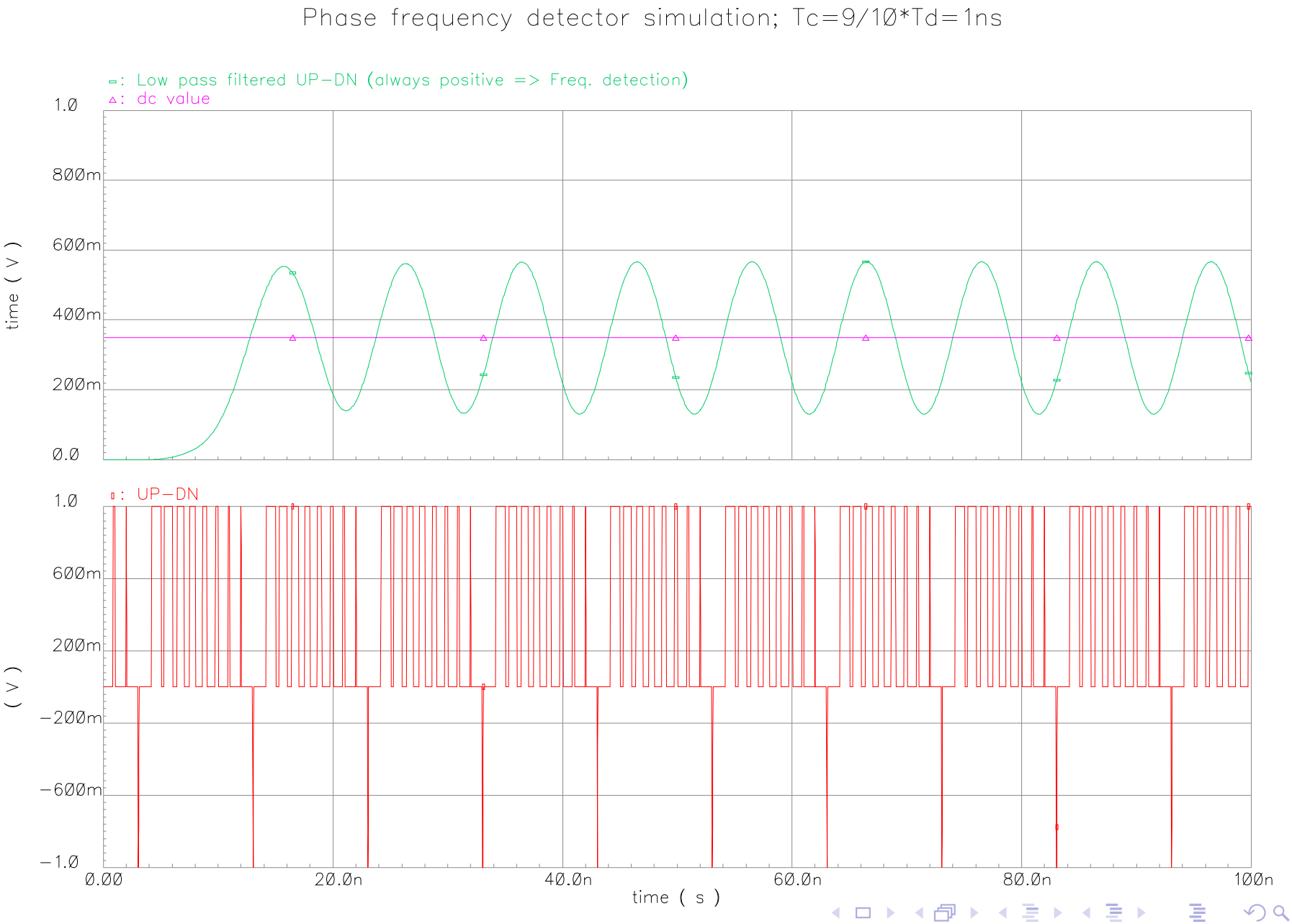
Unsuccessful capture-but stays locked over this range



Phase frequency detector: $f_c = 19/20 f_d$

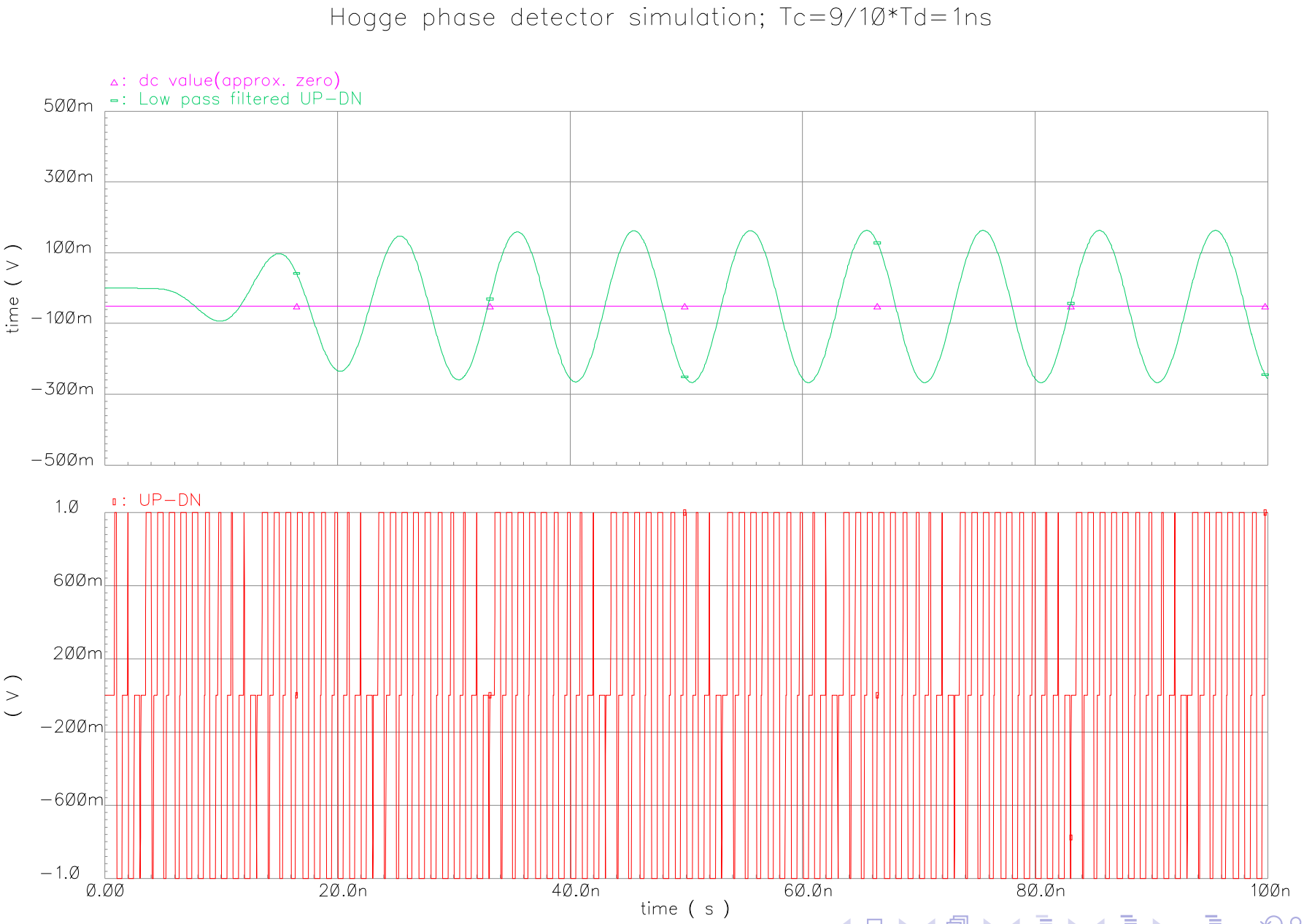


Phase frequency detector: $f_c = 9/10 f_d$

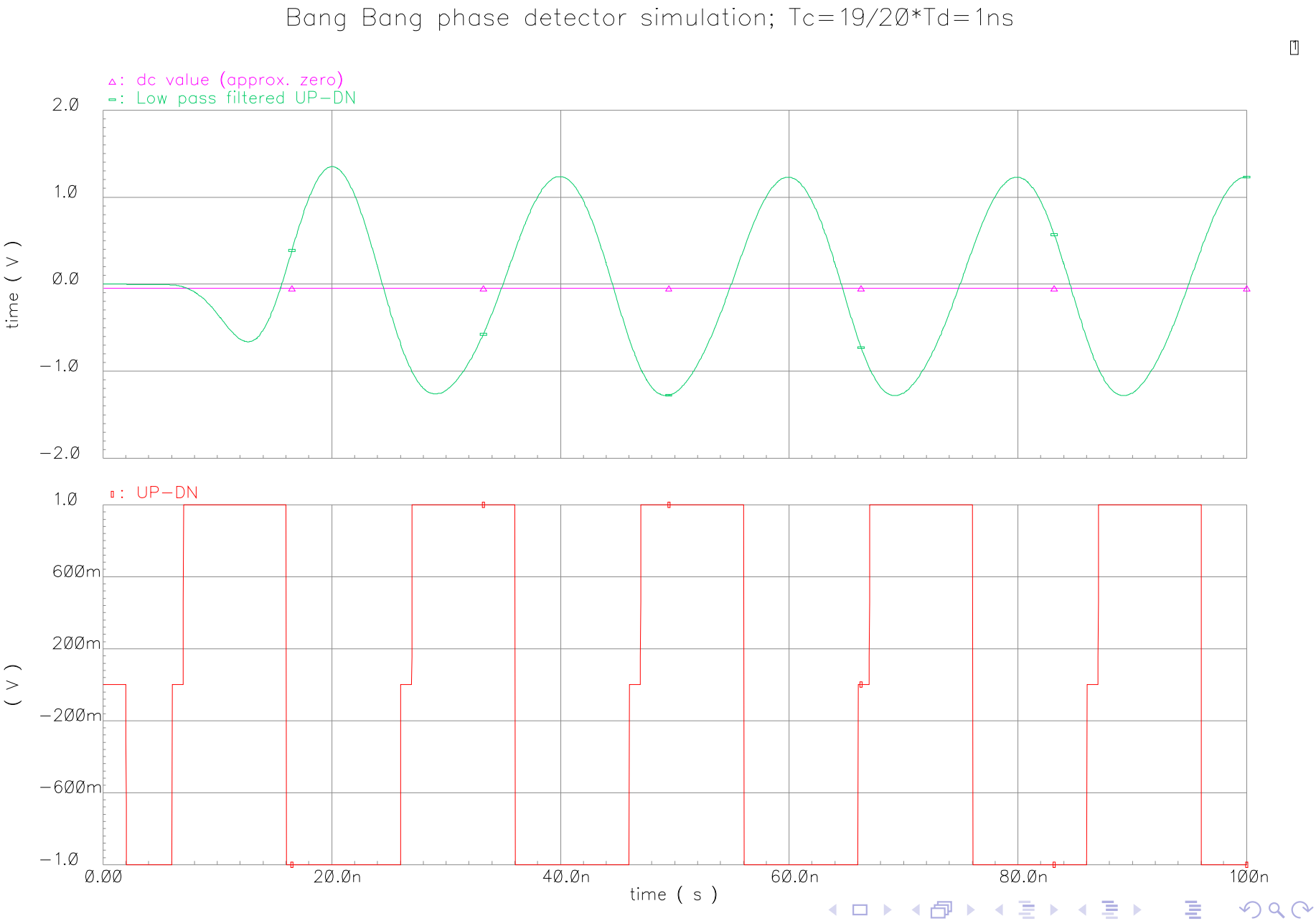


Hogge phase detector: $f_c = 19/20 f_d$

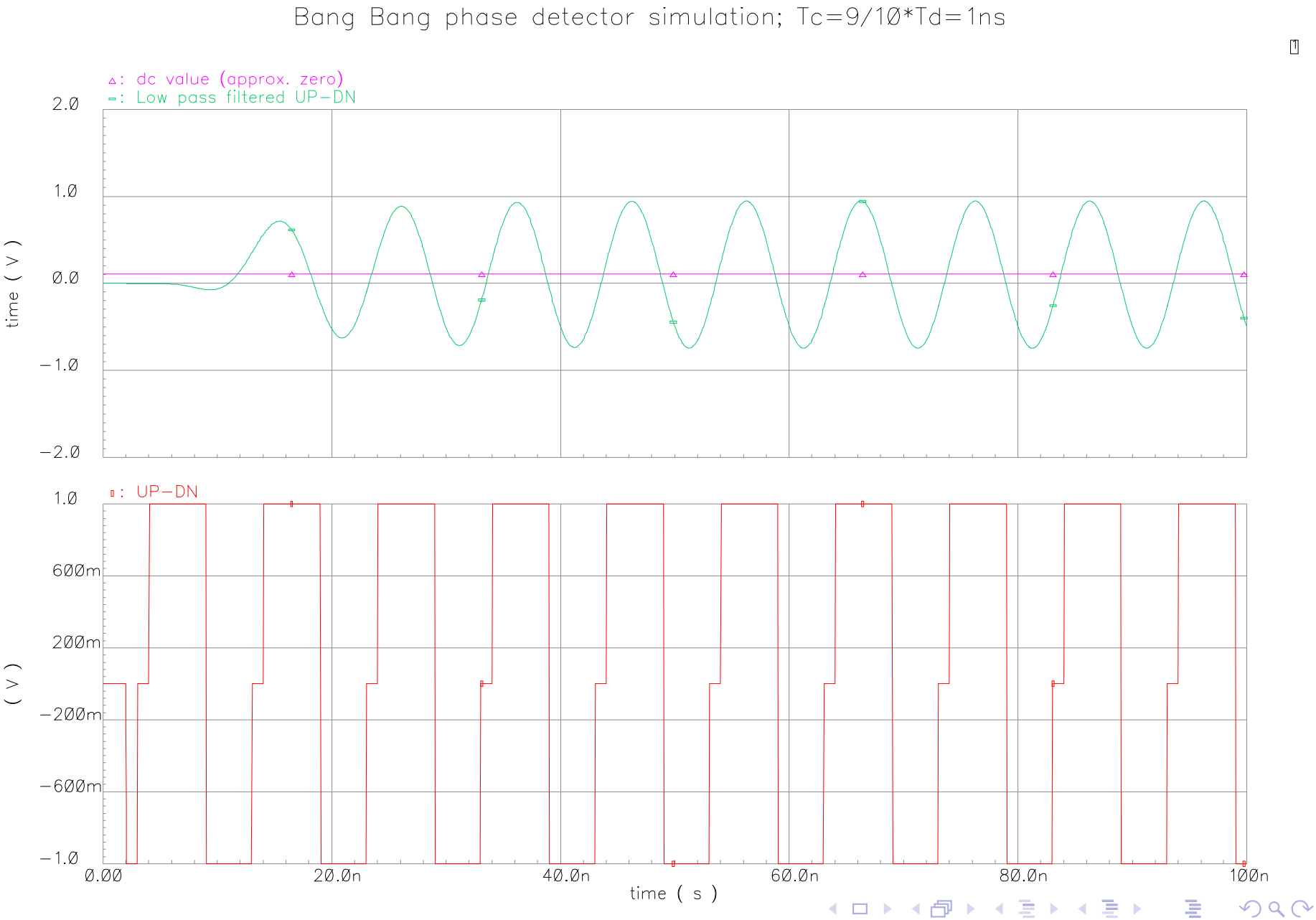
Hogge phase detector: $f_c = 9/10 f_d$



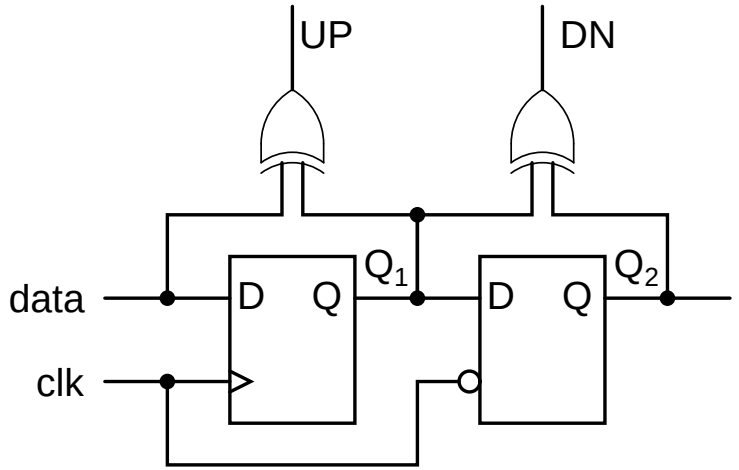
Bang bang phase detector: $f_c = 19/20 f_d$

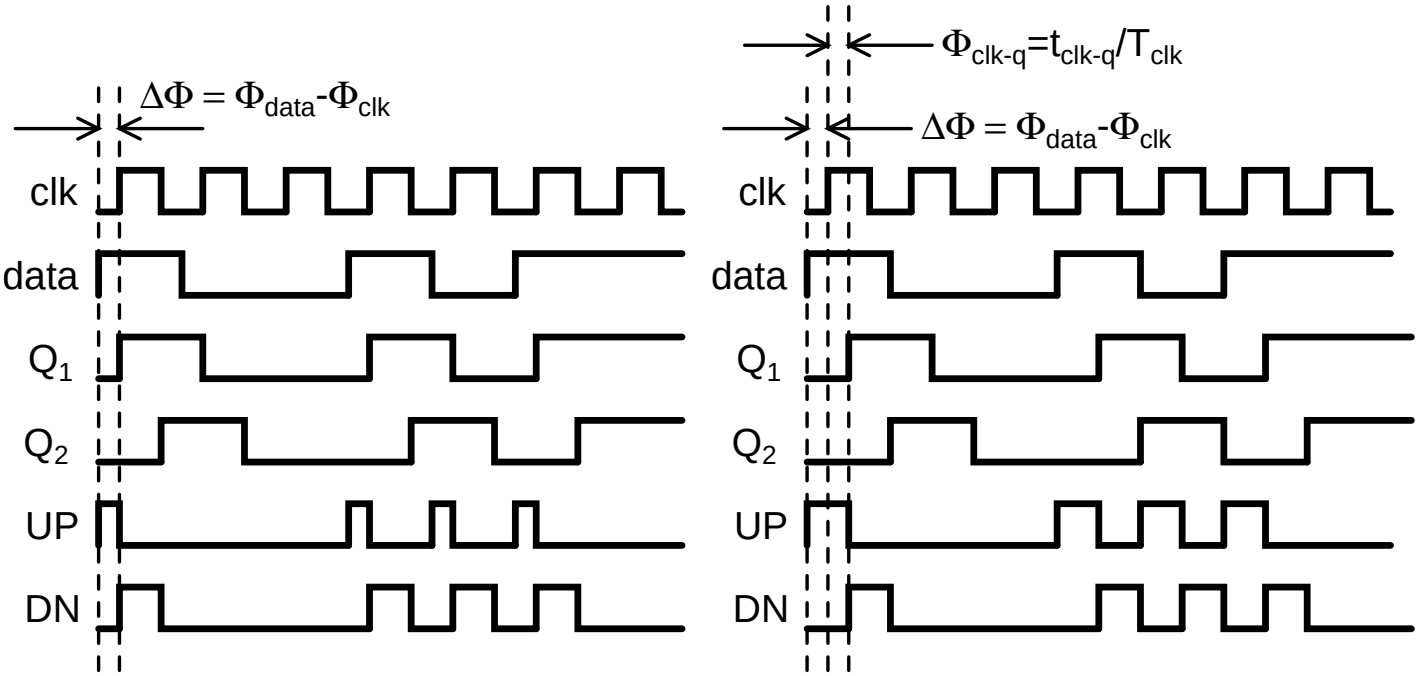


Bang bang phase detector: $f_c = 9/10 f_d$



Hogge phase detector: effects of flip flop delay





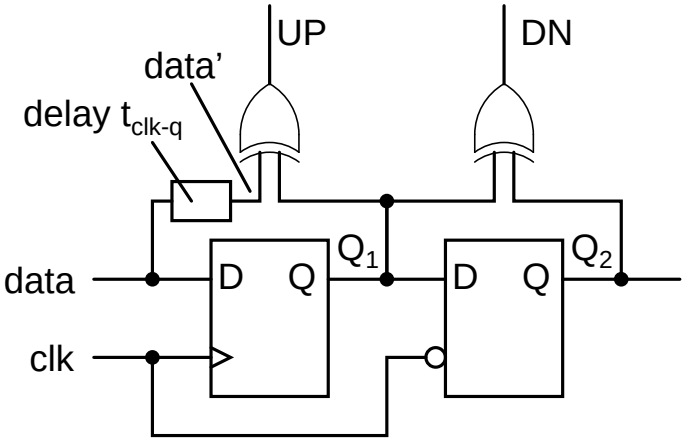
using ideal flip flops

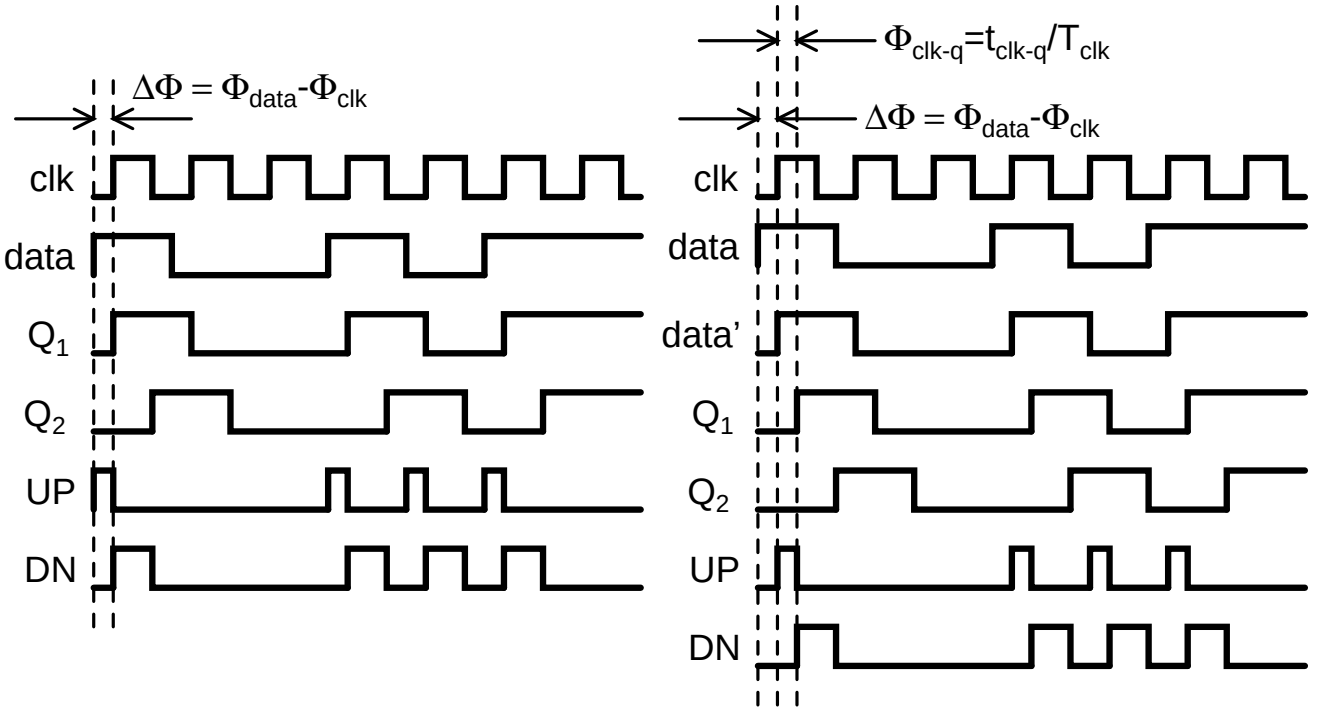
using flip flops with delay tclk-q

Hogge phase detector: effects of flip flop delay

- Clock to Q delay widens UP pulse by t_{clk-q}
- UP pulse width is unaltered
- Phase offset of t_{clk-q}/T_{clk} to obtain zero average of $UP - DN$

Hogge phase detector: offset correction





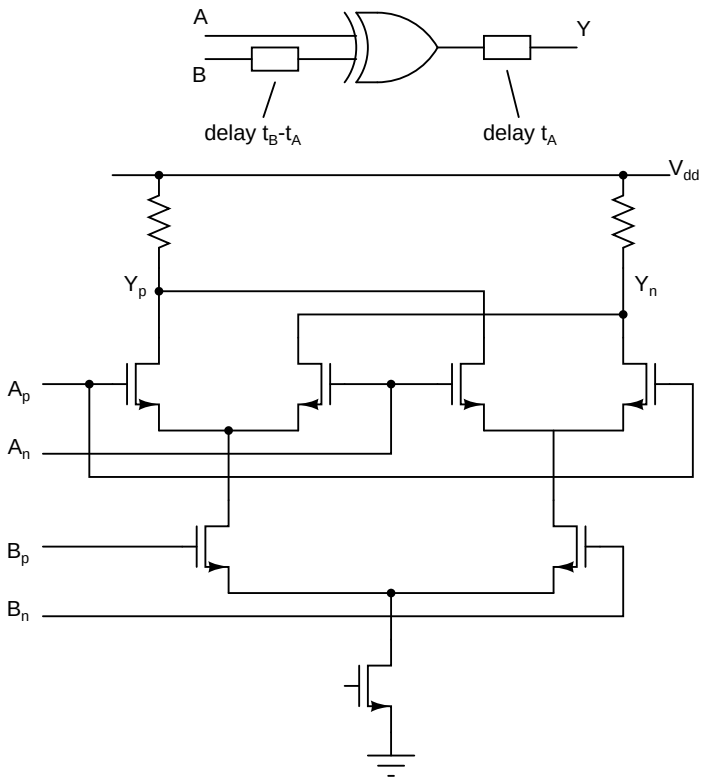
using ideal flip flops

using delay compensation

Hogge phase detector: offset correction

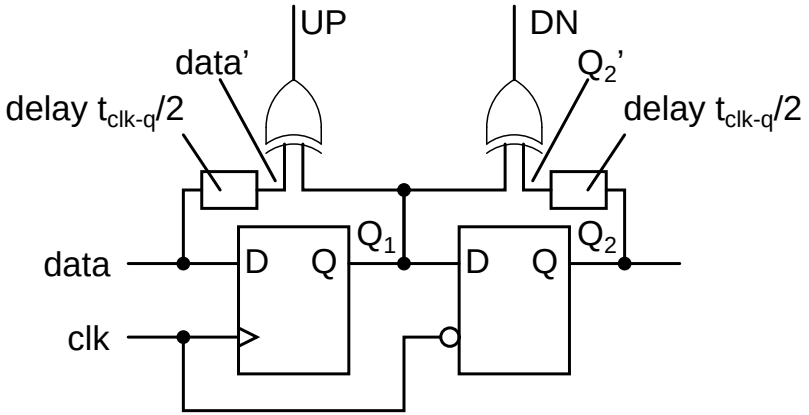
- Delay the input by t_{clk-q} before feeding to the XOR gate
- Reduces *UP* pulse width t_{clk-q} and eliminates the offset

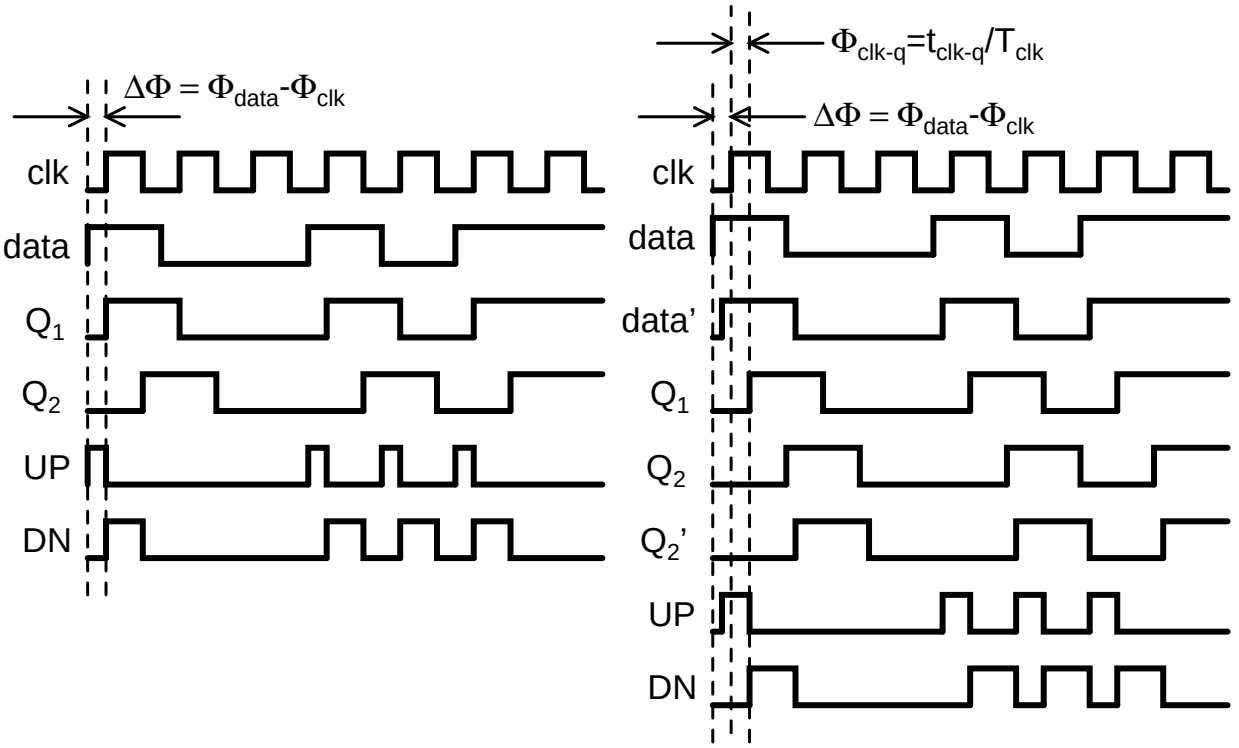
CML XOR gate



- Delay from *B* more than delay from *A*
- Use this asymmetry to correct Hogge phase detector offset

Hogge phase detector: offset correction





using ideal flip flops

asymmetric flip flops with appropriate delays

Hogge phase detector: offset correction

- Reduce *UP* pulse width by $t_{clk-q}/2$ and increase *DN* pulse width by $t_{clk-q}/2$ to correct the offset
- Difference is XOR input delays must be $t_{clk-q}/2$
- In practice, cancellation won't be exact

EE685: VLSI Broadband Communication Circuits

- Serial communication link
  - Equalizers to enhance eye opening
  - Clock and data recovery
- Topics covered
  - Generate discrete time channel model from continuous-time channel response
  - Determine optimal equalizer coeffi cients
  - Design high speed transmit FIR feedforward or receive decision feedback equalizers
  - Design clock and data recovery circuits, given a VCO
  - Eye diagrams
- Topics left out
  - Transmission lines—channels
  - Fractionally spaced equalizers
  - Oscillator design
  - Detailed treatment of jitter

References

- John G. Proakis, *Digital Communications*, McGraw Hill, 2000.
- B. Razavi (editor), *Monolithic Phase Locked Loops and Clock Recovery Circuits-Theory and Design*, IEEE Press, 1996.
- B. Razavi (editor), *Phase-Locking in High-Performance Systems: From Devices to Architectures*, Wiley-IEEE Press, 2003.
- Rick Walker's papers at http://www.omnisterra.com/walker/pubs.html