EE685: VLSI Broadband Communication Circuits; HW6

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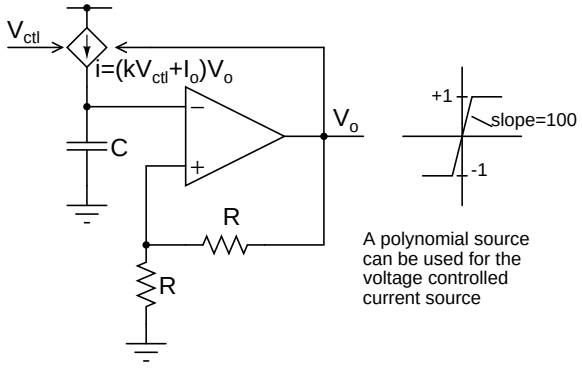

Figure 1: Voltage controlled oscillator

VCO macromodel: Use the schmitt trigger oscillator in Fig. 1 to model a voltage controlled oscillator. For the opamp, use a voltage controlled voltage source with a gain of 100 and saturation voltages of $\pm 1\,\mathrm{V}$[1]. Adjust k, I_o, C to get an oscillation frequency of 900 MHz for $V_{ctl} = V_{dd}/2$ and $K_{vco} = 250\,\mathrm{MHz/V}$. To drive flip flops and other circuits differentially, scale the opamp output appropriately and add the desired common mode voltage.

Clock and data recovery circuit with a linear phase detector: Design a CDR for 1 Gb/s data using the blocks designed in the previous assignment. The rising edge of the recovered clock should be in the middle of data. The CDR loop should have a bandwidth of 10 MHz with 50% input transition density. Use ideal voltage sources to level shift the phase detector outputs to drive the charge pump if necessary.

Simulate the CDR with a 500 mVppd PRBS7 input with a 100 ps rise/fall times and the VCO control voltage initialized to $V_{dd}/2$.

Plot the VCO control voltage versus time and show that it settles to the correct value.

Plot the eye diagrams of the input data and the recovered clock (on top of each other) after settling is achieved. What is the phase offset of the recovered clock from the data transitions? What is the jitter in the recovered clock?

Clock and data recovery circuit with a binary phase detector: Substitute the linear phase detector in the circuit above with a binary phase detector.

Simulate the CDR with a 500 mVppd PRBS7 input with a 100 ps rise/fall times and the VCO control voltage initialized to $V_{dd}/2$.

Plot the VCO control voltage versus time and show that it settles to the correct value.

Plot the eye diagrams of the input data and the recovered clock (on top of each other) after settling is achieved. What is the phase offset of the recovered clock from the data transitions? What is the jitter in the recovered clock?

Compare the settling time, phase offset and jitter of the CDR with the binary phase detector and the linear phase detector.

Time taken to do the assignment: How many hours did you spend on this assignment? Of those, how many were spent in writing up the report?

[1] For analyzing the oscillator, use infinite slope.