EE685: VLSI Broadband Communication Circuits; HW5

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Linear phase detector: Design a linear (Hogge) phase detector for 1 Gb/s data using flip flops designed in the first assignment and CML gates. Simulate the transfer curve of average output voltage (Average value of the difference between UP and DN waveforms from the phase detector) versus input phase difference over the input range of the phase detector. Use closely spaced points around $\Delta\phi = 0$. Use alternating binary data input for the simulation.

Bang Bang phase detector: Design a bang-bang (Alexander) phase detector for 1 Gb/s data using flip flops designed in the first assignment and CML gates. Simulate the transfer curve of average output voltage (Average value of the difference between UP and DN waveforms from the phase detector) versus input phase difference over the input range of the phase detector. Use closely spaced points around $\Delta\phi = 0$. Use alternating binary data input for the simulation.

Charge pump: Design a charge pump using nMOS and pMOS differential pairs and 10 μA cascode current sources. It should be able to operate over an output voltage range of $V_{DD}/2 \pm 0.5$ V. Design the circuit for biasing the cascode current sources from a single 10 μA reference. Use identical common mode voltages for UP and DN signals.

Terminate the charge pump output with a $V_{DD}/2$ voltage source and drive it with alternating UP and DN signals with 0.5 ns width with a 1 ns period. Plot the output current waveform. Determine the average output current of the charge pump over 100 cycles. This gives you the dynamic offset current of the charge pump. What phase offset does it correspond to? Repeat the offset simulations for termination voltages of $V_{DD}/2 \pm 0.5$ V

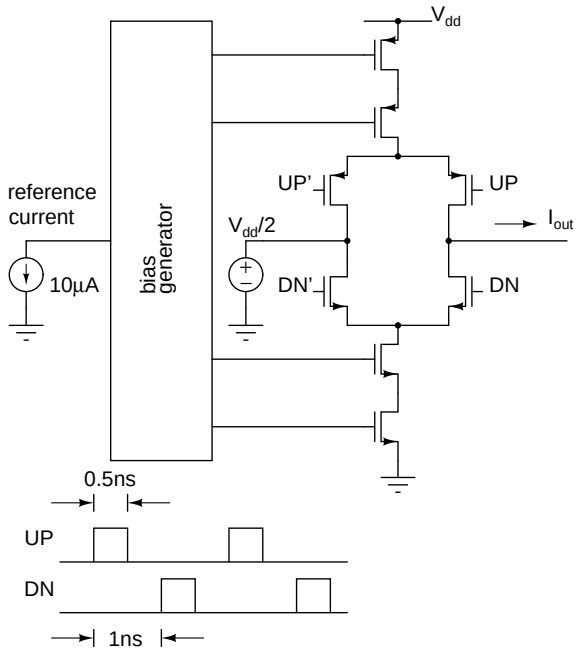

Figure 1: Charge pump

VCO macromodel: Use the schmitt trigger oscillator in Fig. 2 to model a voltage controlled oscillator. For the opamp, use a voltage controlled voltage source with a gain of 100 and saturation voltages of ± 1 V. Adjust RC and the feedback multiplication circuitry to get an oscillation frequency of 900 MHz for $V_{ctl} = V_{dd}/2$ and $K_{vco} = 250$ MHz/V. To drive flip flops and other circuits differentially, scale the

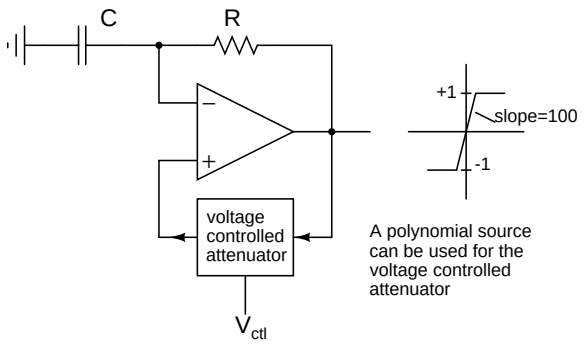

Figure 2: Voltage controlled oscillator

opamp output appropriately and add the desired common mode voltage.

Time taken to do the assignment: How many hours did you spend on this assignment? Of those, how many were spent in writing up the report?