Pipelined multi step A/D converters

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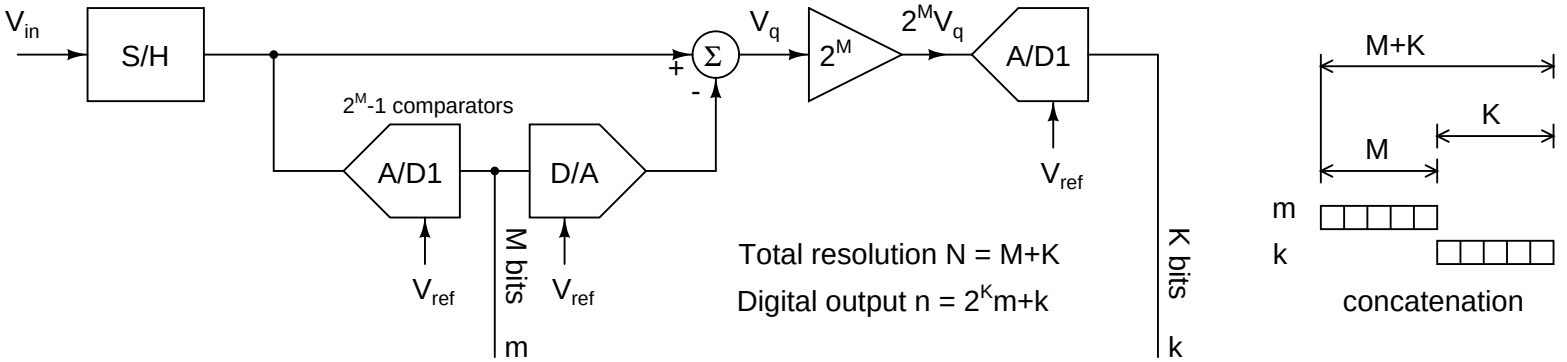
Motivation for multi step A/D conversion

- Flash converters:
  - Area and power consumption increase exponentially with number of bits N
  - Impractical beyond 7-8 bits.
- Multi step conversion-Coarse conversion followed by fine conversion
  - Multi-step converters
  - Subranging converters
- Multi step conversion takes more time
  - Pipelining to increase sampling rate

Two step A/D converter-basic operation

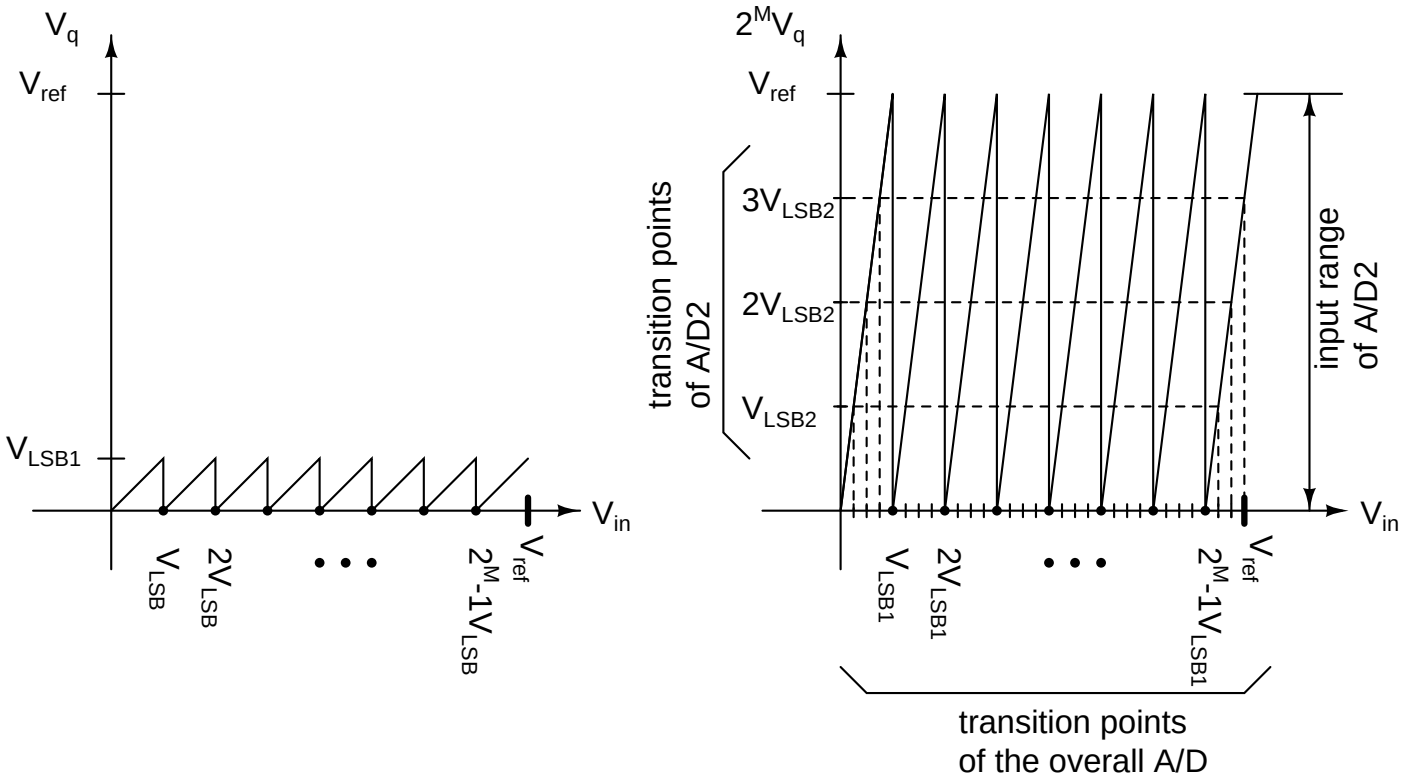


- Second A/D quantizes the quantization error of first A/D
- Concatenate the bits from the two A/D converters to form the final output

Two step A/D converter-basic operation

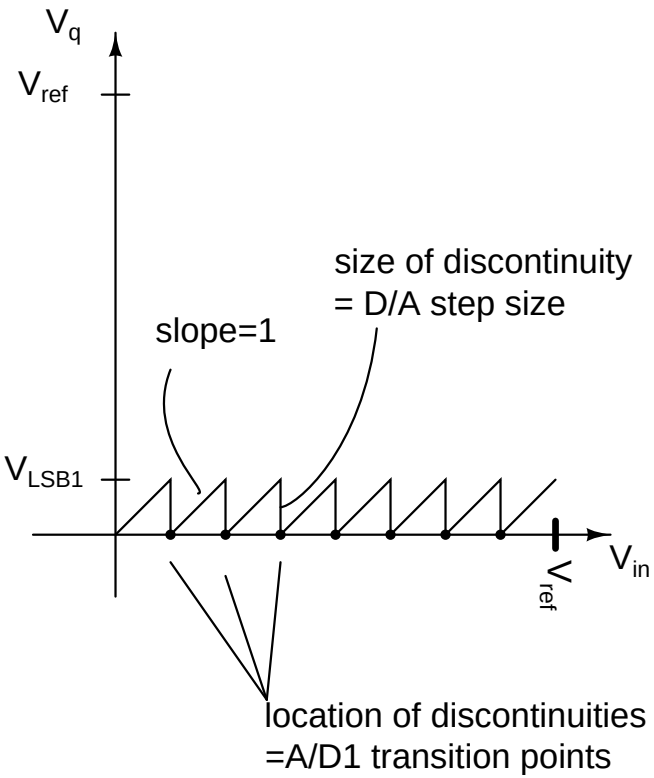
- A/D1, DAC, and A/D2 have the same range V_{ref}
- Second A/D quantizes the quantization error of first A/D
  - Use a DAC and subtractor to determine V_q
  - Amplify V_q to full range of the second A/D
- Final output n from m, k
  - A/D1 output is m (DAC output is $m/2^M V_{ref}$)
  - A/D2 input is at k^{th} transition ($k/2^K V_{ref}$)
  - $V_{in} = k/2^K V_{ref} \times 1/2^M + m/2^M V_{ref}$
  - $V_{in} = (2^K m + k)/2^{M+K} V_{ref}$
- Resolution $N = M + K$, output $\Rightarrow n = 2^K m + k \Rightarrow$ Concatenate the bits from the two A/D converters to form the final output

Two step A/D converter: Example with $M = 3, K = 2$



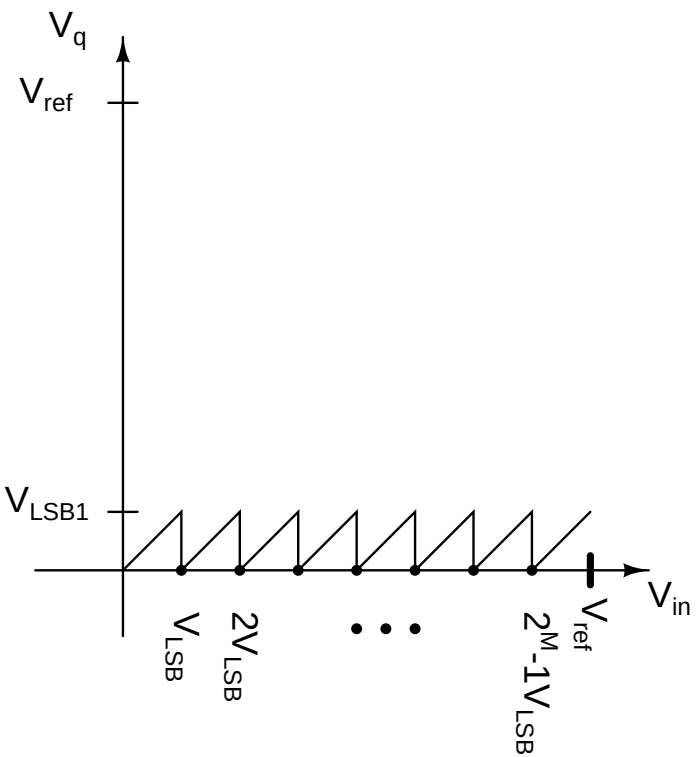
- Second A/D quantizes the quantization error of first A/D
- Transitions of second A/D lie between transitions of the first, creating finely spaced transition points for the overall A/D.

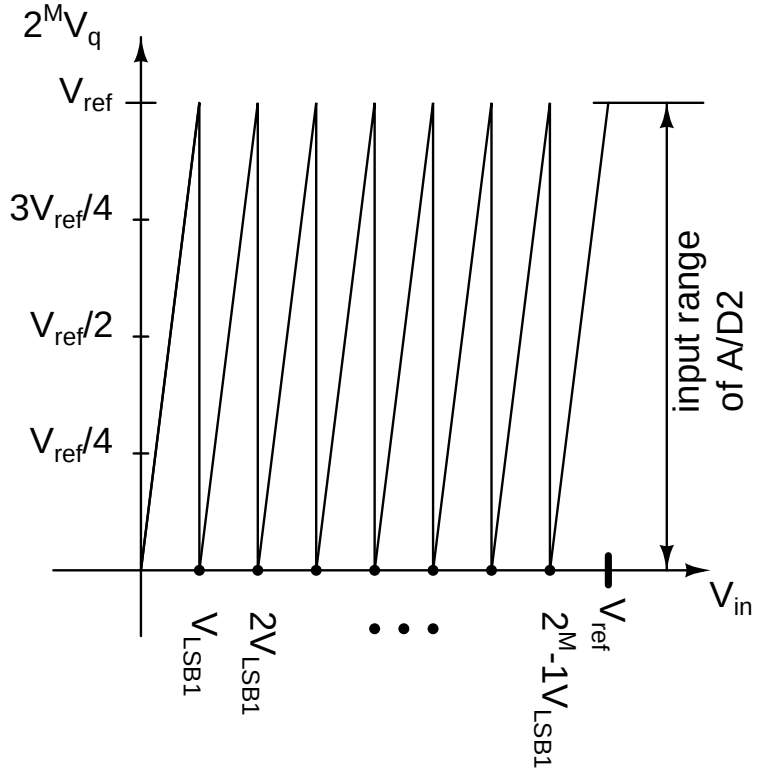
Quantization error V_q



- V_q vs. V_{in}: Discontinuous transfer curve
  - Location of discontinuities: Transition points of A/D1
  - Size of discontinuities: Step size of D/A
  - Slope: unity

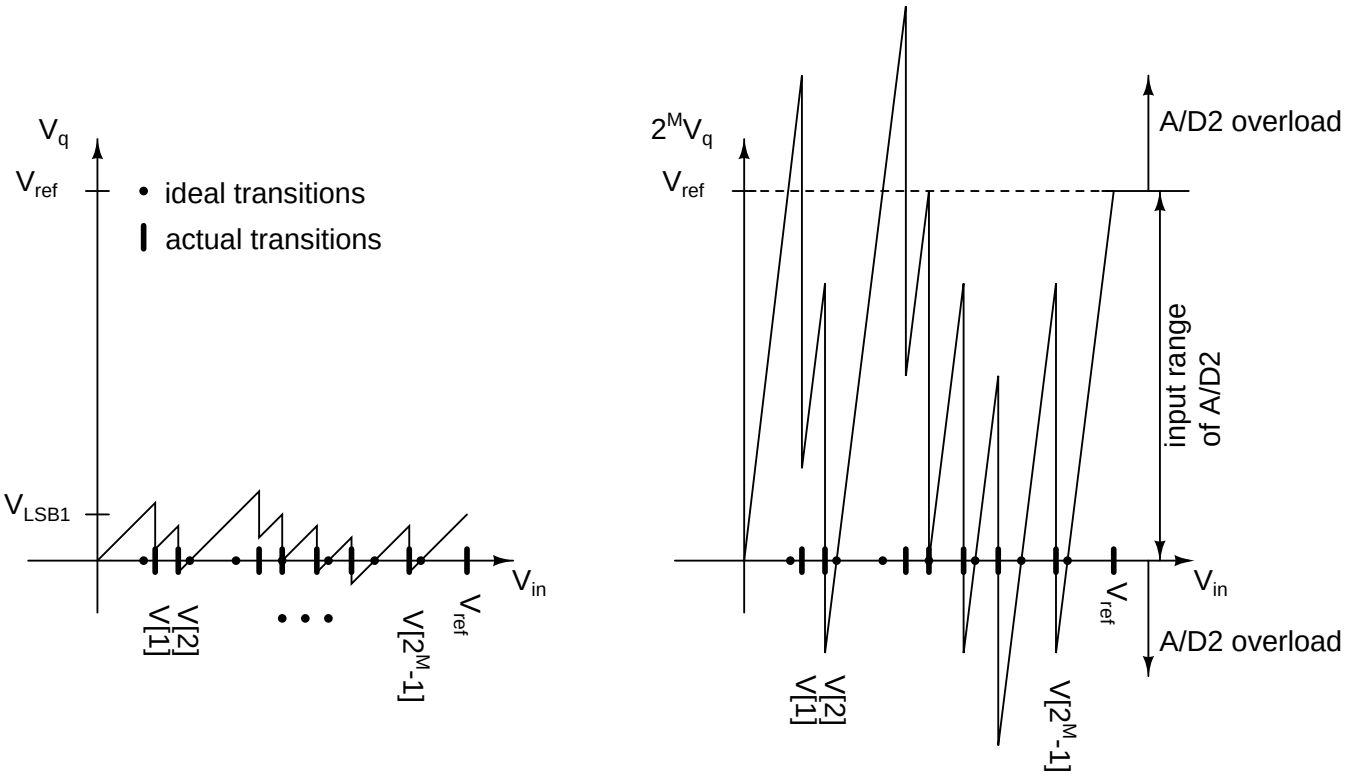
Two step A/D converter—ideal A/D1





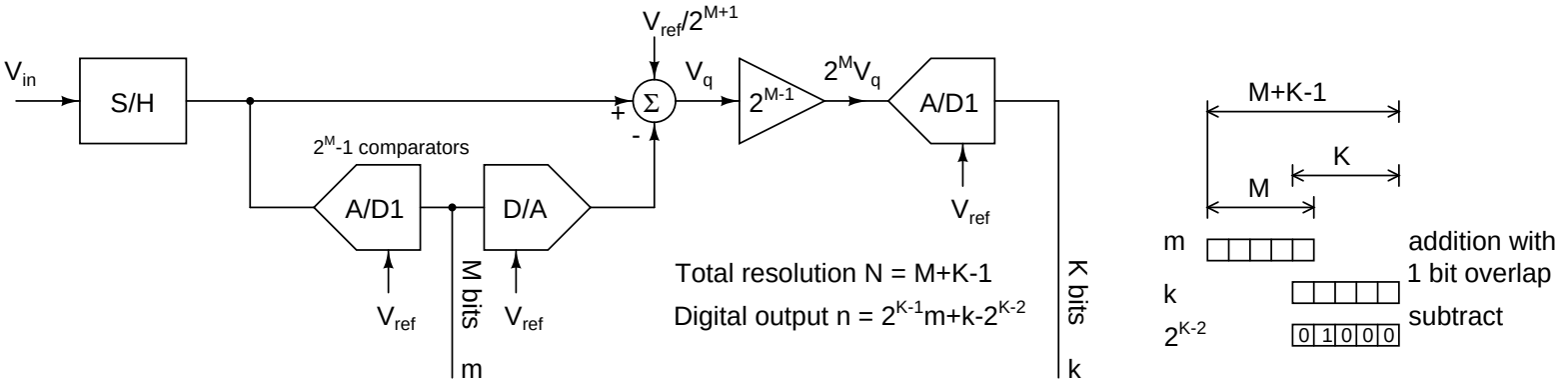
- A/D1 transitions exactly at integer multiples of $V_{ref}/2^M$
- Quantization error V_q limited to $(0, V_{ref}/2^M)$
- $2^M V_q$ exactly fits the range of A/D2

Two step A/D converter—M bit accurate A/D1



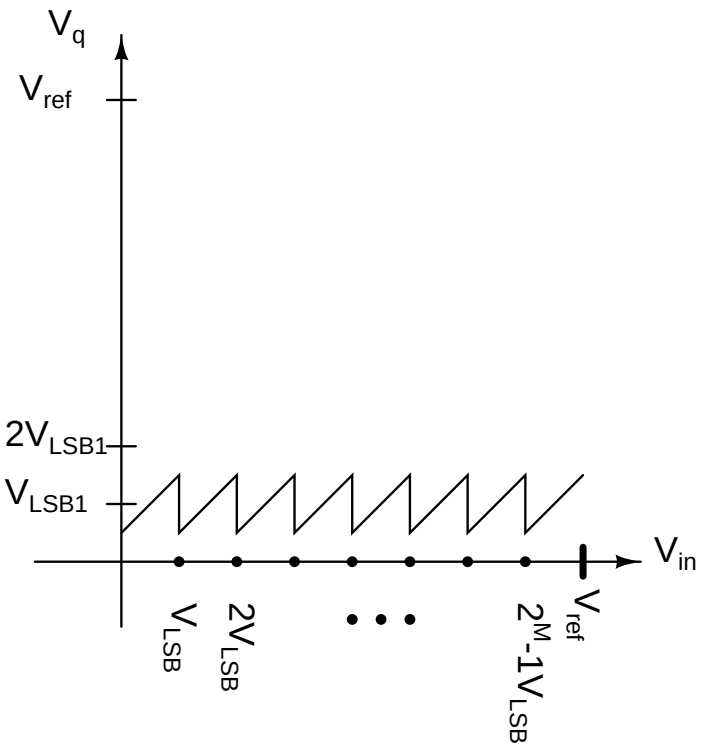
- A/D1 transitions in error by up to $V_{ref}/2^{M+1}$
- Quantization error V_q limited to $(-V_{ref}/2^{M+1}, 3V_{ref}/2^{M+1})$—a range of $V_{ref}/2^{M-1}$
- $2^M V_q$ overloads A/D2

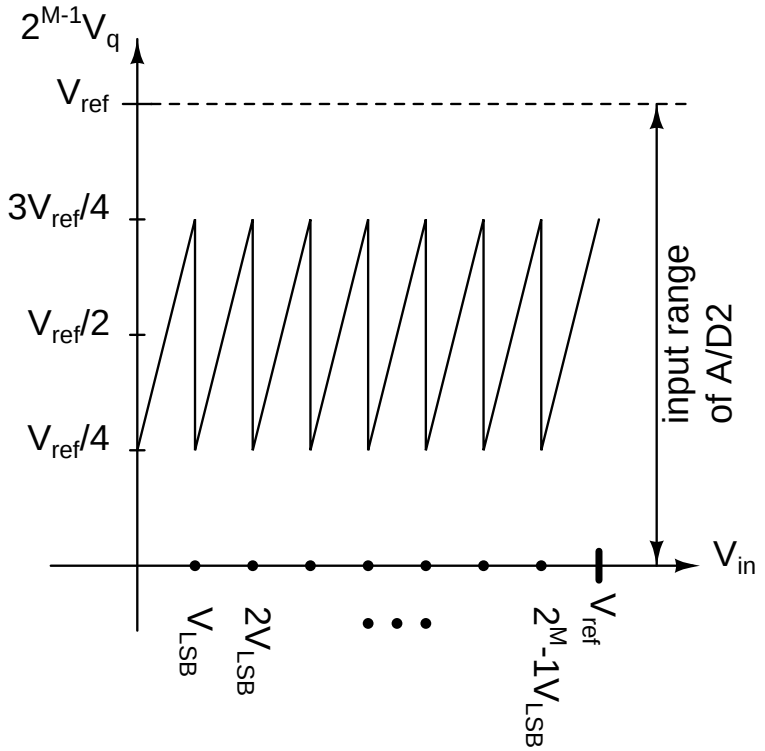
Two step A/D with digitial error correction (I)



- Reduce interstage gain to 2^{M-1}
- Add $V_{ref}/2^{M+1}$ (0.5 LSB1) offset to DAC output to keep V_q positive
- Subtract 2^{K-2} from digital output to compensate for the added offset
- Overall accuracy is $N = M + K - 1$ bits; A/D1 contributes $M - 1$ bits, A/D2 contributes K bits; 1 bit redundancy
- Output $n = 2^{K-1}m + k - 2^{K-2}$

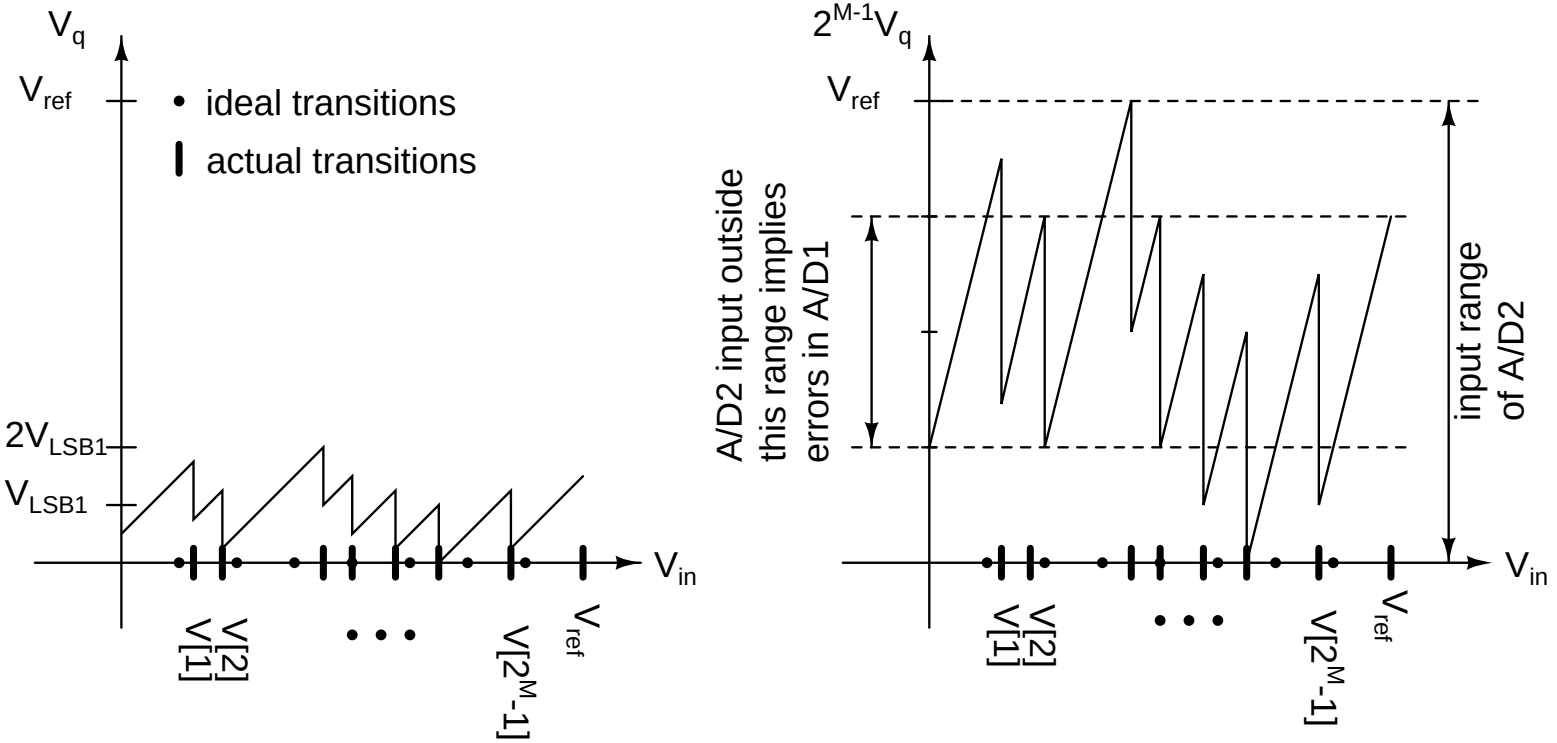
Two step A/D with digitial error correction (I)—Ideal A/D1





- $2^{M-1}V_q$ varies from $V_{ref}/4$ to $3V_{ref}/4$
- $2^{M-1}V_q$ outside this range implies errors in A/D1

Two step A/D with digital error correction (I)—M bit accurate A/D1

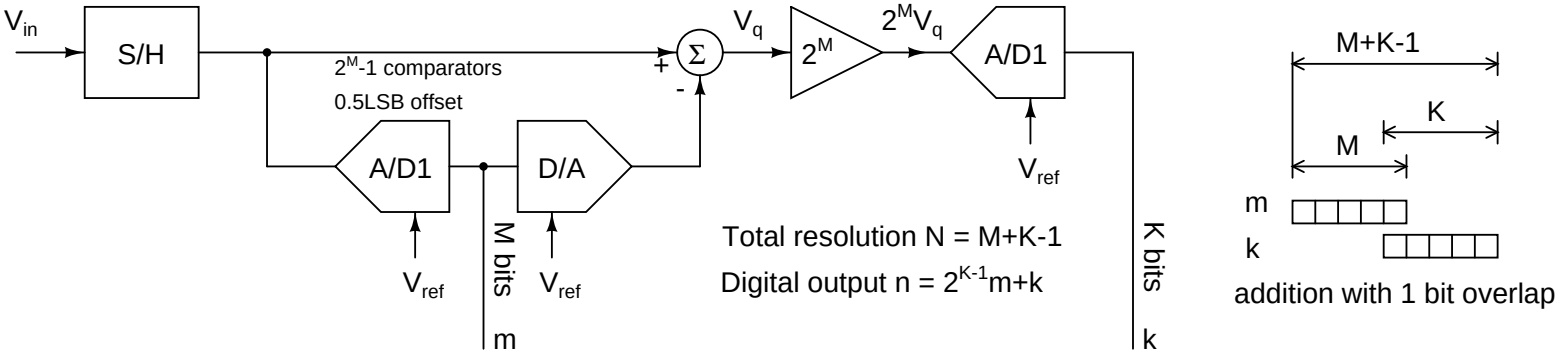


- $2^{M-1}V_q$ varies from 0 to V_{ref}
- A/D2 is not overloaded for up to 0.5 LSB errors in A/D1

Two step A/D with digitial error correction (I)—M bit accurate A/D1

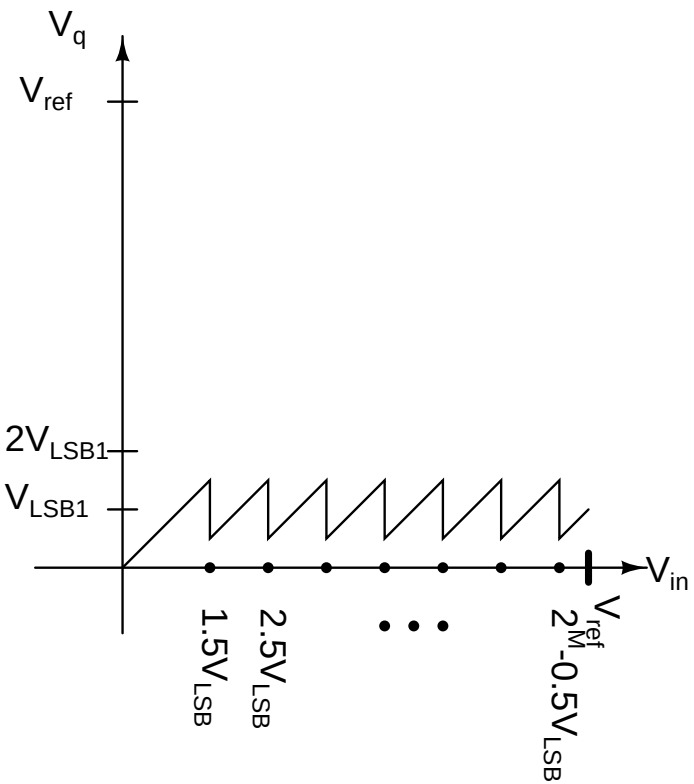
- A/D1 Transition shifted to the left
  - m greater than its ideal value by 1
  - k lesser than than its ideal value by 2^{K-1}
  - A/D output $n = 2^{K-1}m + k - 2^{K-2}$ doesn't change
- A/D1 Transition shifted to the right
  - m lesser than its ideal value by 1
  - k greater than than its ideal value by 2^{K-1}
  - A/D output $n = 2^{K-1}m + k - 2^{K-2}$ doesn't change
- 1 LSB error in m can be corrected

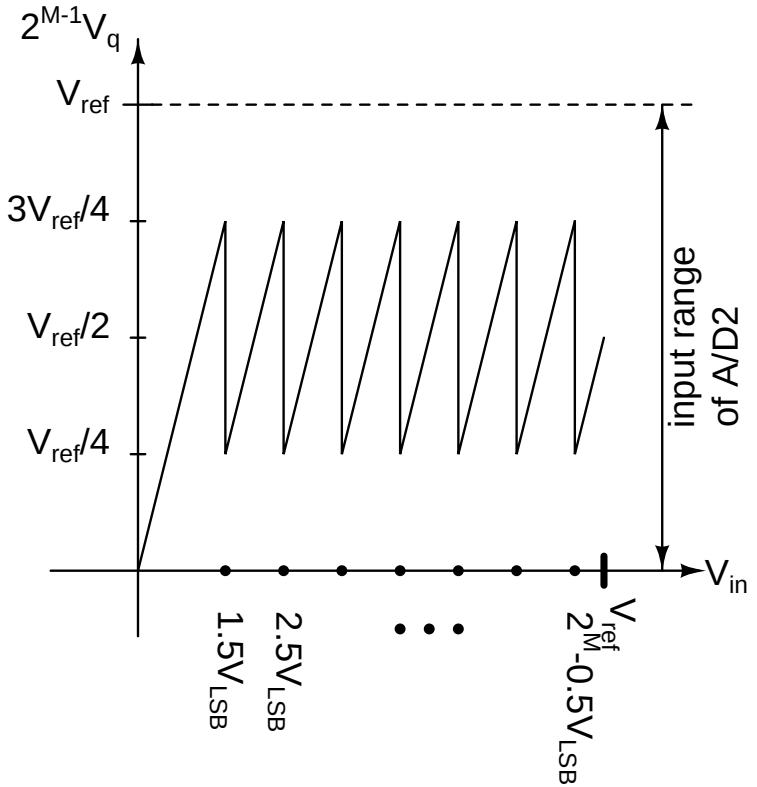
Two step A/D with digitial error correction (II)



- Reduce interstage gain to 2^{M-1}
- Shift the transitions of A/D1 to the right by $V_{ref}/2^{M+1}$ (0.5 LSB1) to keep V_q positive
- Overall accuracy is $N = M + K - 1$ bits; A/D1 contributes $M - 1$ bits, A/D2 contributes K bits; 1 bit redundancy
- Output $n = 2^{K-1}m + k$, no digital subtraction required implies simpler digital logic

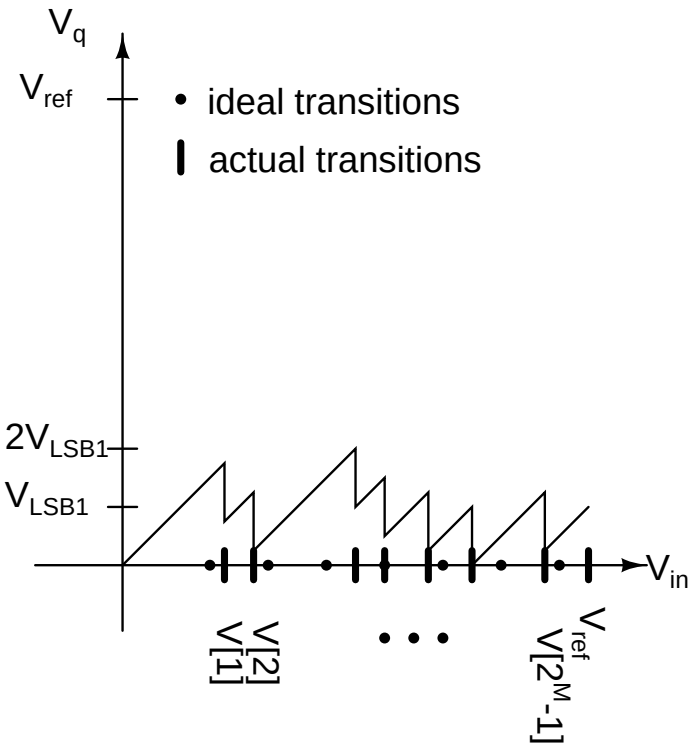
Two step A/D with digitial error correction (II)—Ideal A/D1

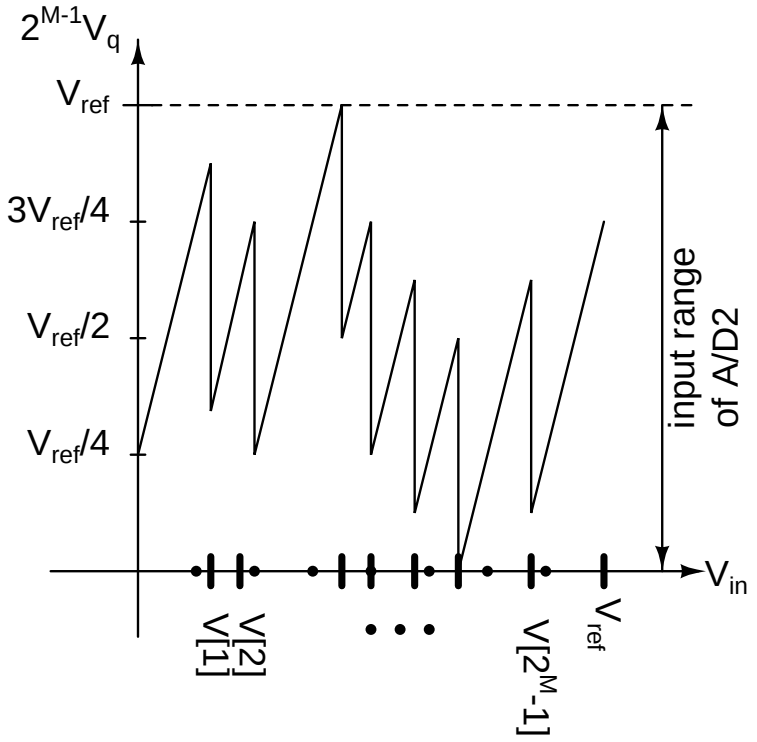




- $2^{M-1}V_q$ varies from 0 to $3V_{ref}/4$; $V_{ref}/4$ to $3V_{ref}/4$ except the first segment
- $2^{M-1}V_q$ outside this range implies errors in A/D1

Two step A/D with digitial error correction (II)—M bit accurate A/D1



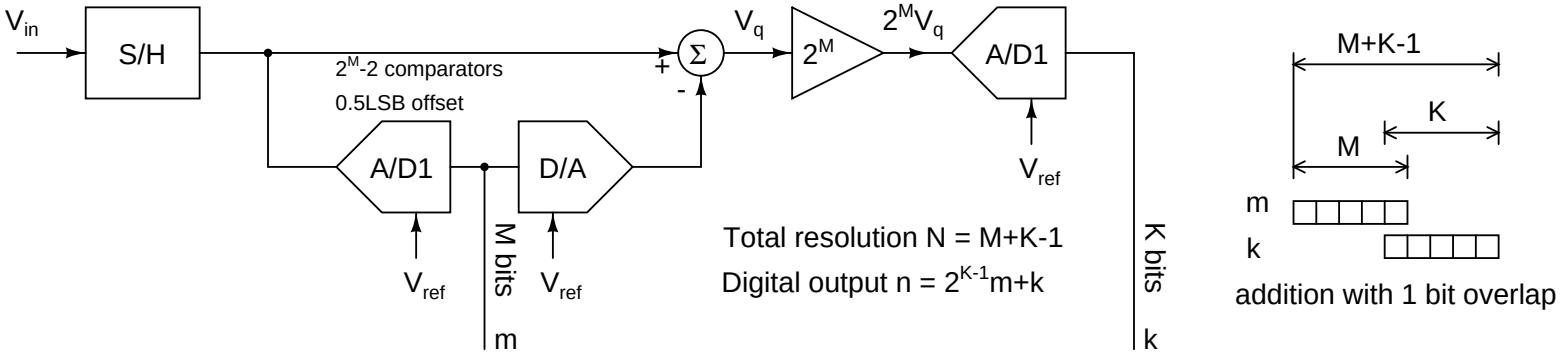


- $2^{M-1}V_q$ varies from 0 to V_{ref}
- A/D2 is not overloaded for up to 0.5 LSB errors in A/D1

Two step A/D with digitial error correction (II)—M bit accurate A/D1

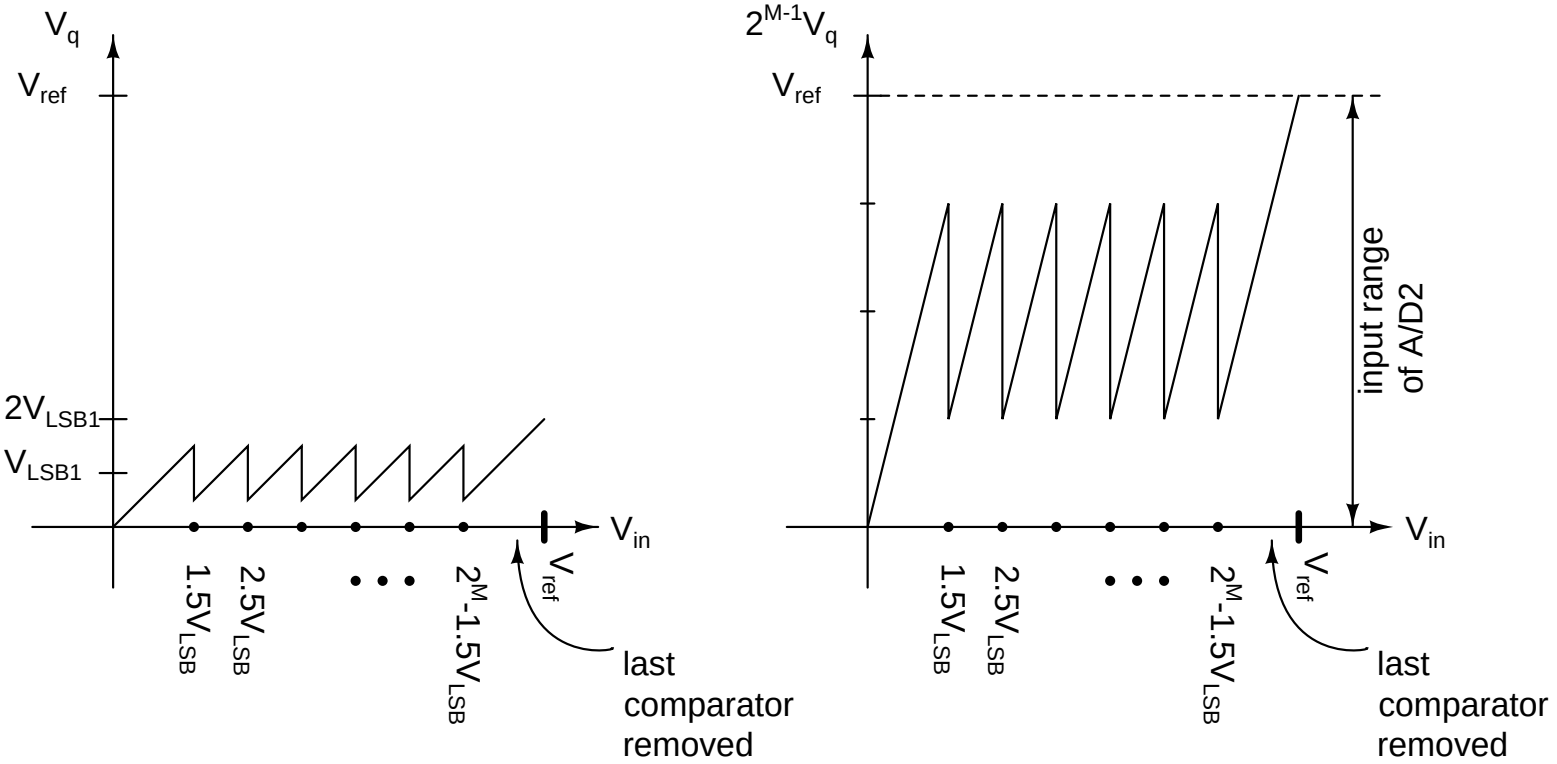
- A/D1 Transition shifted to the left
  - m greater than its ideal value by 1
  - k lesser than than its ideal value by 2^{K-1}
  - A/D output $n = 2^{K-1}m + k$ doesn't change
- A/D1 Transition shifted to the right
  - m lesser than its ideal value by 1
  - k greater than than its ideal value by 2^{K-1}
  - A/D output $n = 2^{K-1}m + k$ doesn't change
- 1 LSB error in m can be corrected

Two step A/D with digital error correction (II-a)



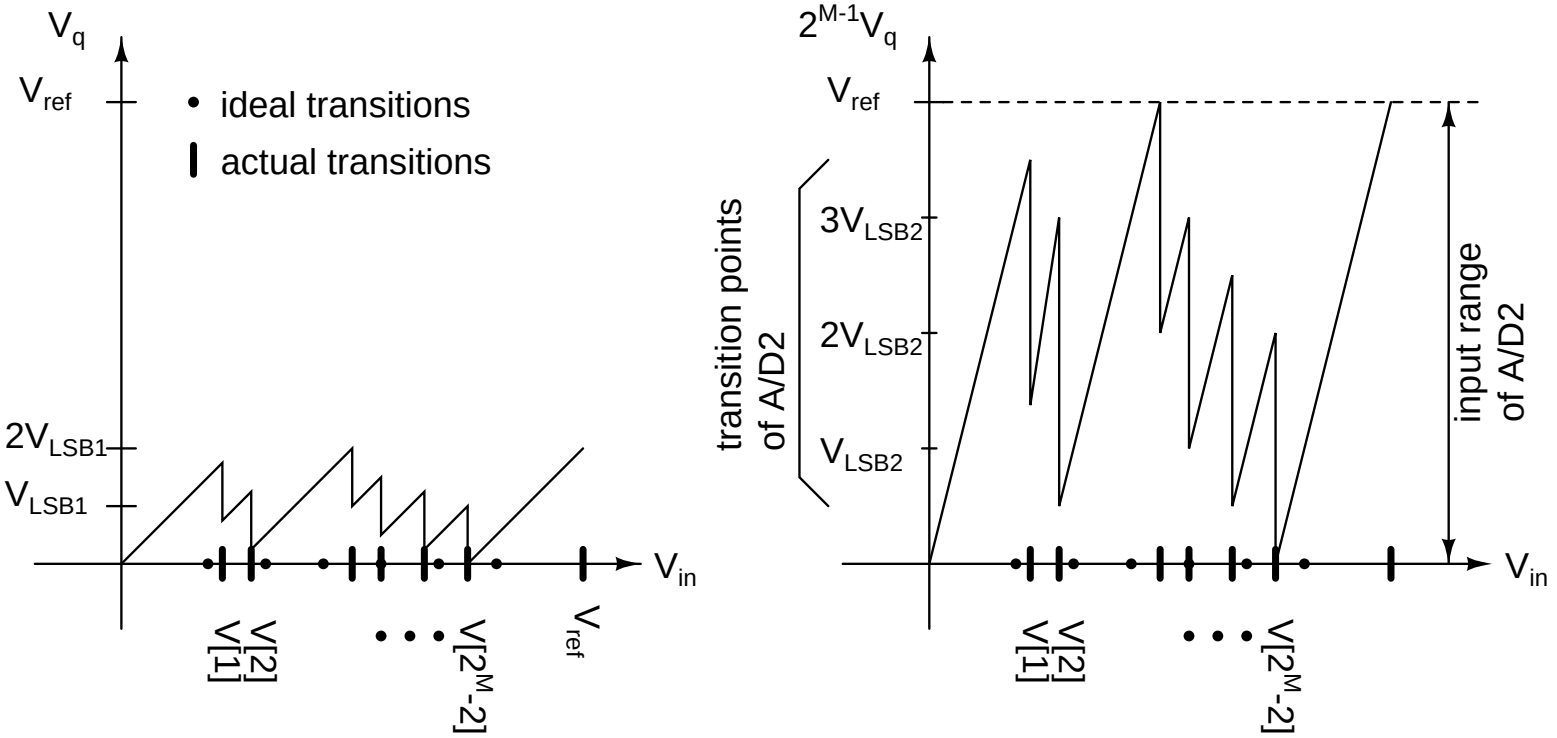
- 0.5LSB ($V_{ref}/2^{M-1}$) shifts in A/D1 transitions can be tolerated
- If the last transition ($V_{ref} - V_{ref}/2^{M-1}$) shifts to the right by $V_{ref}/2^{M-1}$, the transition is effectively nonexistent-Still the A/D output is correct
- Remove the last comparator $\Rightarrow$ M bit A/D1 has $2^M - 2$ comparators set to $1.5V_{ref}/2^M, 2.5V_{ref}/2^M, \ldots, V_{ref} - 1.5V_{ref}/2^M$
- Reduced number of comparators

Two step A/D with digitial error correction (IIa)—Ideal A/D1



- $2^{M-1}V_q$ varies from 0 to V_{ref}; $V_{ref}/4$ to $3V_{ref}/4$ except the first and last segments
- $2^{M-1}V_q$ outside this range implies errors in A/D1

Two step A/D with digitial error correction (IIa)—M bit accurate A/D1

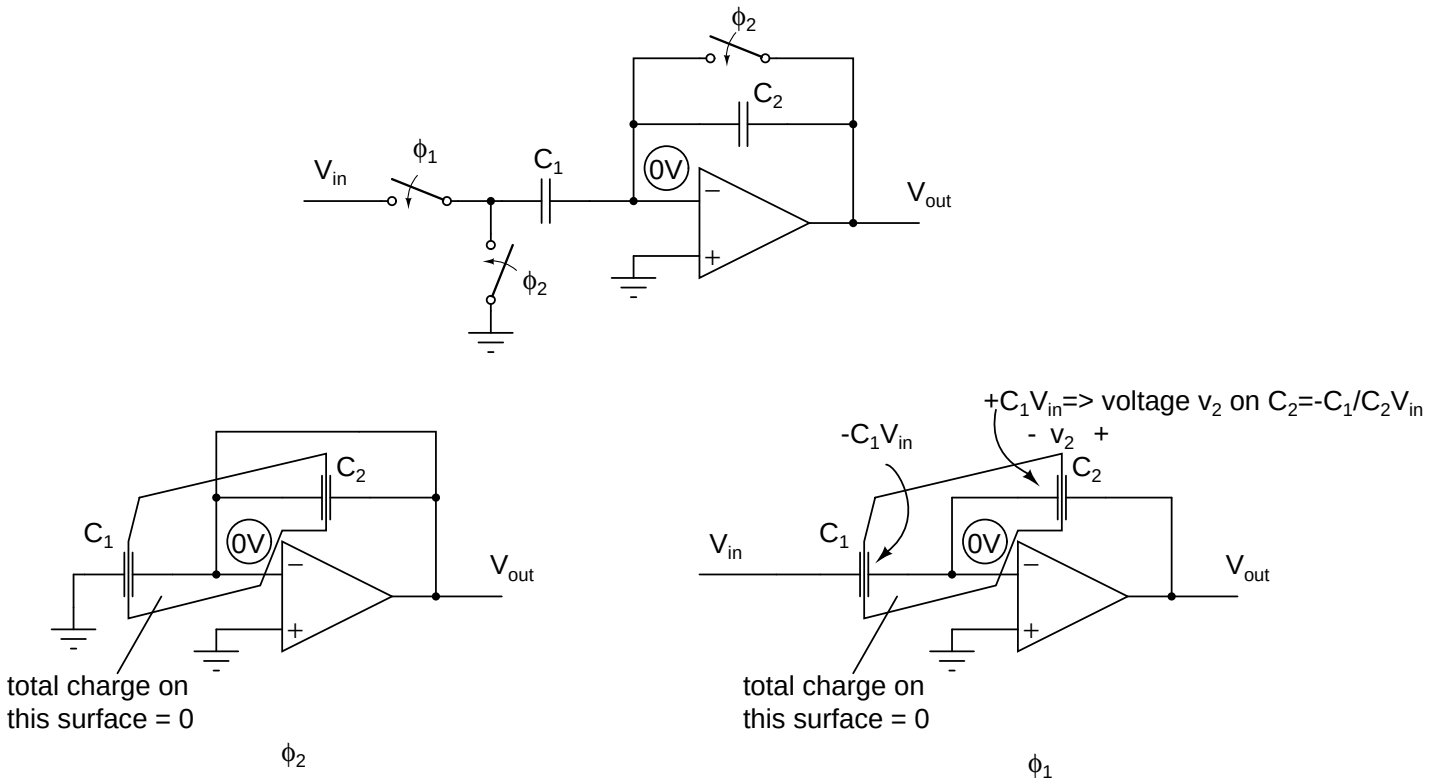


- $2^{M-1}V_q$ varies from 0 to V_{ref}
- A/D2 is not overloaded for up to 0.5 LSB errors in A/D1

Two step A/D with digitial error correction (IIa)—M bit accurate A/D1

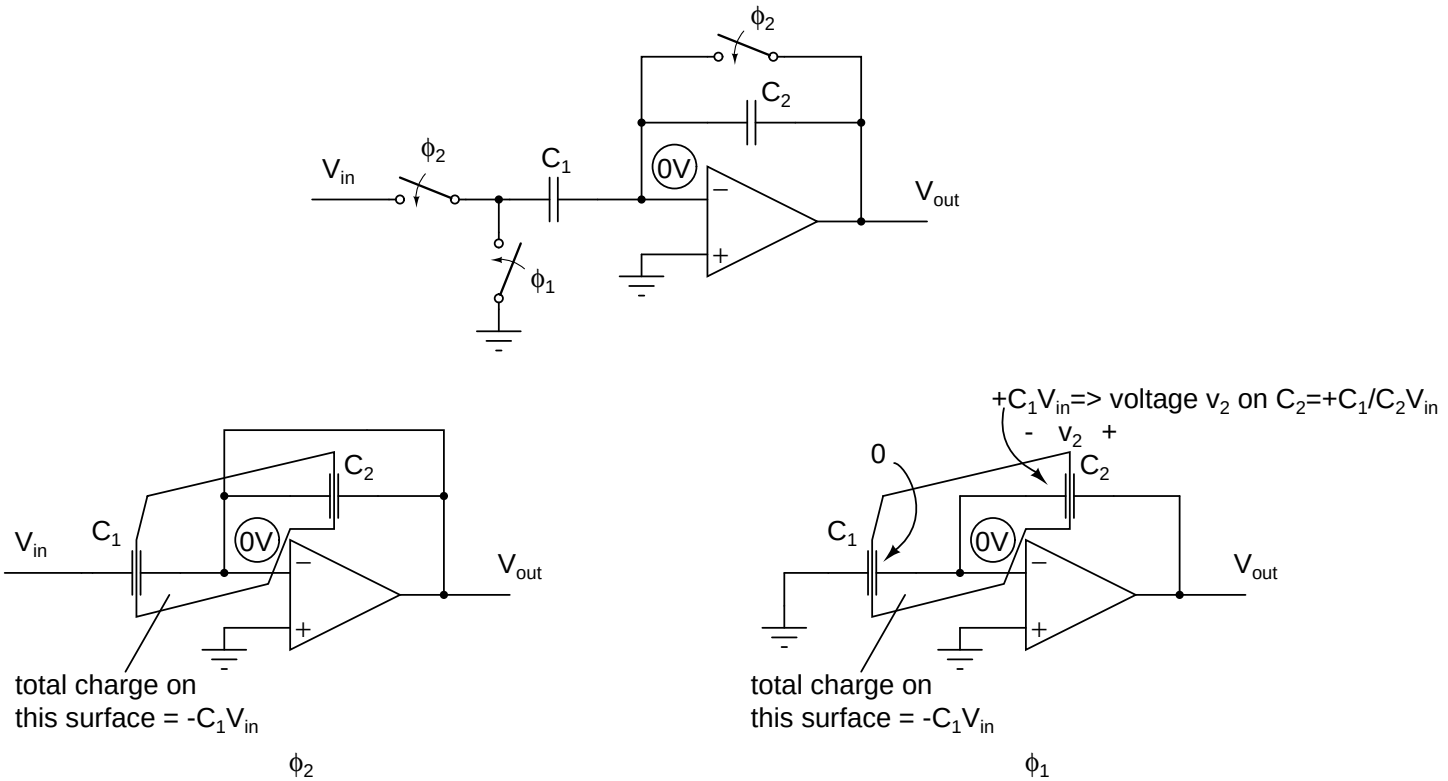
- A/D1 Transition shifted to the left
  - m greater than its ideal value by 1
  - k lesser than than its ideal value by 2^{K-1}
  - A/D output $n = 2^{K-1}m + k$ doesn't change
- A/D1 Transition shifted to the right
  - m lesser than its ideal value by 1
  - k greater than than its ideal value by 2^{K-1}
  - A/D output $n = 2^{K-1}m + k$ doesn't change
- 1 LSB error in m can be corrected

Switched capacitor (SC) amplifier



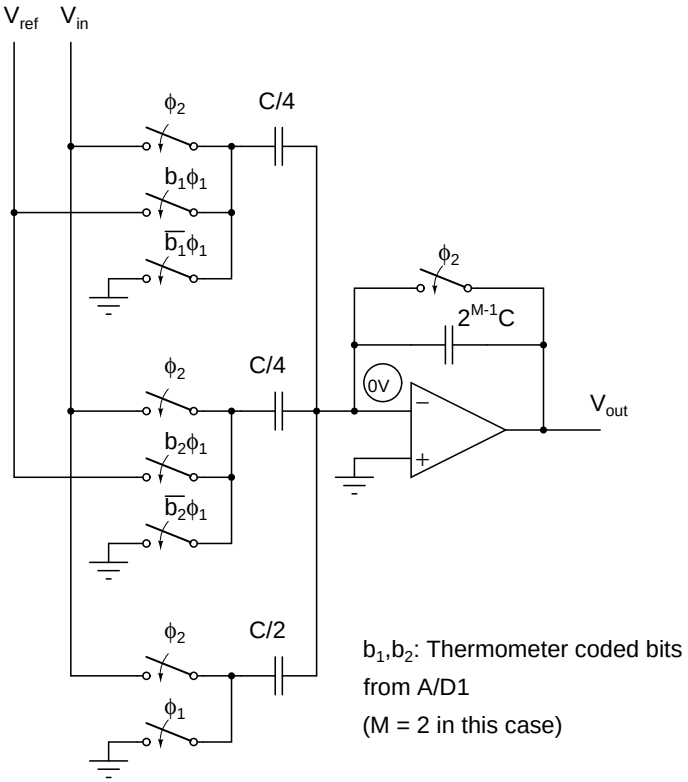
- ϕ_2: C_1 connected to ground; C_2 reset; reset switch provides dc negative feedback around the opamp
- ϕ_1: Input sampled on C_1; C_2 in feedback
- $\phi_2 \rightarrow \phi_1$: Charge at virtual ground node is conserved $\Rightarrow V_{out} = -C_1/C_2 V_{in}$

Non inverting SC amplifi er



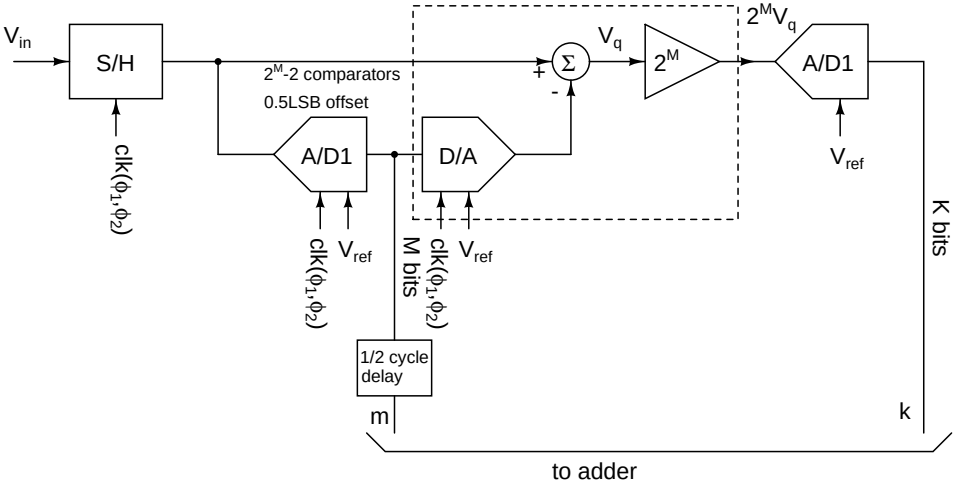
- Change the phase of input sampling to invert the gain

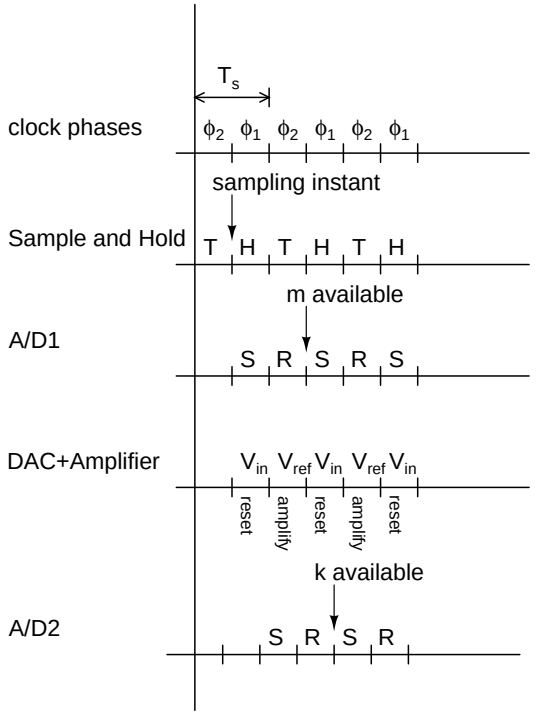
SC realization of DAC and amplifi er



- Pipelined A/D needs DAC, subtractor, and amplifier
  - V_{in} sampled on C_1 in ϕ_2 (positive gain)
  - V_{ref} sampled on $M/2^M C_1$ in ϕ_1 (negative gain). $M/2^M C_1$ realized using a switched capacitor array controlled by A/D1 output
  - $C_1/C_2 = 2^{M-1}$
  - At the end of ϕ_1, $V_{out} = 2^{M-1}\left(V_{in} - m/2^M V_{ref}\right)$

Two stage converter timing and pipelining

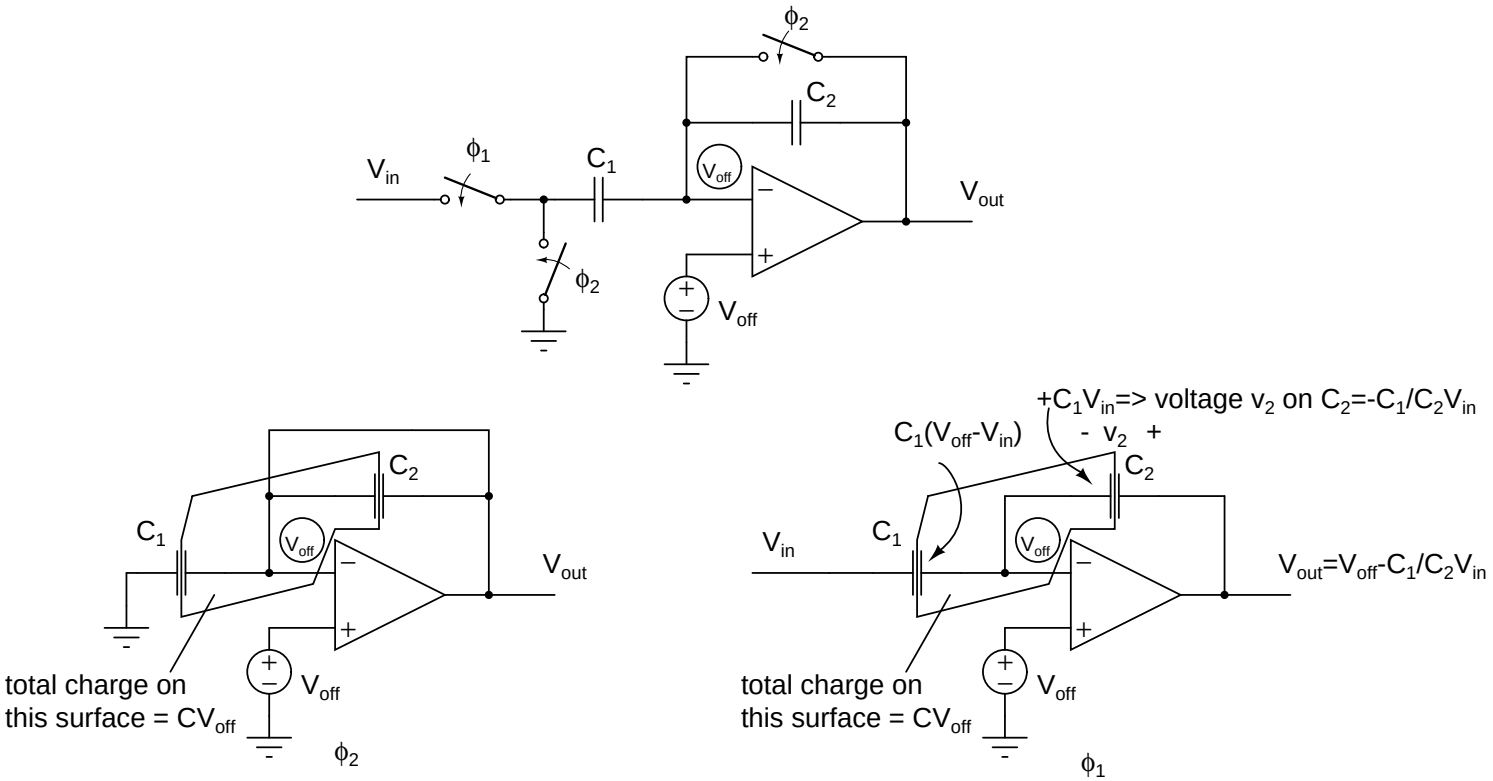




Two stage converter timing and pipelining

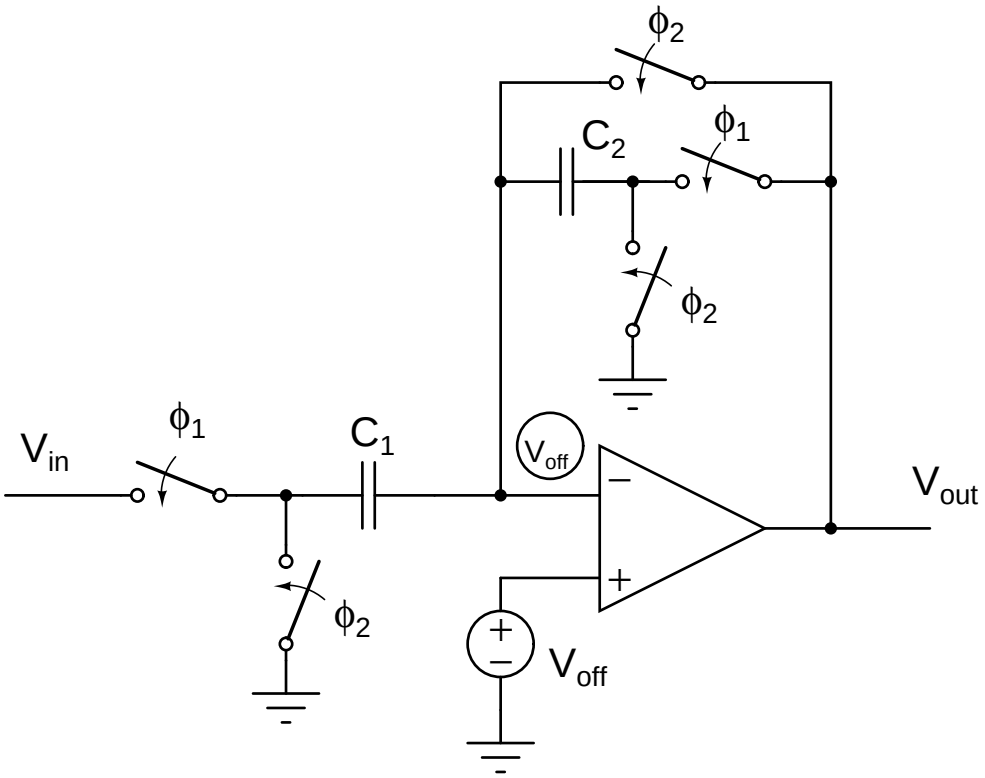
- ϕ_2
  - S/H holds the input $V_i[n]$ from the end of previous ϕ_1
  - A/D1 samples the output of S/H
  - Amplifi er samples the output of S/H on C
  - Opamp is reset
- ϕ_1
  - S/H tracks the input
  - A/D1 regenerates the digital value m
  - Amplifi er samples V_{ref} of S/H on $m/2^M C$
  - Opamp output settles to the amplifi ed residue
  - A/D2 samples the amplifi ed residue
- ϕ_2
  - A/D2 regenerates the digital value $k.\ m$, delayed by $1/2$ clock cycle, can be added to this to obtain the fi nal output
  - S/H, A/D1, Amplifi er function as before, but on the next sample $V_i[n+1]$
- In a multistep A/D, the phase of the second stage is reversed when compared to the first, phase of the third stage is the same, and so on

Effect of opamp offset



- ϕ_2: C_1 is charged to $V_{in} - V_{off}$ instead of $V_{in} \Rightarrow$ input offset cancellation; no offset in voltage across C_2
- ϕ_2: $V_{out} = -C_1/C_2 V_{in} + V_{off}$; Unity gain for offset instead of $1 + C_1/C_2$(as in a continuous time amplifier)

Correction of offset on C_2

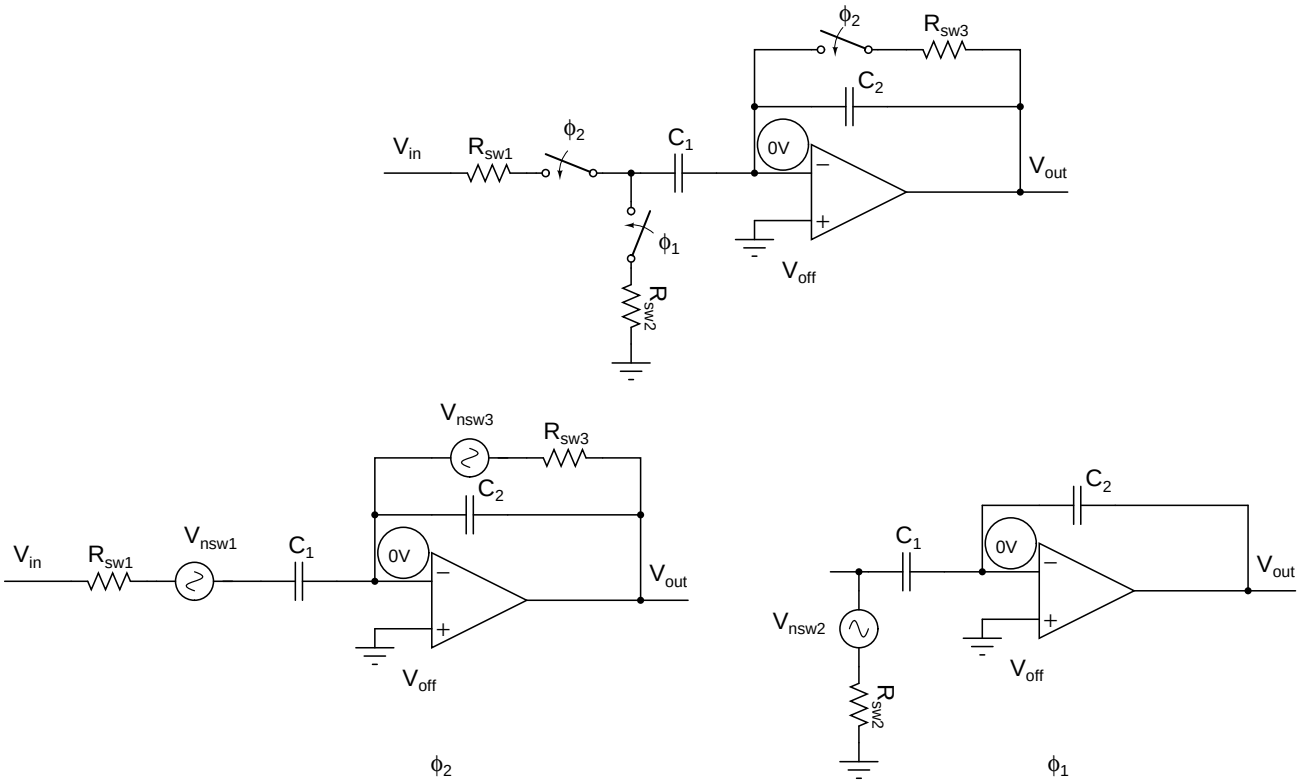


- ϕ_2: Charge C_2 to the offset voltage instead of 0 V
- ϕ_1: $V_{out} = -C_1/C_2 V_{in}$; Offset completely cancelled

Nonidealities

- Random mismatch: Capacitors must be large enough (relative matching $\alpha 1/\sqrt{WL}$ to maintain DAC, amplifier accuracy
- Thermal noise: Capacitors must be large enough to limit noise well below 1 LSB. Opamp's input referred noise should be small enough.
- Opamp dc gain: Should be large enough to reduce amplifier's output error to $V_{ref}/2^{K+1}$.
- Opamp bandwidth: Should be large enough for amplifier's output settling error to be less than $V_{ref}/2^{K+1}$.

Thermal noise in SC amplifi ers

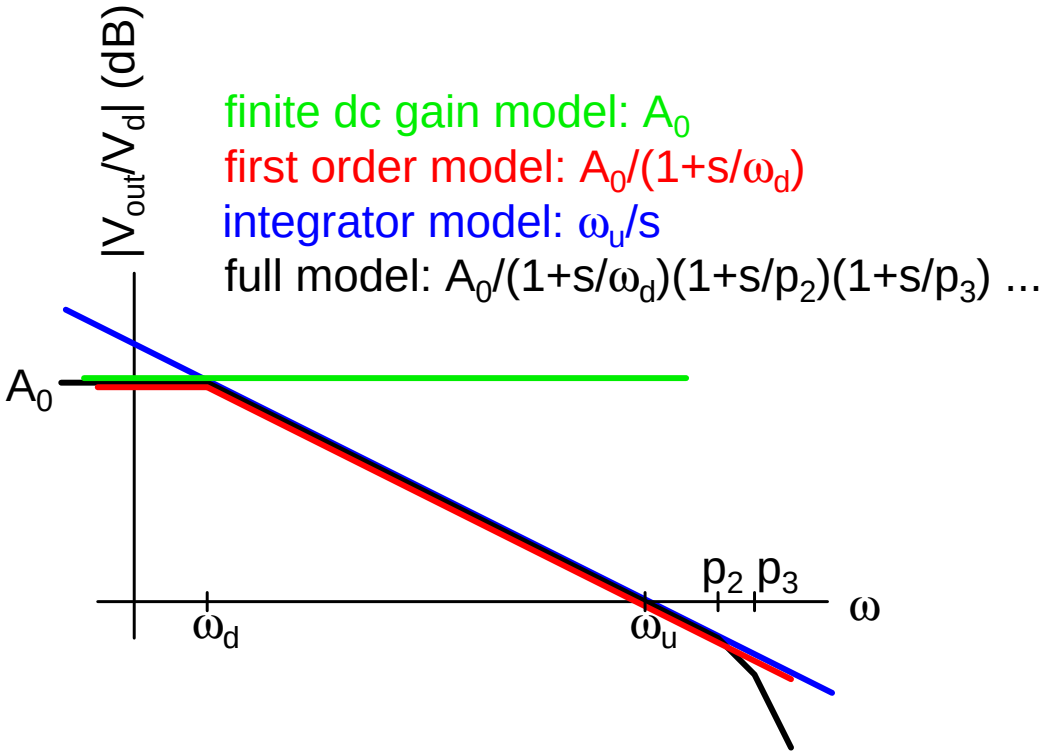


- Noise from switch resistances
- Noise from the amplifier-ignored

Thermal noise in SC amplifi ers

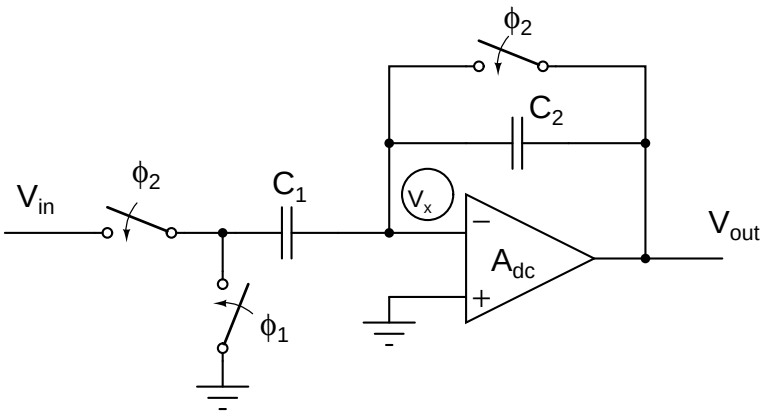
- ϕ_2:
  - R_{sw1}: C_1 has a voltage noise of variance kT/C_1
  - R_{sw2}: C_2 has a voltage noise of variance kT/C_2.
- ϕ_1:
  - R_{sw1}: Its contribution in ϕ_2 (kT/C_1) will be amplifi ed to $kT/C_1(C_1/C_2)^2$
  - R_{sw2}: Its contribution in ϕ_2 (kT/C_1) will be held
  - R_{sw3}: Results in a noise kT/C_1 on C_1 and $kT/C_1(C_1/C_2)^2$ at the output
- Total output noise: $kT/C_2(2C_1/C_2+1) \approx 2kT/C_1(C_1/C_2)^2$
- Input referred noise: $kT/C_1(2+C_2/C_1) \approx 2kT/C_1$
- C_1 must be large enough to minimize the effects of thermal noise

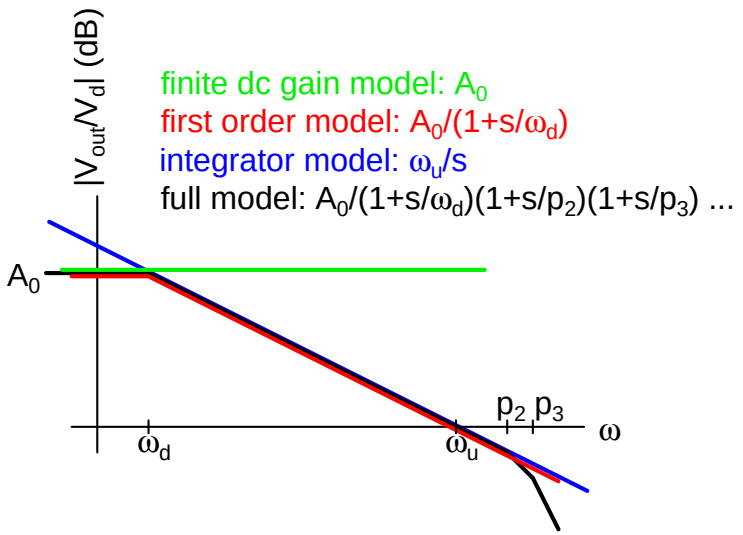
Op amp models



- Opamp has finite dc gain, predominantly first order rolloff, and many high frequency poles
- High frequency poles should be beyond the unity gain frequency of the feedback loop gain (not necessarily the opamp's open loop gain) for stability.
- Effect of dc gain and first order rolloff modeled separately for simplicity

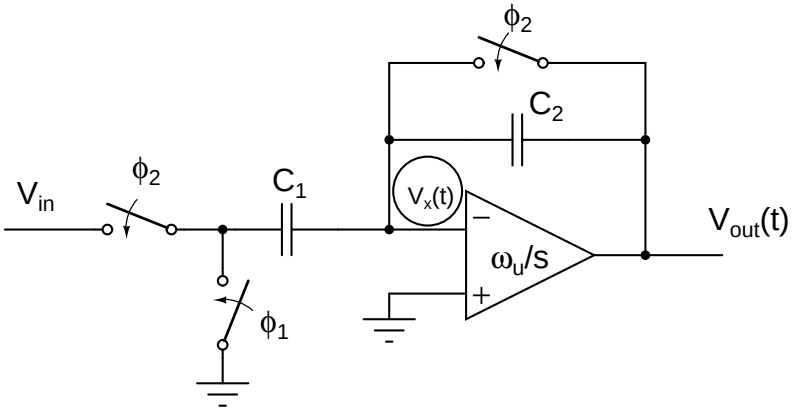
Effect of opamp dc gain

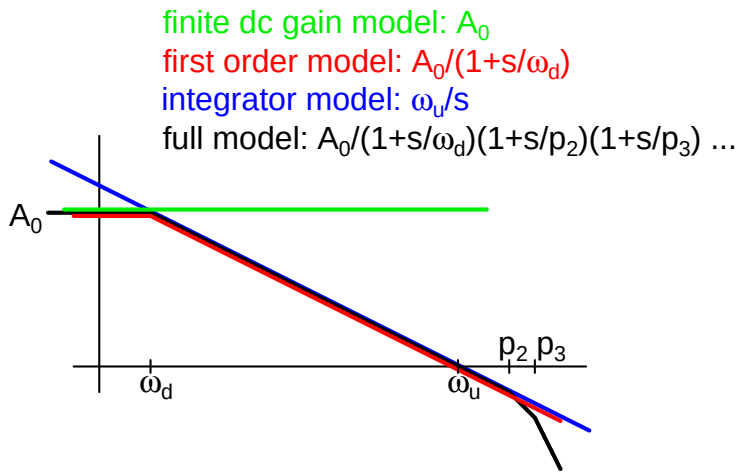




- ϕ_2: $V_{out} = V_x = 0$
- ϕ_1: $V_{out} = C_1/C_2 \times 1/1 + (1 + C_1/C_2)/A_0 V_{in}$;
- Reduced dc gain in the amplifier
- Error should be smaller than $V_{ref}/2^{K+1} \Rightarrow$ $A_0 > 2^{M+K} + 2^{K+1} - 2^{M-1} - 1$
- Approximately, $A_0 > 2^{M+K}$, 2/LSB of the overall converter

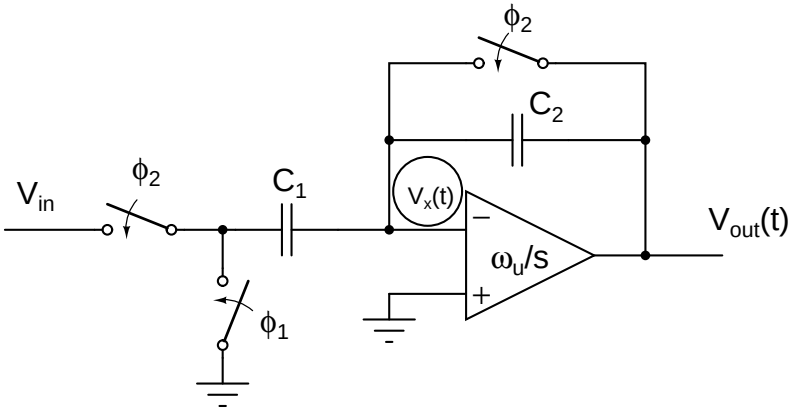
Effect of fi nite unity gain frequency of the opamp

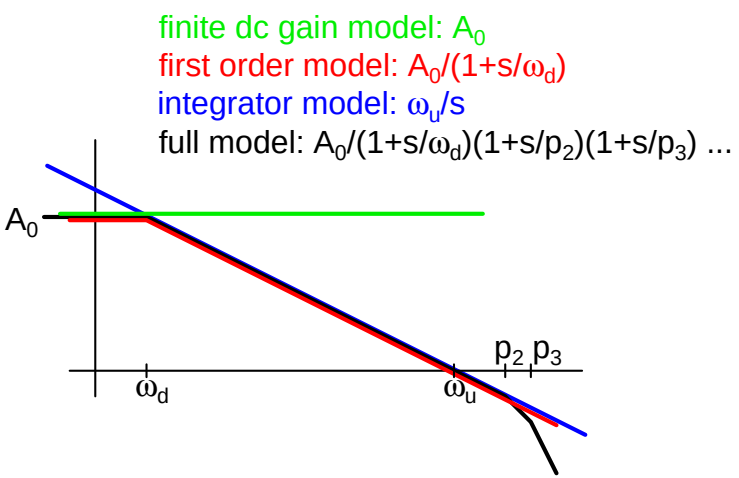




- ϕ_2: $V_{out}(t) = V_x(t) = V_{out}(0)\exp(-\omega_u t)$
- Incomplete reset
- Worst case: $V_{out}(0) = V_{ref}$; Error smaller than $V_{ref}/2^{K+1}$ at the $t = T_s/2$
- $\omega_u \geq 2\ln(2)(K+1)f_s$
- $p_{2,3,...} > \omega_u$

Effect of fi nite unity gain frequency of the opamp



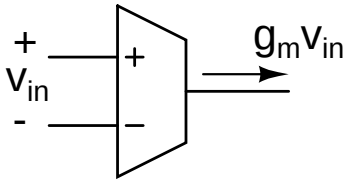


- ϕ_1: $V_{out}(t) = C_1/C_2 V_{in}\left(1-\exp(-\omega_u \frac{C_2}{C_1+C_2}t)\right) + V_{out}(0)\exp(-\omega_u \frac{C_2}{C_1+C_2}t)$
- Incomplete settling of amplified residue V_q
- Worst case: $C_1/C_2 V_{in} = V_{ref}$; Error smaller than $V_{ref}/2^{K+1}$ at the $t = T_s/2$; $V_{out}(0) = 0$ after reset.
- $\omega_u/(1+2^{M-1}) \geq 2\ln(2)(K+1)f_s$ (ω_u in rad/s, f_s in Hz)
- $\omega_u/(1+2^{M-1})$ is the unity loop gain frequency assuming no parasitics
- $p_{2,3,...} > \omega_u/(1+2^{M-1})$

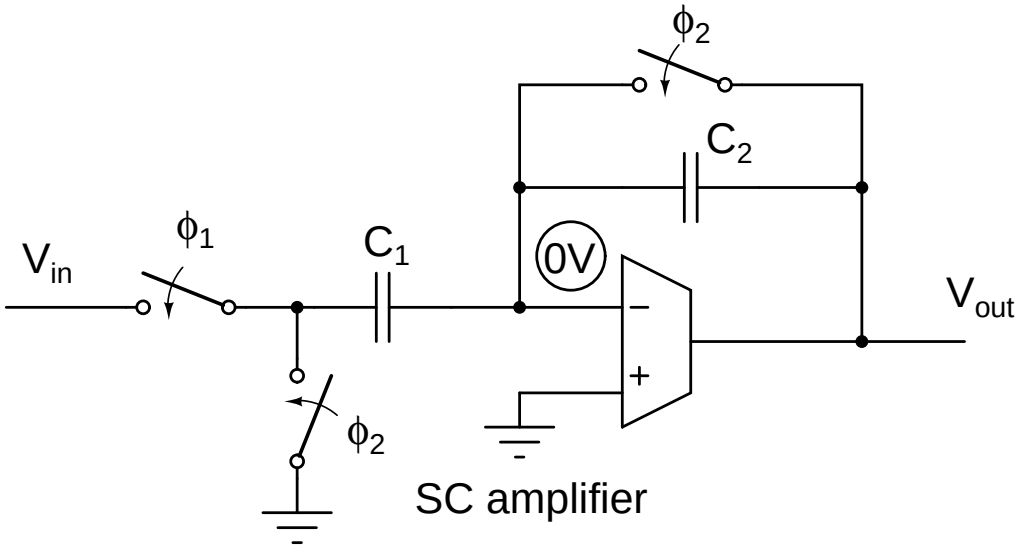
Effect of fi nite unity gain frequency of the opamp

- Depending on amplifier topology, reset and amplifying phases pose different constraints
- In our example, amplifying phase constraint is more stringent (loop gain in amplifying and reset phases are very different-better to have them close to each other)
- ω_u itself can depend on capacitive load(different for ϕ_1, ϕ_2)
- Higher order poles $p_2, p_3, \ldots$ need to be placed above the unity loop gain frequency, not necessarily ω_u

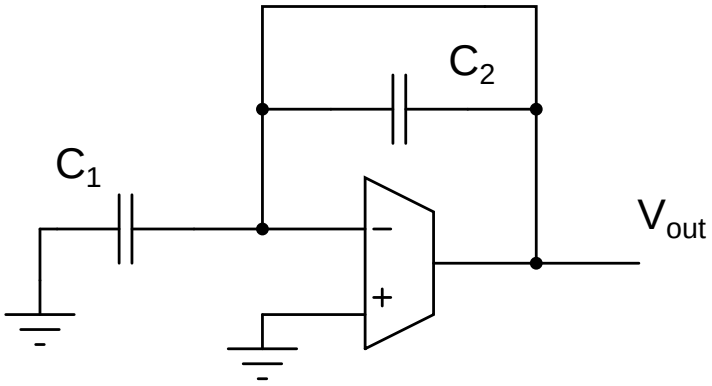
Single stage opamp-transconductor

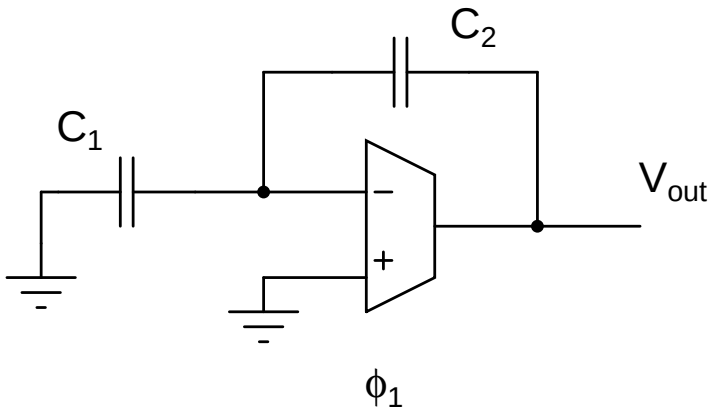


Model of a
single stage opamp



SC amplifier

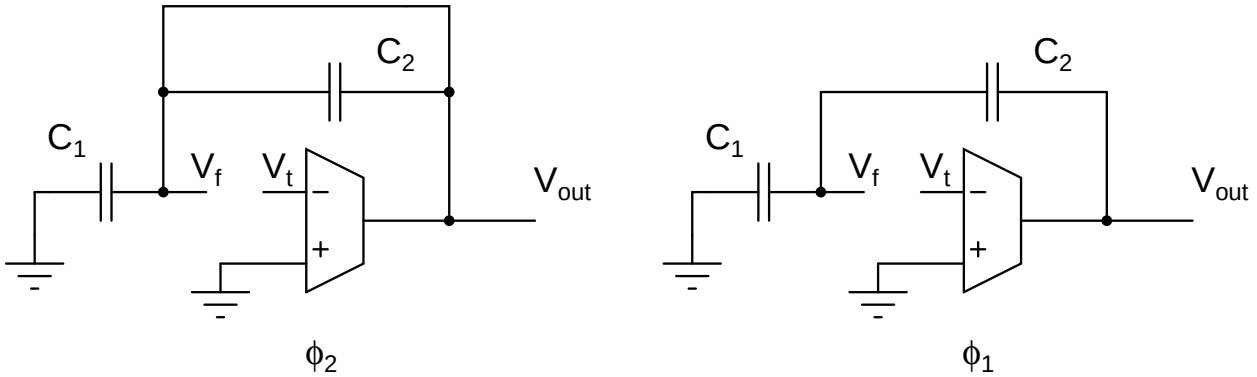




- ϕ_1: Capacitive load = C_1
- ϕ_2: Capacitive load = $C_1 C_2/(C_1 + C_2)$

Single stage opamp-transconductor

Loop opened at opamp input

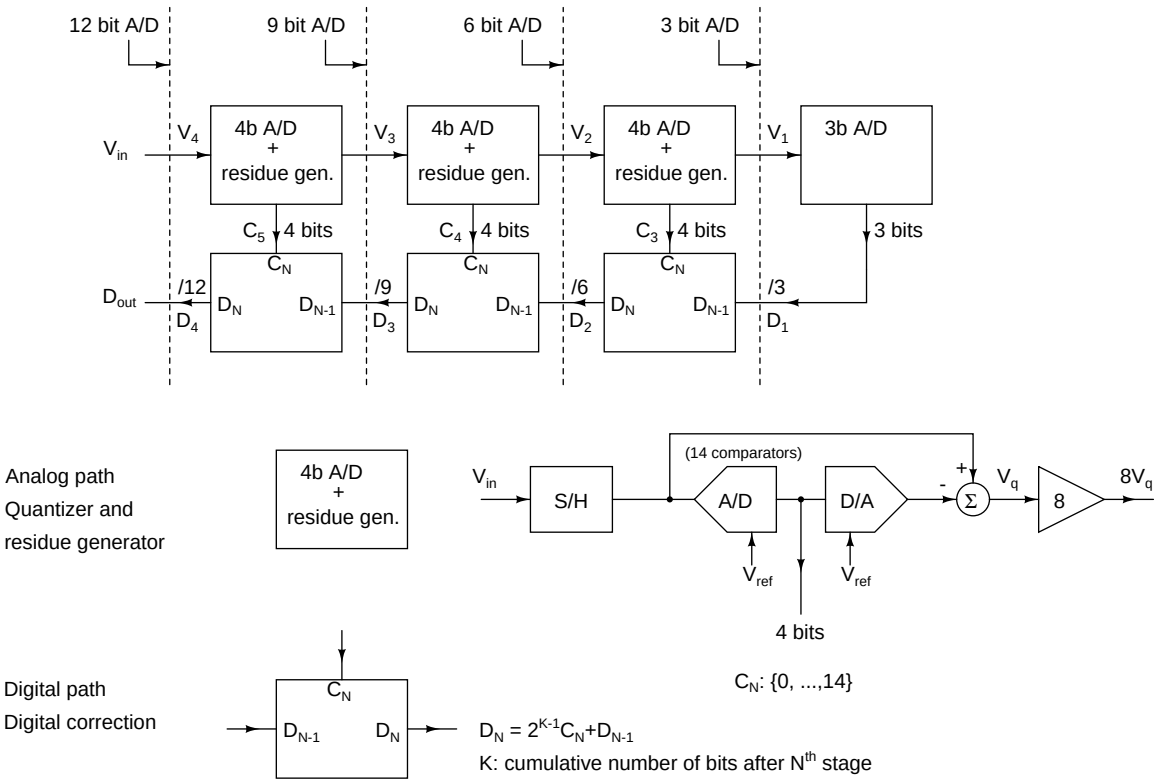


- Loop broken at the opamp input to evaluate loop gain
- ϕ_1
  - $V_{out}(s)/V_t(s) = g_m/sC_1$
  - Opamp unity gain frequency $\omega_u = g_m/C_1$
  - $V_f(s)/V_t(s) = g_m/sC_1$
  - Unity loop gain frequency $\omega_{u,loop} = g_m/C_1$
- ϕ_2
  - $V_{out}(s)/V_t(s) = g_m/s(C_1C_2/C_1 + C_2)$
  - Opamp unity gain frequency $\omega_u = g_m/(C_1C_2/C_1 + C_2)$
  - $V_f(s)/V_t(s) = g_m/sC_1$
  - Unity loop gain frequency $\omega_{u,loop} = g_m/C_1$

Multi step converters

- Two step architecture can be extended to multiple steps
- All stages except the last have their outputs digitally corrected from the following A/D output
- Accuracy of components in each stage depends on the accuracy of the A/D converter following it.
- Accuracy requirements less stringent down the pipeline, but optimizing every stage separately increases design effort
- Pipelined operation to obtain high sampling rates
- Last stage is not digitally corrected

Multi step A/D converter



- 4,4,4,3 bits for an effective resolution of 12 bits
- 3 effective bits per stage

Multi step converter-tradeoffs

- Large number of stages, fewer bits per stage
  - Fewer comparators, low accuracy-lower power consumption
  - Larger number of amplifi ers-power consumption increases
  - Larger latency
- Fewer stages, more bits per stage
  - More comparators, higher accuracy designs
  - Smaller number of amplifi ers-lower power consumption
  - Smaller latency
- Typically 3-4 bits per stage easy to design