Pipelined multi step A/D converters

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Motivation for multi step A/D conversion

- Flash converters:
  - Area and power consumption increase exponentially with number of bits $N$
  - Impractical beyond 7-8 bits.
- Multi step conversion—Coarse conversion followed by fine conversion
  - Multi-step converters
  - Subranging converters
- Multi step conversion takes more time
  - Pipelining to increase sampling rate
- Second A/D quantizes the quantization error of first A/D
- Concatenate the bits from the two A/D converters to form the final output
Two step A/D converter-basic operation

- A/D1, DAC, and A/D2 have the same range $V_{ref}$
- Second A/D quantizes the quantization error of first A/D
  - Use a DAC and subtractor to determine $V_q$
  - Amplify $V_q$ to full range of the second A/D
- Final output $n$ from $m$, $k$
  - A/D1 output is $m$ (DAC output is $m/2^M V_{ref}$)
  - A/D2 input is at $k^{th}$ transition ($k/2^K V_{ref}$)
  - $V_{in} = k/2^K V_{ref} \times 1/2^M + m/2^M V_{ref}$
  - $V_{in} = (2^K m + k)/2^{M+K} V_{ref}$
- Resolution $N = M + K$, output $n = 2^K m + k$ 
  - Concatenate the bits from the two A/D converters to form the final output
Two step A/D converter: Example with $M = 3$, $K = 2$

- Second A/D quantizes the quantization error of first A/D
- Transitions of second A/D lie between transitions of the first, creating finely spaced transition points for the overall A/D.
Quantization error $V_q$

- $V_q$ vs. $V_{in}$: Discontinuous transfer curve
  - Location of discontinuities: Transition points of A/D1
  - Size of discontinuities: Step size of D/A
  - Slope: unity

Location of discontinuities:
- Transition points of A/D1

Size of discontinuities:
- Step size of D/A

Slope:
- Unity
A/D1 transitions exactly at integer multiples of $V_{ref}/2^M$
Quantization error $V_q$ limited to $(0, V_{ref}/2^M)$
$2^M V_q$ exactly fits the range of A/D2
Two step A/D converter—M bit accurate A/D1

- A/D1 transitions in error by up to $V_{ref}/2^{M+1}$
- Quantization error $V_q$ limited to $(-V_{ref}/2^{M+1}, 3V_{ref}/2^{M+1})$—a range of $V_{ref}/2^{M-1}$
- $2^M V_q$ overloads A/D2
Two step A/D with digital error correction (I)

- Reduce interstage gain to $2^{M-1}$
- Add $V_{ref}/2^{M+1}$ (0.5 LSB1) offset to DAC output to keep $V_q$ positive
- Subtract $2^{K-2}$ from digital output to compensate for the added offset
- Overall accuracy is $N = M + K - 1$ bits; A/D1 contributes $M - 1$ bits, A/D2 contributes $K$ bits; 1 bit redundancy
- Output $n = 2^{K-1}m + k - 2^{K-2}$
Two step A/D with digital error correction (I)—Ideal
A/D1

- $2^{M-1}V_q$ varies from $V_{ref}/4$ to $3V_{ref}/4$
- $2^{M-1}V_q$ outside this range implies errors in A/D1
Two step A/D with digital error correction (I)—M bit accurate A/D1

\[ 2^{M-1} V_q \text{ varies from 0 to } V_{\text{ref}} \]

\[ \text{A/D2 is not overloaded for up to 0.5 LSB errors in A/D1} \]
Two step A/D with digital error correction (I)—M bit accurate A/D1

- A/D1 Transition shifted to the left
  - \( m \) greater than its ideal value by 1
  - \( k \) lesser than its ideal value by 2
  - A/D output \( n = 2^{K-1} m + k - 2^{K-2} \) doesn’t change

- A/D1 Transition shifted to the right
  - \( m \) lesser than its ideal value by 1
  - \( k \) greater than its ideal value by 2
  - A/D output \( n = 2^{K-1} m + k - 2^{K-2} \) doesn’t change

- 1 LSB error in \( m \) can be corrected

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Reduce interstage gain to $2^{M-1}$

Shift the transitions of A/D1 to the right by $V_{ref}/2^{M+1}$ (0.5 LSB1) to keep $V_q$ positive

Overall accuracy is $N = M + K - 1$ bits; A/D1 contributes $M - 1$ bits, A/D2 contributes $K$ bits; 1 bit redundancy

Output $n = 2^{K-1}m + k$, no digital subtraction required implies simpler digital logic
Two step A/D with digital error correction (II)—Ideal A/D1

- $2^{M-1}V_q$ varies from 0 to $3V_{ref}/4$; $V_{ref}/4$ to $3V_{ref}/4$ except the first segment
- $2^{M-1}V_q$ outside this range implies errors in A/D1
Two step A/D with digital error correction (II)—M bit accurate A/D1

- ideal transitions
- actual transitions

$2^{M-1}V_q$ varies from 0 to $V_{ref}$

A/D2 is not overloaded for up to 0.5 LSB errors in A/D1
Two step A/D with digital error correction (II)—M bit accurate A/D1

- A/D1 Transition shifted to the left
  - $m$ greater than its ideal value by 1
  - $k$ lesser than its ideal value by $2^{K-1}$
  - A/D output $n = 2^{K-1}m + k$ doesn’t change

- A/D1 Transition shifted to the right
  - $m$ lesser than its ideal value by 1
  - $k$ greater than its ideal value by $2^{K-1}$
  - A/D output $n = 2^{K-1}m + k$ doesn’t change

- 1 LSB error in $m$ can be corrected
0.5LSB \( \left( \frac{V_{\text{ref}}}{2^M} \right) \) shifts in A/D1 transitions can be tolerated

If the last transition \( \left( V_{\text{ref}} - \frac{V_{\text{ref}}}{2^M} \right) \) shifts to the right by \( \frac{V_{\text{ref}}}{2^M} \), the transition is effectively nonexistent-Still the A/D output is correct

Remove the last comparator \( \Rightarrow M \) bit A/D1 has \( 2^M - 2 \) comparators set to
\[
1.5 \frac{V_{\text{ref}}}{2^M}, 2.5 \frac{V_{\text{ref}}}{2^M}, \ldots, V_{\text{ref}} - 1.5 \frac{V_{\text{ref}}}{2^M}
\]

Reduced number of comparators
Two step A/D with digital error correction (IIa)—Ideal A/D1

- $2^{M-1}V_q$ varies from 0 to $V_{ref}$; $V_{ref}/4$ to $3V_{ref}/4$ except the first and last segments
- $2^{M-1}V_q$ outside this range implies errors in A/D1
Two step A/D with digital error correction (IIa)—M bit accurate A/D1

- $2^{M-1}V_q$ varies from 0 to $V_{ref}$
- A/D2 is not overloaded for up to 0.5 LSB errors in A/D1
Two step A/D with digital error correction (IIa)—M bit accurate A/D1

- A/D1 Transition shifted to the left
  - $m$ greater than its ideal value by 1
  - $k$ lesser than than its ideal value by $2^{K-1}$
  - A/D output $n = 2^{K-1}m + k$ doesn’t change

- A/D1 Transition shifted to the right
  - $m$ lesser than its ideal value by 1
  - $k$ greater than than its ideal value by $2^{K-1}$
  - A/D output $n = 2^{K-1}m + k$ doesn’t change

- 1 LSB error in $m$ can be corrected
Switched capacitor (SC) amplifier

- \( V_{in} \)
- \( V_{out} \)
- \( C_1 \)
- \( C_2 \)
- \( \phi_1 \)
- \( \phi_2 \)

\( V_{out} = -\frac{C_1}{C_2} V_{in} \)

- \( \phi_2 \): \( C_1 \) connected to ground; \( C_2 \) reset; reset switch provides dc negative feedback around the opamp

- \( \phi_1 \): Input sampled on \( C_1 \); \( C_2 \) in feedback

- \( \phi_2 \rightarrow \phi_1 \): Charge at virtual ground node is conserved

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Pipelined multi step A/D converters
Non inverting SC amplifier

\[ V_{in} \rightarrow \phi_2 \rightarrow C_1 \rightarrow \text{op-amp} \rightarrow \phi_1 \rightarrow C_2 \rightarrow V_{out} \]

- Change the phase of input sampling to invert the gain

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Pipelined multi step A/D converters
Pipelined A/D needs DAC, subtractor, and amplifier

- $V_{in}$ sampled on $C_1$ in $\phi_2$ (positive gain)
- $V_{ref}$ sampled on $M/2^M C_1$ in $\phi_1$ (negative gain). $M/2^M C_1$ realized using a switched capacitor array controlled by A/D1 output
- $C_1/C_2 = 2^{M-1}$
- At the end of $\phi_1$, $V_{out} = 2^{M-1} \left(V_{in} - m/2^M V_{ref}\right)$
Two stage converter timing and pipelining

Sample and Hold

A/D1

DAC+Amplifier

A/D2

Clock phases

$\phi_2 \phi_1 \phi_2 \phi_1 \phi_2 \phi_1$

Sampling instant

$m$ available

$k$ available

$V_{in}$, $V_{ref}$, $V_{in}$, $V_{ref}$, $V_{in}$

$S$, $R$, $S$, $R$, $S$

$T_s$

$2^M$-2 comparators

0.5LSB offset

1/2 cycle delay

$m$

$k$

To adder
Two stage converter timing and pipelining

- $\phi_2$
  - S/H holds the input $V_i[n]$ from the end of previous $\phi_1$
  - A/D1 samples the output of S/H
  - Amplifier samples the output of S/H on $C$
  - Opamp is reset

- $\phi_1$
  - S/H tracks the input
  - A/D1 regenerates the digital value $m$
  - Amplifier samples $V_{\text{ref}}$ of S/H on $m/2^M C$
  - Opamp output settles to the amplified residue
  - A/D2 samples the amplified residue

- $\phi_2$
  - A/D2 regenerates the digital value $k$. $m$, delayed by $1/2$ clock cycle, can be added to this to obtain the final output
  - S/H, A/D1, Amplifier function as before, but on the next sample $V_i[n + 1]$

- In a multistep A/D, the phase of the second stage is reversed when compared to the first, phase of the third stage is the same, and so on
Effect of opamp offset

- $\phi_2$: $C_1$ is charged to $V_{in} - V_{off}$ instead of $V_{in} \Rightarrow$ input offset cancellation; no offset in voltage across $C_2$
- $\phi_2$: $V_{out} = -\frac{C_1}{C_2} V_{in} + V_{off}$; Unity gain for offset instead of $1 + \frac{C_1}{C_2}$ (as in a continuous time amplifier)
Correction of offset on $C_2$

- $\phi_2$: Charge $C_2$ to the offset voltage instead of 0 V
- $\phi_1$: $V_{out} = -\frac{C_1}{C_2} V_{in}$; Offset completely cancelled
Nonidealities

- Random mismatch: Capacitors must be large enough (relative matching $\alpha 1/\sqrt{WL}$) to maintain DAC, amplifier accuracy.

- Thermal noise: Capacitors must be large enough to limit noise well below 1 LSB. Opamp’s input referred noise should be small enough.

- Opamp dc gain: Should be large enough to reduce amplifier’s output error to $V_{\text{ref}}/2^{K+1}$.

- Opamp bandwidth: Should be large enough for amplifier’s output settling error to be less than $V_{\text{ref}}/2^{K+1}$.
Thermal noise in SC amplifiers

- Noise from switch resistances
- Noise from the amplifier-ignored
Thermal noise in SC amplifiers

- $\phi_2$:
  - $R_{sw1}$: $C_1$ has a voltage noise of variance $kT/C_1$
  - $R_{sw2}$: $C_2$ has a voltage noise of variance $kT/C_2$.

- $\phi_1$:
  - $R_{sw1}$: Its contribution in $\phi_2 (kT/C_1)$ will be amplified to $kT/C_1 (C_1/C_2)^2$
  - $R_{sw2}$: Its contribution in $\phi_2 (kT/C_1)$ will be held
  - $R_{sw3}$: Results in a noise $kT/C_1$ on $C_1$ and $kT/C_1 (C_1/C_2)^2$ at the output

- Total output noise: $kT/C_2 (2C_1/C_2 + 1) \approx 2kT/C_1 (C_1/C_2)^2$
- Input referred noise: $kT/C_1 (2 + C_2/C_1) \approx 2kT/C_1$
- $C_1$ must be large enough to minimize the effects of thermal noise
Op amp models

- Opamp has finite dc gain, predominantly first order rolloff, and many high frequency poles
- High frequency poles should be beyond the unity gain frequency of the feedback loop gain (not necessarily the opamp’s open loop gain) for stability.
- Effect of dc gain and first order rolloff modeled separately for simplicity

finite dc gain model: $A_0$
first order model: $A_0/(1+s/\omega_d)$
integrator model: $\omega_u/s$
full model: $A_0/(1+s/\omega_d)(1+s/p_2)(1+s/p_3) ...$
Effect of opamp dc gain

- $\phi_2$: $V_{out} = V_x = 0$
- $\phi_1$: $V_{out} = C_1/C_2 \times 1/1 + (1 + C_1/C_2)/A_0 V_{in}$;

Reduced dc gain in the amplifier

Error should be smaller than $V_{ref}/2^{K+1} \Rightarrow A_0 > 2^{M+K} + 2^{K+1} - 2^{M-1} - 1$

Approximately, $A_0 > 2^{M+K}$, 2/LSB of the overall converter
Effect of finite unity gain frequency of the opamp

\[ V_{\text{in}} \] \hspace{1cm} \phi_2 \hspace{1cm} C_1 \hspace{1cm} V_x(t) \hspace{1cm} \phi_1 \hspace{1cm} C_2 \hspace{1cm} \omega_u/s \hspace{1cm} V_{\text{out}}(t) \]

- \( \phi_2 \): \( V_{\text{out}}(t) = V_x(t) = V_{\text{out}}(0) \exp(-\omega_u t) \)
- Incomplete reset
- Worst case: \( V_{\text{out}}(0) = V_{\text{ref}} \); Error smaller than \( V_{\text{ref}} / 2^{K+1} \) at the \( t = T_s / 2 \)
- \( \omega_u \geq 2 \ln(2)(K + 1)f_s \)
- \( p_2, p_3, \ldots > \omega_u \)

finite dc gain model: \( A_0 \)
first order model: \( A_0/(1+s/\omega_d) \)
integrator model: \( \omega_u/s \)
full model: \( A_0/(1+s/\omega_d)(1+s/p_2)(1+s/p_3) \ldots \)
Effect of finite unity gain frequency of the opamp

\[ \phi_1: V_{out}(t) = C_1/C_2 V_{in} \left( 1 - \exp(-\omega_u C_2/C_1 + C_2 t) \right) + V_{out}(0) \exp(-\omega_u C_2/C_1 + C_2 t) \]

Incomplete settling of amplified residue \( V_q \)

Worst case: \( C_1/C_2 V_{in} = V_{ref} \); Error smaller than \( V_{ref}/2^{K+1} \) at the \( t = T_s/2 \); \( V_{out}(0) = 0 \) after reset.

\( \omega_u/(1 + 2^{M-1}) \geq 2 \ln(2)(K + 1)f_s \) (\( \omega_u \) in rad/s, \( f_s \) in Hz)

\( \omega_u/(1 + 2^{M-1}) \) is the unity loop gain frequency assuming no parasitics

\( p_{2,3,...} > \omega_u/(1 + 2^{M-1}) \)

finite dc gain model: \( A_0 \)
first order model: \( A_0/(1+s/\omega_d) \)
integrator model: \( \omega_u/s \)
full model: \( A_0/(1+s/\omega_d)(1+s/p_2)(1+s/p_3) \)...
Depending on amplifier topology, reset and amplifying phases pose different constraints.

In our example, amplifying phase constraint is more stringent (loop gain in amplifying and reset phases are very different—better to have them close to each other).

\( \omega_u \) itself can depend on capacitive load (different for \( \phi_1, \phi_2 \)).

Higher order poles \( p_2, p_3, \ldots \) need to be placed above the unity loop gain frequency, not necessarily \( \omega_u \).
Single stage opamp-transconductor

Model of a single stage opamp

SC amplifier

- \( \phi_1 \): Capacitive load = \( C_1 \)
- \( \phi_2 \): Capacitive load = \( C_1 C_2/(C_1 + C_2) \)

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Single stage opamp-transconductor

Loop opened at opamp input

- Loop broken at the opamp input to evaluate loop gain
  - $\phi_1$
    - $V_{out}(s)/V_t(s) = \frac{g_m}{sC_1}$
    - Opamp unity gain frequency $\omega_u = \frac{g_m}{C_1}$
    - $V_f(s)/V_t(s) = \frac{g_m}{sC_1}$
    - Unity loop gain frequency $\omega_{u,\text{loop}} = \frac{g_m}{C_1}$
  - $\phi_2$
    - $V_{out}(s)/V_t(s) = \frac{g_m}{s(C_1C_2/C_1 + C_2)}$
    - Opamp unity gain frequency $\omega_u = \frac{g_m}{(C_1C_2/C_1 + C_2)}$
    - $V_f(s)/V_t(s) = \frac{g_m}{sC_1}$
    - Unity loop gain frequency $\omega_{u,\text{loop}} = \frac{g_m}{C_1}$
Multi step converters

- Two step architecture can be extended to multiple steps.
- All stages except the last have their outputs digitally corrected from the following A/D output.
- Accuracy of components in each stage depends on the accuracy of the A/D converter following it.
- Accuracy requirements less stringent down the pipeline, but optimizing every stage separately increases design effort.
- Pipelined operation to obtain high sampling rates.
- Last stage is not digitally corrected.
Multi step A/D converter

- 4,4,4,3 bits for an effective resolution of 12 bits
- 3 effective bits per stage

**Equation:**
\[ D_N = 2^{K-1}C_N + D_{N-1} \]
K: cumulative number of bits after Nth stage

**Diagram:**
- Analog path: Quantizer and residue generator
- Digital path: Digital correction

**Notations:**
- \( V_{in} \) and \( V_{out} \)
- \( C_N \) bits
- \( D_N \) bits
- \( S/H \) sample and hold
- \( A/D \) analog to digital converter
- \( D/A \) digital to analog converter
- \( V_q \) output voltage
- \( 8V_q \) output voltage
- \( V_{ref} \) reference voltage

**Key Points:**
- 12 bit A/D
- 9 bit A/D
- 6 bit A/D
- 3 bit A/D

**Diagram Details:**
- V1, V2, V3, V4
- D1, D2, D3, D4
- Residue generation at each stage

**Additional Information:**
- Pipelined multi step A/D converters
- 4 effective bits per stage
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Multi step converter-tradeoffs

- Large number of stages, fewer bits per stage
  - Fewer comparators, low accuracy-lower power consumption
  - Larger number of amplifiers-power consumption increases
  - Larger latency
- Fewer stages, more bits per stage
  - More comparators, higher accuracy designs
  - Smaller number of amplifiers-lower power consumption
  - Smaller latency
- Typically 3-4 bits per stage easy to design