

EE658: VLSI Data Conversion Circuits; HW6

Nagendra Krishnapura (nagendra@iitm.ac.in)

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Submit all solutions by email as a single pdf file; 0.18 μm technology parameters: $V_{Tn} = 0.5\text{ V}$; $V_{Tp} = 0.5\text{ V}$; $K_n = 300\ \mu\text{A}/\text{V}^2$; $K_p = 50\ \mu\text{A}/\text{V}^2$; $A_{VT} = 3.5\text{ mV}/\mu\text{m}$; $A_\beta = 1\%\ \mu\text{m}$; $V_{dd} = 1.8\text{ V}$; $L_{min} = 0.18\ \mu\text{m}$, $W_{min} = 0.24\ \mu\text{m}$;

1. Fig. 1 shows a two step flash converter with error correction. The overall resolution is $N = M + K - 1$ bits. The error in each block is shown as an analog voltage referred to either the input or the output. i.e. The m^{th} transition of A/D1 occurs at $mV_{LSB1} + V_{e,A/D1}[m]$ and the m^{th} output of D/A is $mV_{LSB1} + V_{e,D/A}[m]$. $0 \leq m \leq 2^M - 1$ and $0 \leq k \leq 2^K - 1$. $V_{LSB} = V_{ref}/2^N$ is the LSB voltage of the overall converter.
 - (a) Derive the value of the input V_{in} which corresponds to m^{th} transition of A/D1. You should get an expression that combines the errors from different components.
 - (b) Derive the value of the input V_{in} which corresponds to k^{th} transition of A/D2. Assume that A/D1 is between m^{th} and $(m + 1)^{\text{th}}$ transitions.
 - (c) In the result from (a) above, assume that the different terms contribute equally to the total error, which is constrained to $0.5V_{LSB}$. Calculate the individual errors in terms of V_{ref} .
 - (d) Calculate the allowable errors in each component for a 8 bit converter, for $M = 5$, $K = 4$ and $M = 4$, $K = 5$. Express the accuracy as an effective number of bits (A component with a voltage range V_{ref} has an L bit accuracy if its error magnitude is less than $V_{ref}/2^{L+1}$, i.e. half LSB at L bits).
2. Assume that you have a 2 step flash A/D converter (no digital error correction) with 2 bits in each stage. All components other than the residue amplifier are ideal. Plot INL and DNL for the following cases. Compare it with the ideal characteristics.
 - (a) (2 pts.) The amplifier has a gain $G > 4$
 - (b) (2 pts.) The amplifier has a gain $G < 4$
 - (c) (2 pts.) The amplifier has an input referred offset $V_{os} > 0$
 - (d) (2 pts.) The amplifier has an input referred offset $V_{os} < 0$
3. Four alternative architectures for a 12 bit 100 MS/s A/D converters are shown in Fig. 2(a-d). The interstage amplifiers use the topology in Fig. 2(e). They use a single stage opamp, shown in Fig. 2. For each architecture, calculate the following and tabulate the results. V_{ref} is 1 V for all stages.
 - (a) Interstage gains required.

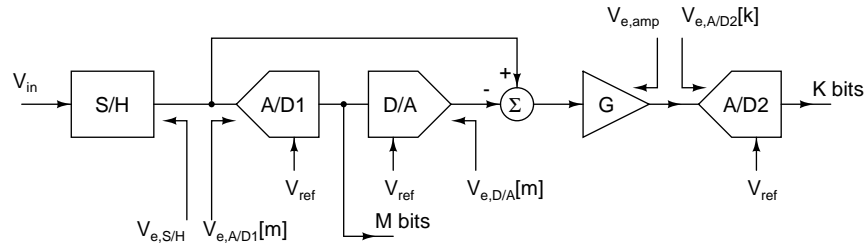


Figure 1:

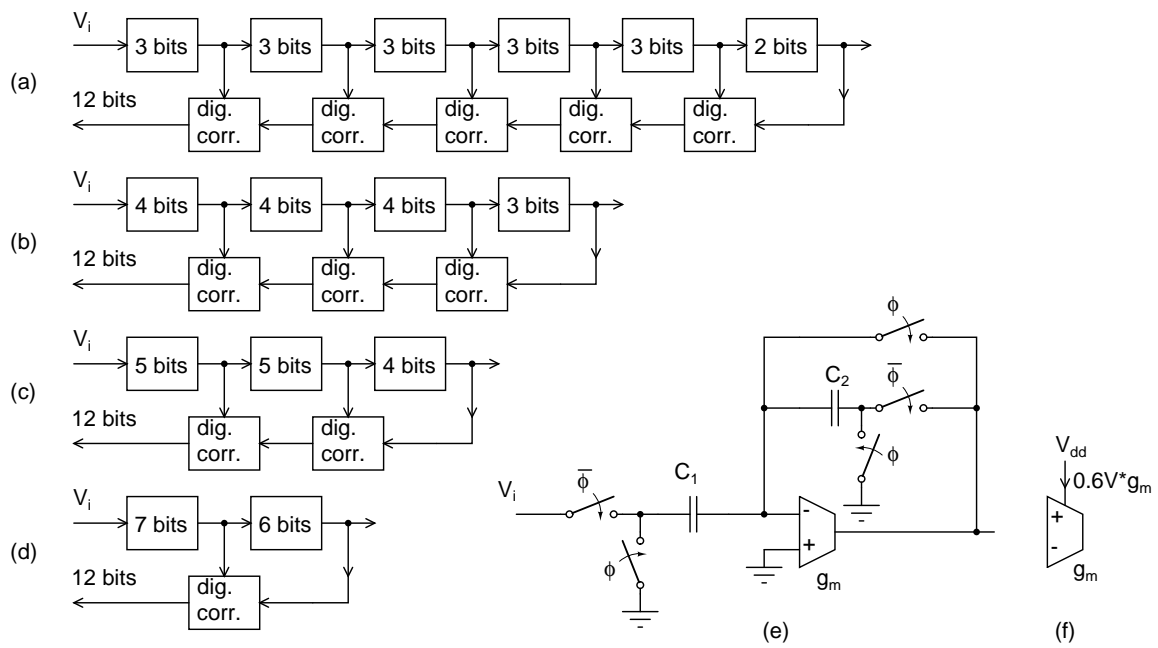


Figure 2:

- (b) Capacitance values in each stage. Assume that the input referred noise of the amplifier is $2kT/C_1$ and that the rms noise needs to be lower than 0.1 LSB of the following stages. The minimum realizable capacitance is 100 fF.
- (c) DC gain required in each opamp.
- (d) Unity gain frequency ω_u of each opamp, and corresponding g_m (assuming a first order opamp). Consider only the amplification phase.
- (e) Unity gain frequency $\omega_{u,loop}$ of each amplifier. This will determine the minimum value for the second pole of the opamp.
- (f) Total number of comparators for each architecture.
- (g) Total current consumption in the opamps. Assume that the current required to realize a transconductor g_m is $(g_m \times 0.6 \text{ V})$. (Fig. 2(f))
- (h) Total power consumption in the comparators. Comparators in each ADC are designed according to the following constraints
- The comparator offset σ_{off} is $2\sigma_{VT}$ of the transistor.
 - The σ_{off} is required to be 0.1 LSB of that particular stage.

If a comparator with minimum size transistors consumes $0.6 \mu\text{A}$, compute the current consumption in each stage for all the architectures.

- (i) Total current consumption of the ADC.
- (j) Latency-Assume that each pipelined stage takes one clock cycle and each digital correction takes one clock cycle.

Compare the architecture on the following grounds-Total power consumption, power consumption in the opamps, total capacitance, highest unity loop gain frequency $\omega_{u,loop}$ to be realized, number of comparators.

This problem is designed to give you a feel for the tradeoffs. Since each error source is considered in isolation, and some error sources such as the second pole of the opamp are omitted entirely, the current consumption in a real 12 bit converter will be higher. However, the comparative numbers provide a realistic idea of the tradeoffs involved.

4. The circuit in Fig. 3(b) is used for the DAC and residue amplifier in the pipelined A/D converter of Fig. 3(a). The first stage has 2 bits. Complete the design of the residue amplifier and simulate it with the input waveform shown. The sampling rate is 100 MHz. For the A/D outputs $b_{1,0}$, you can assume ideal waveforms corresponding to V_{in} .

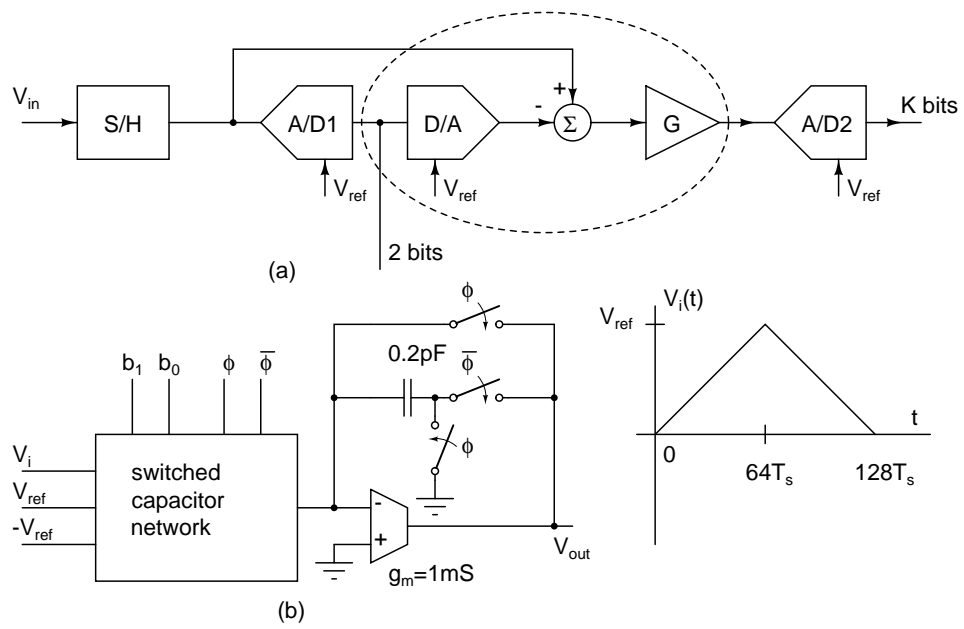


Figure 3: