# EE658: VLSI Data Conversion Circuits; HW2

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1. A/D nonlinearity: The output code density of an A/D converter to a low frequency full scale sine wave is given in `a2dcodes.dat`. How many bits does the A/D converter have? Analyze the code density to obtain its INL and DNL. Simulate this A/D converter with a full scale sinewave near half the sampling rate. Compute SFDR, SNDR, and SNR. What is the ENOB of this converter? What is the maximum jitter that can be tolerated so that the SNR due to jitter is 3dB more than the SNDR computed above?