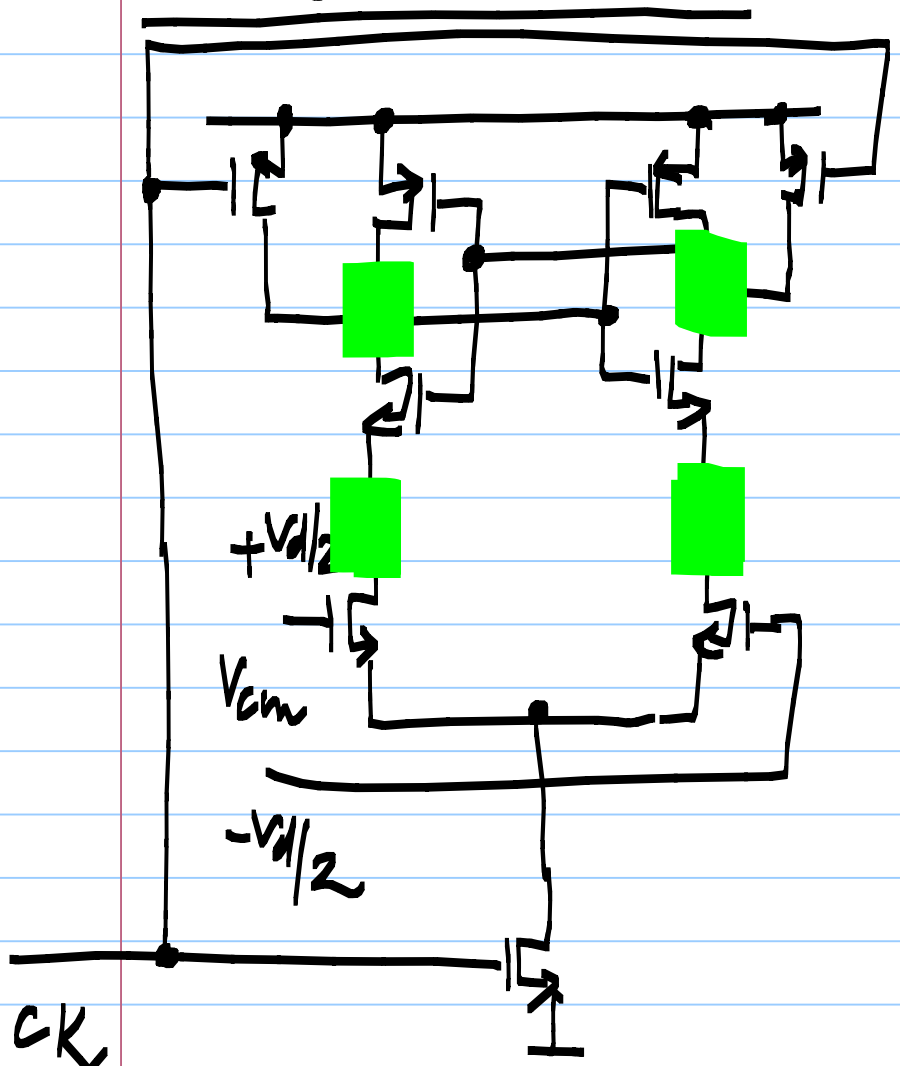
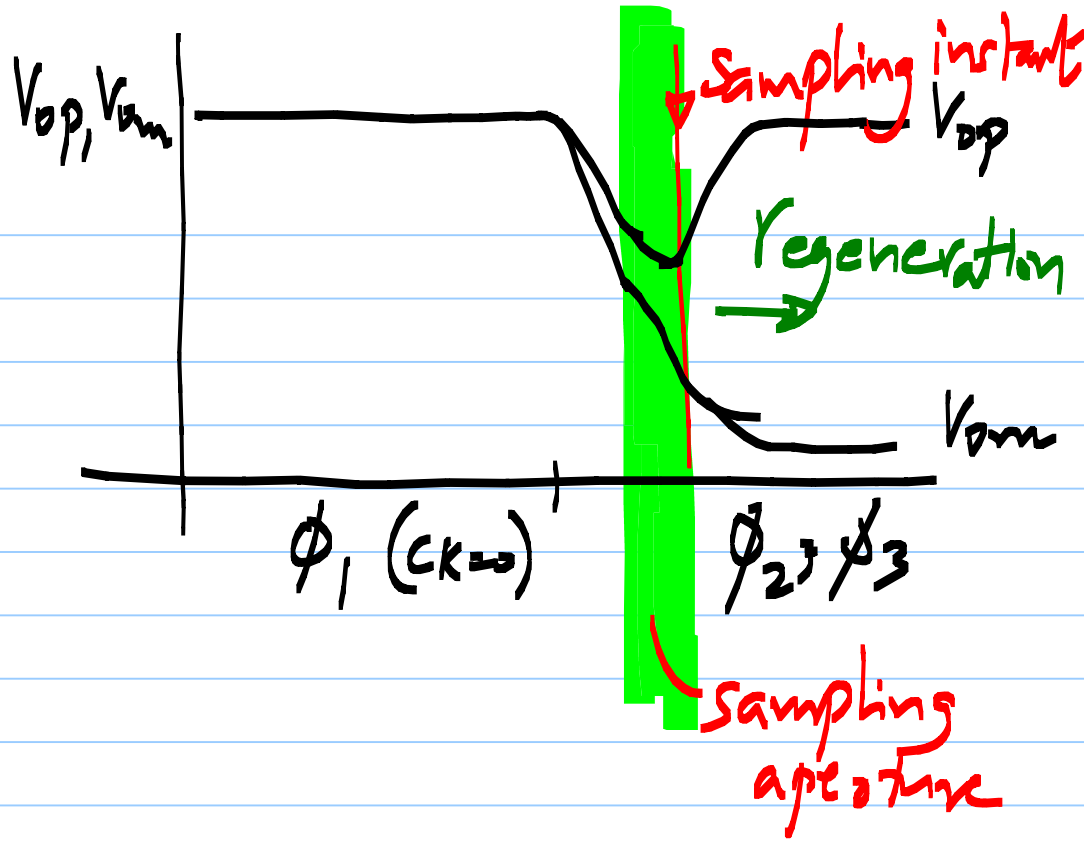
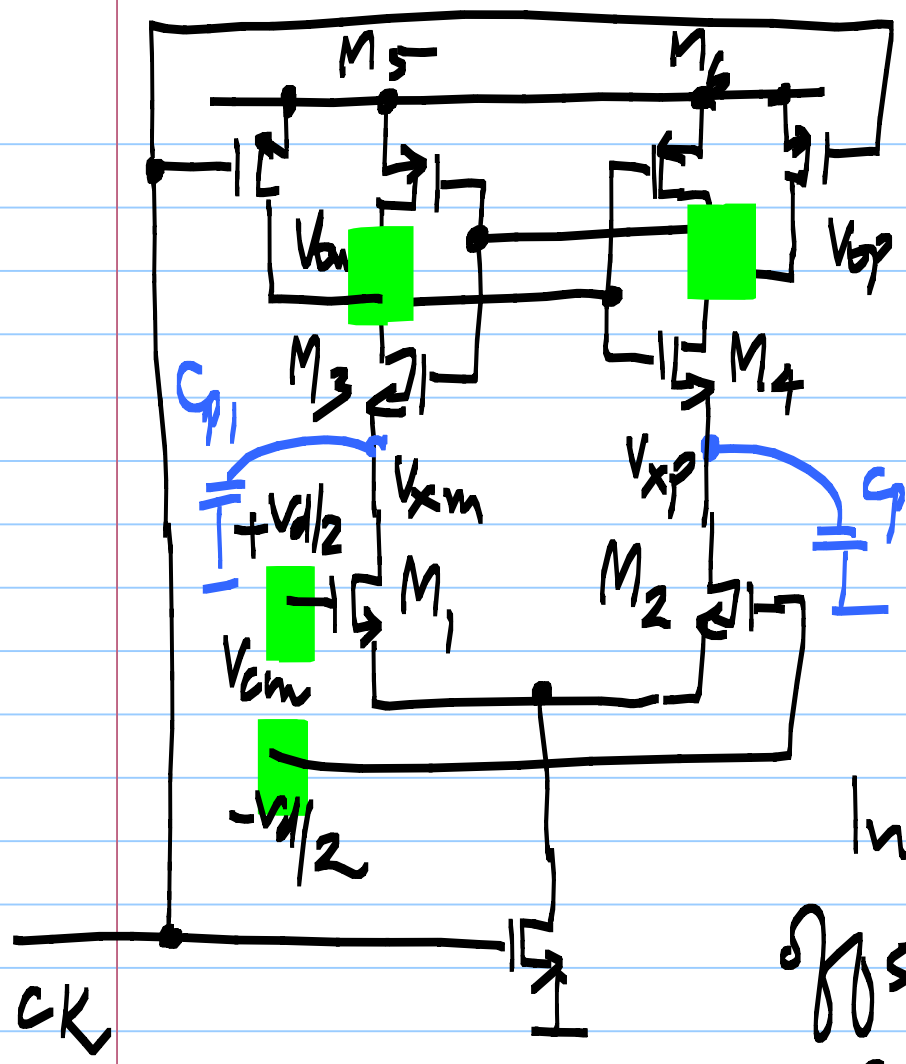
Strongarm latch



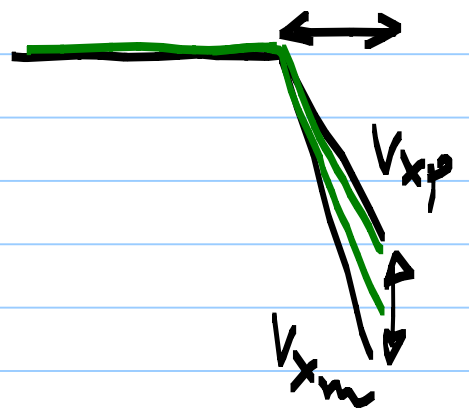


Minimize parasitic capacitances on the latch nodes



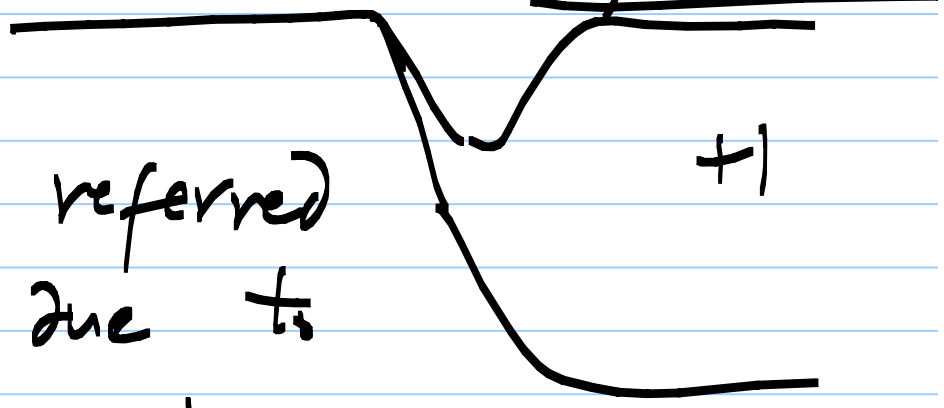
$C_{p1} \neq C_{p2}$

$C_{p1} < C_{p2}$

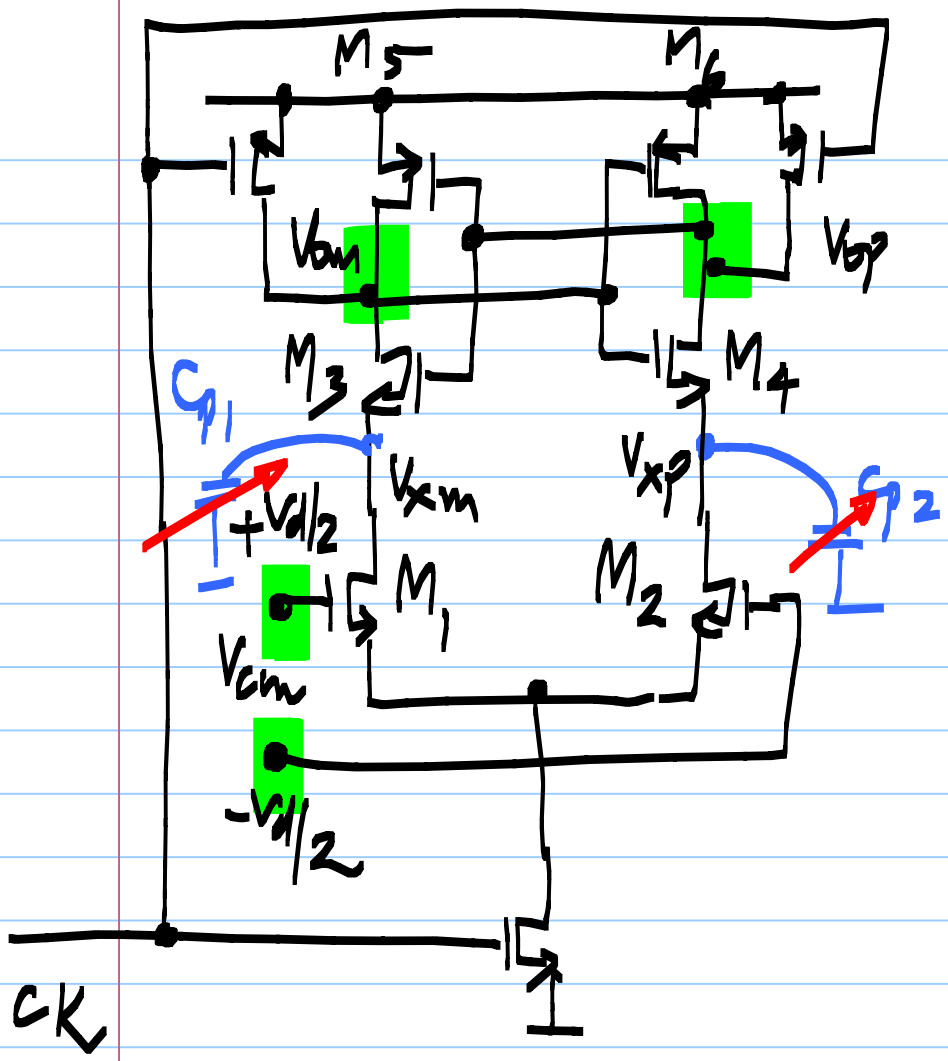


Dynamic offset

Large cM swing + Cp mismatch



Input referred offset due to Cp mismatch



Dynamic offset due to CM swing + C_p mismatch

Static offset due to mismatch between transistors

Use variable C_{p1}, C_{p2} to perform offset correction

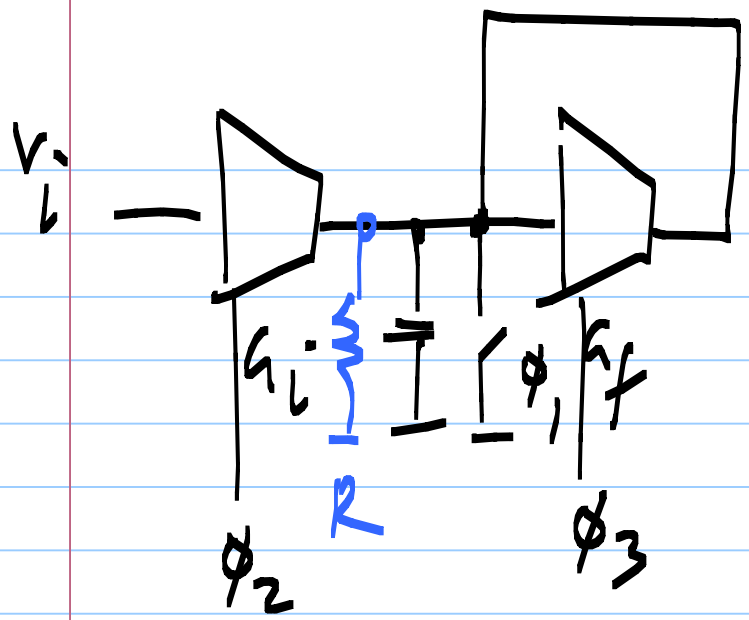
→ lower latch gain!

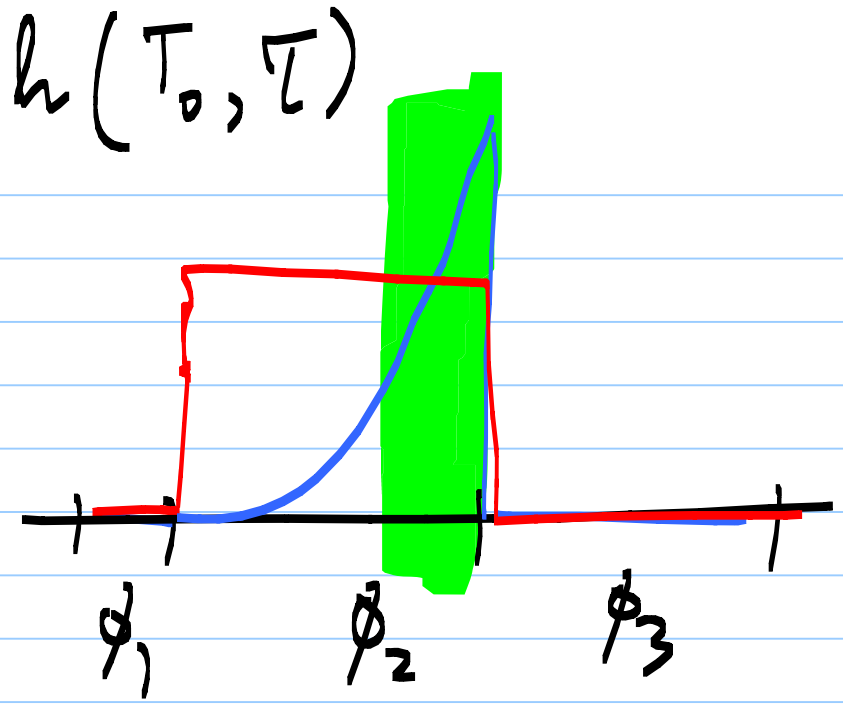
Edge triggered FF

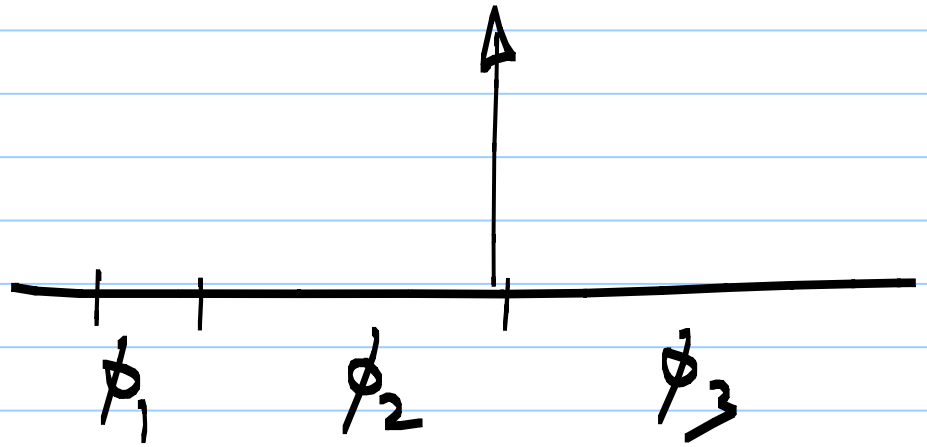
StrongArm latch: (+ RS latch) = DFF

- Single clock phase
- Small aperture time (high BW)

- Decision slicer in the Rx
- FFs in CDR, Deserializer
- FFs in Tx equalizer, Serializer

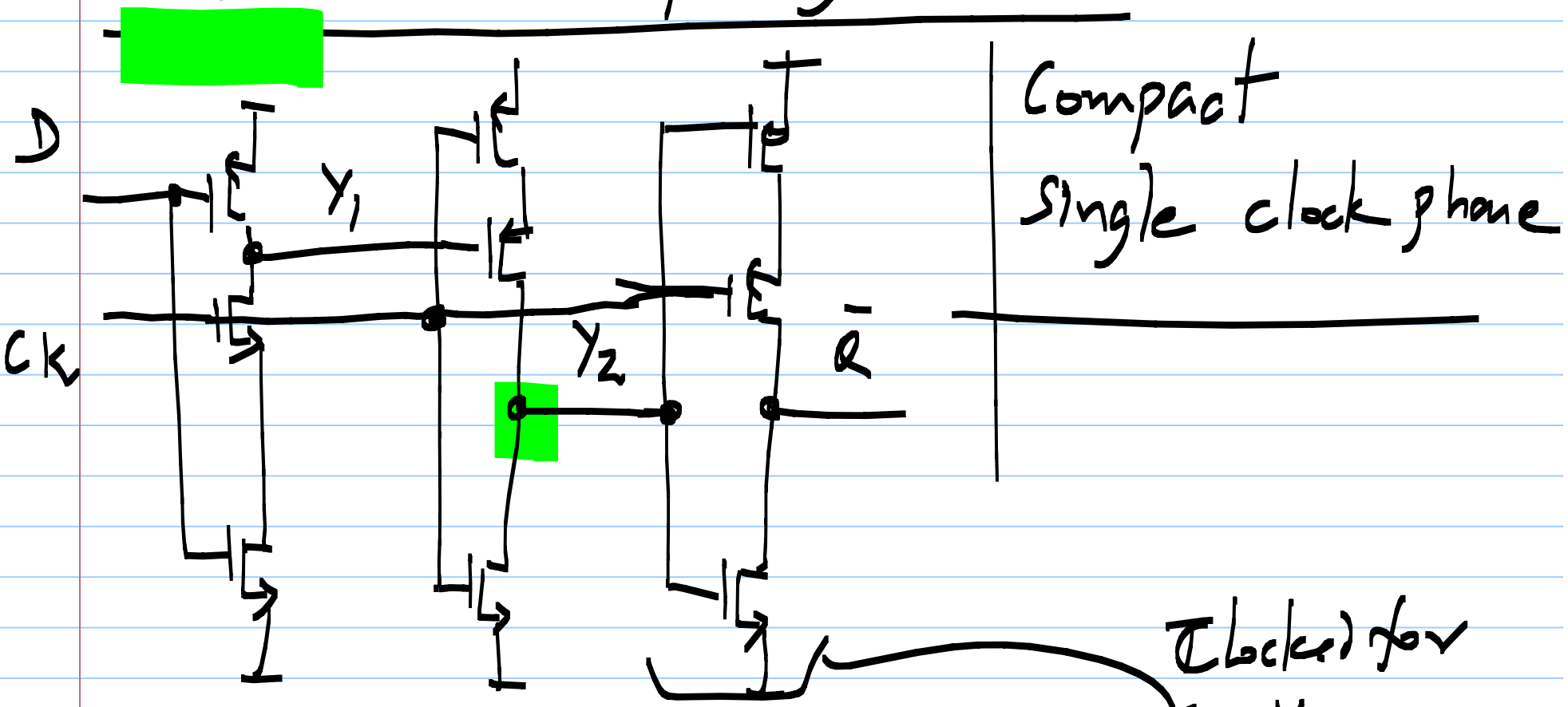

V_i
C_i
R
ϕ_1
C_f
ϕ_2
ϕ_3

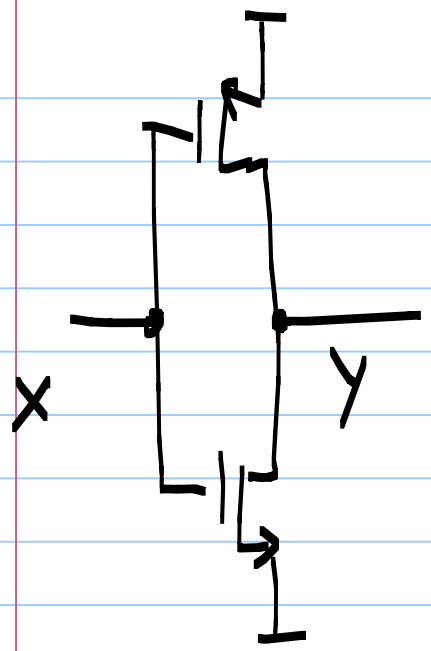

$h(T_0, \tau)$
ϕ_1
ϕ_2
ϕ_3


ϕ_1
ϕ_2
ϕ_3

* Conventional CMOS circuits at lower rates
* True-single-phase clocked Flip Flop (TSPC)
  - Dynamic FF - single clock phase
    (No regeneration)
    - charge held on some nodes
    - Lower frequency limit

Tspc FF (frequency dividers)

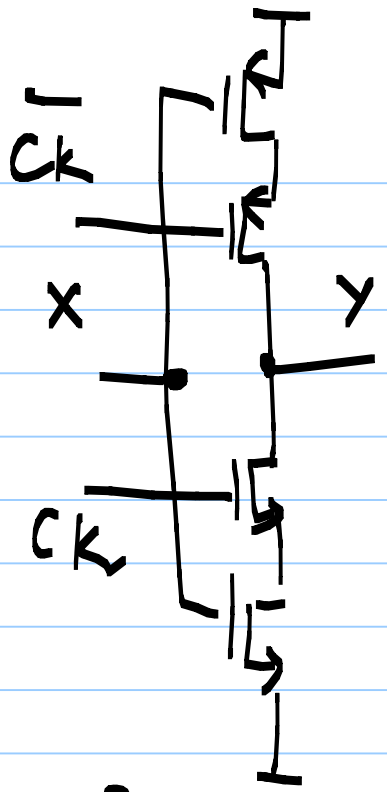




CMOS

Inverter

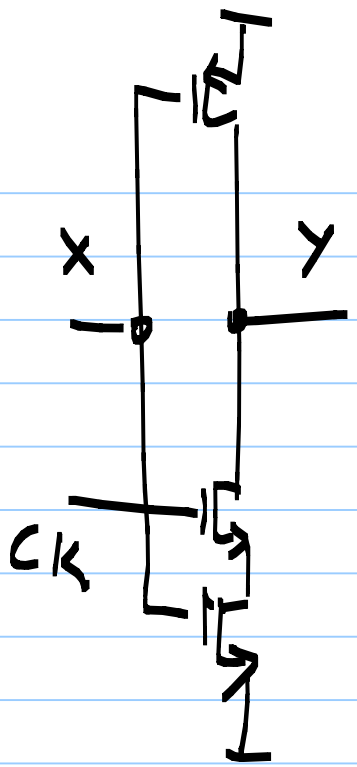
$Y = \bar{X}$



C^2MOS

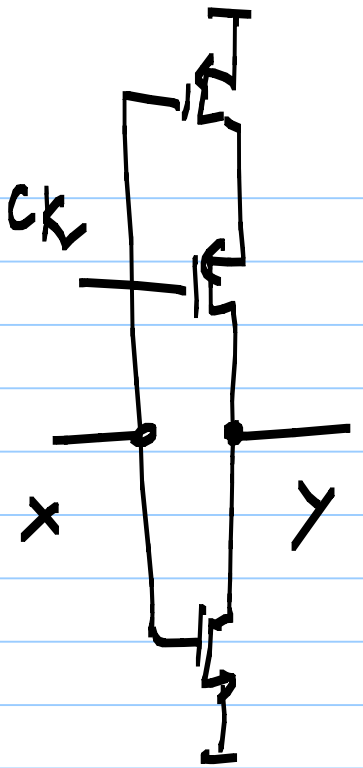
$Y = \bar{X}$ if;

ck = 1



clocked

for x = 1

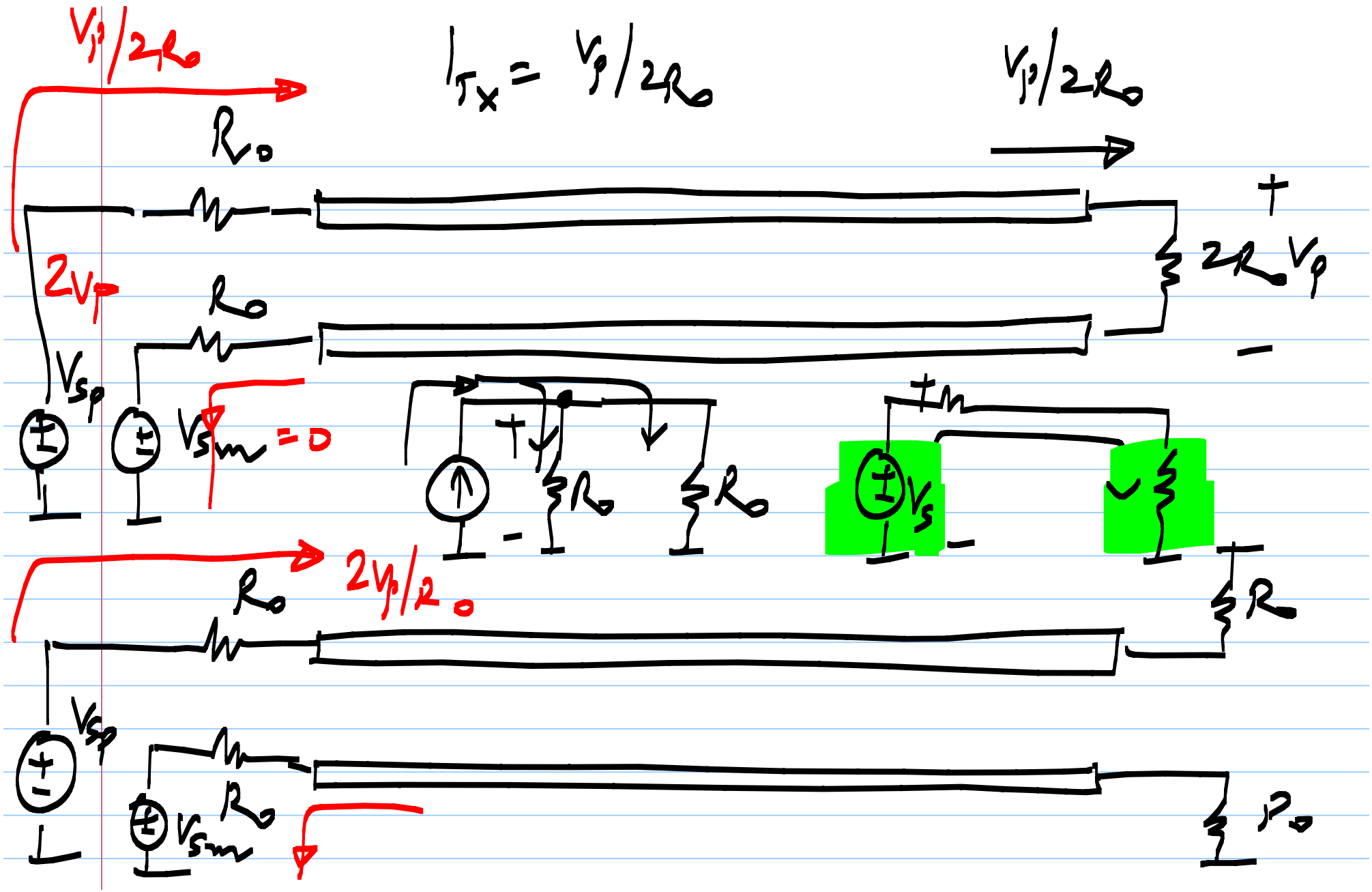


clocked for

x = 0

Current-mode drivers

Transmit drivers:


$V_p/2R_0$
$I_{TX} = V_p/2R_0$
$V_p/2R_0$
R_0
$2V_p$
$2R_0$
V_p
V_{sp}
$V_{sm} = 0$
R_0
R_0
V_s
$2V_p/2R_0$
R
V_{sp}
V_{sm}
R_0
R_0

Transmit Drivers:

* Differential termination is more efficient (less transmitter current)
* Voltage mode transmitter is more efficient

Same transmitter supply voltage in both cases