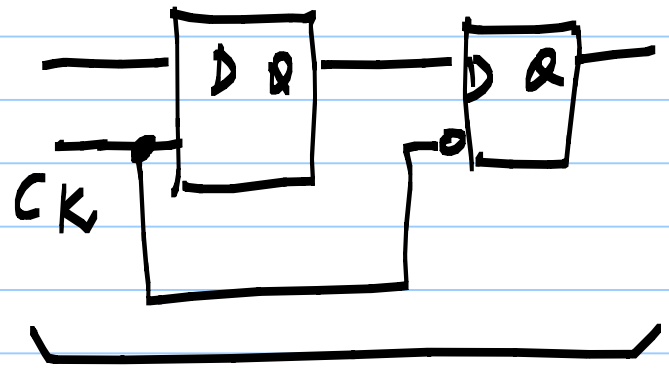
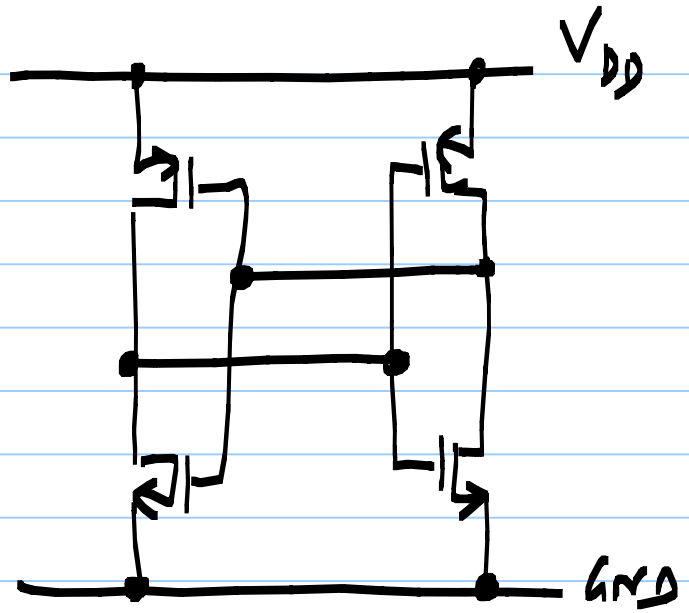
CML latch :- 2 latches for master-slave FF

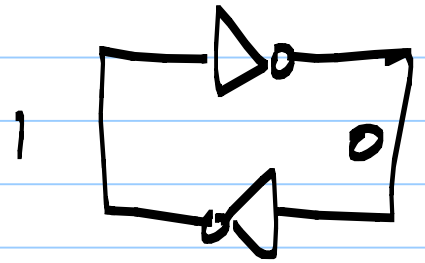


Master-slave FF

* High speed
* static power dissipation
* Hard to accommodate transistors in a low supply voltage.

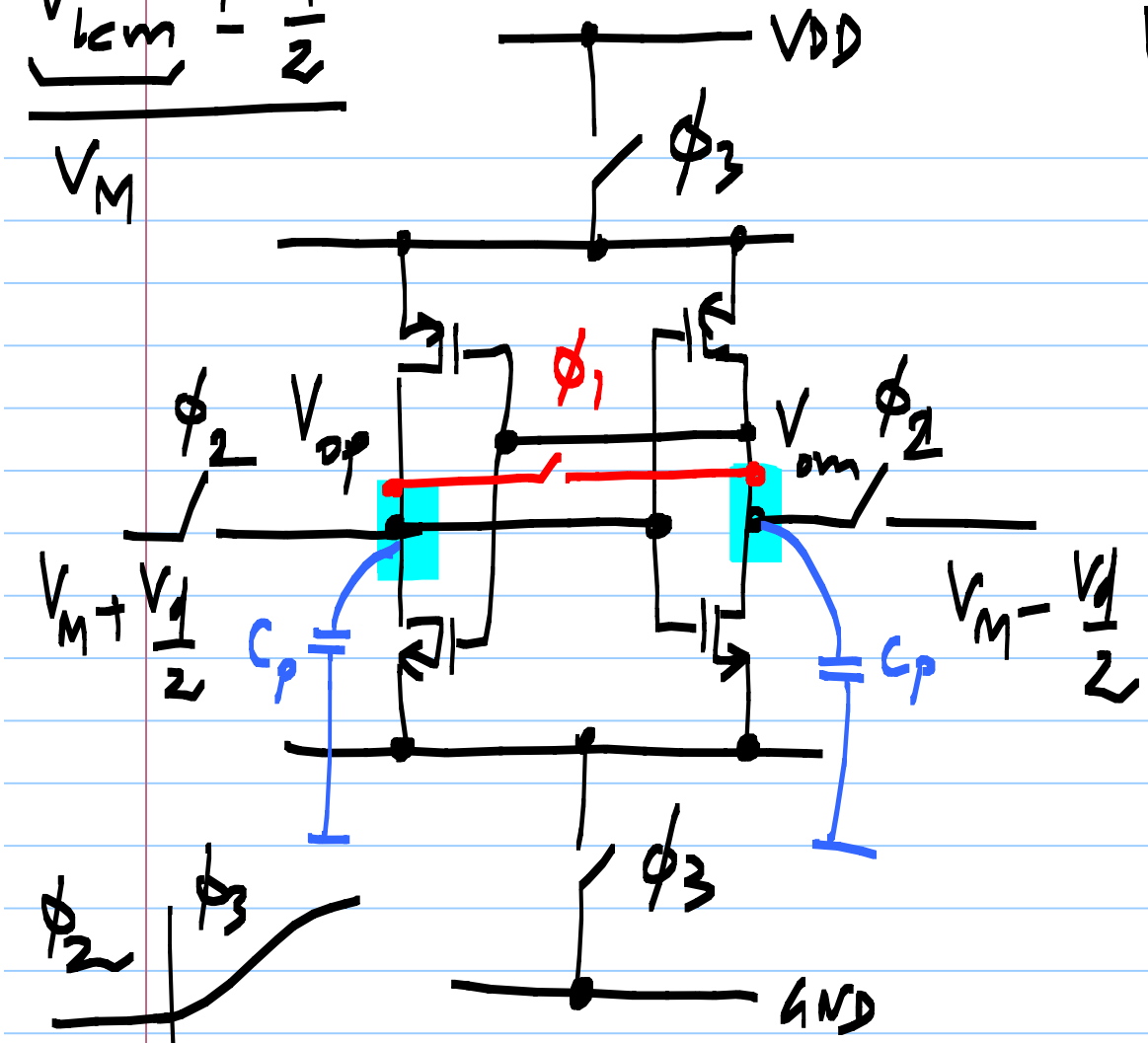
Cross-coupled inverters

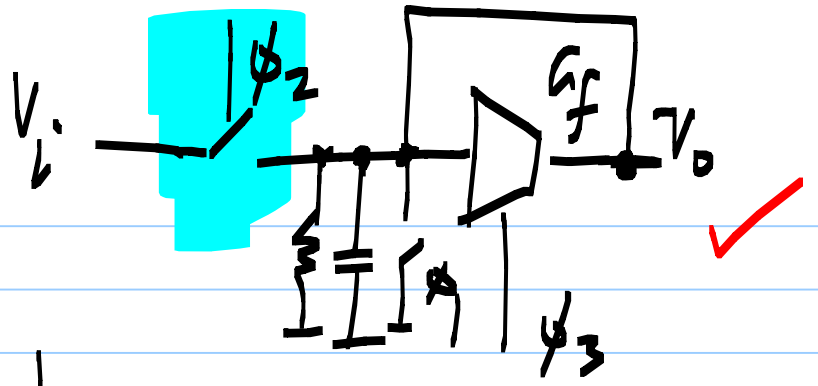




$V_{icm} \pm \frac{V_d}{2}$

V_M

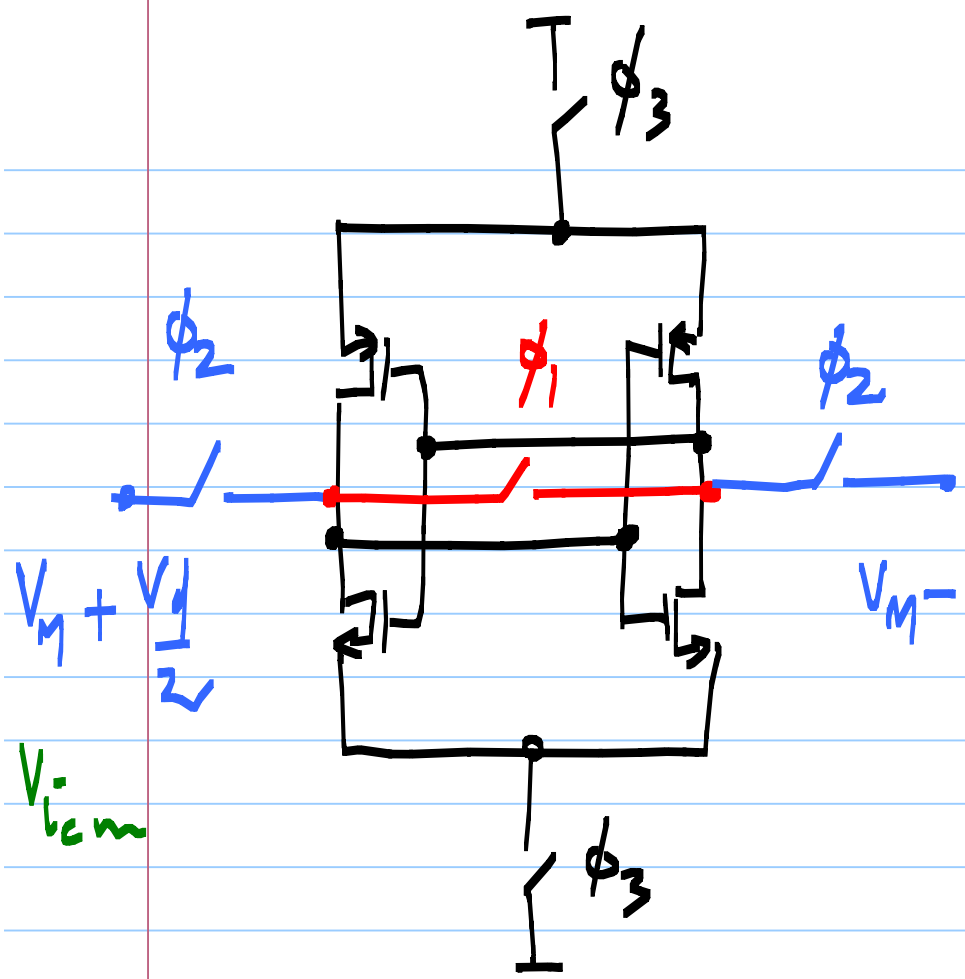


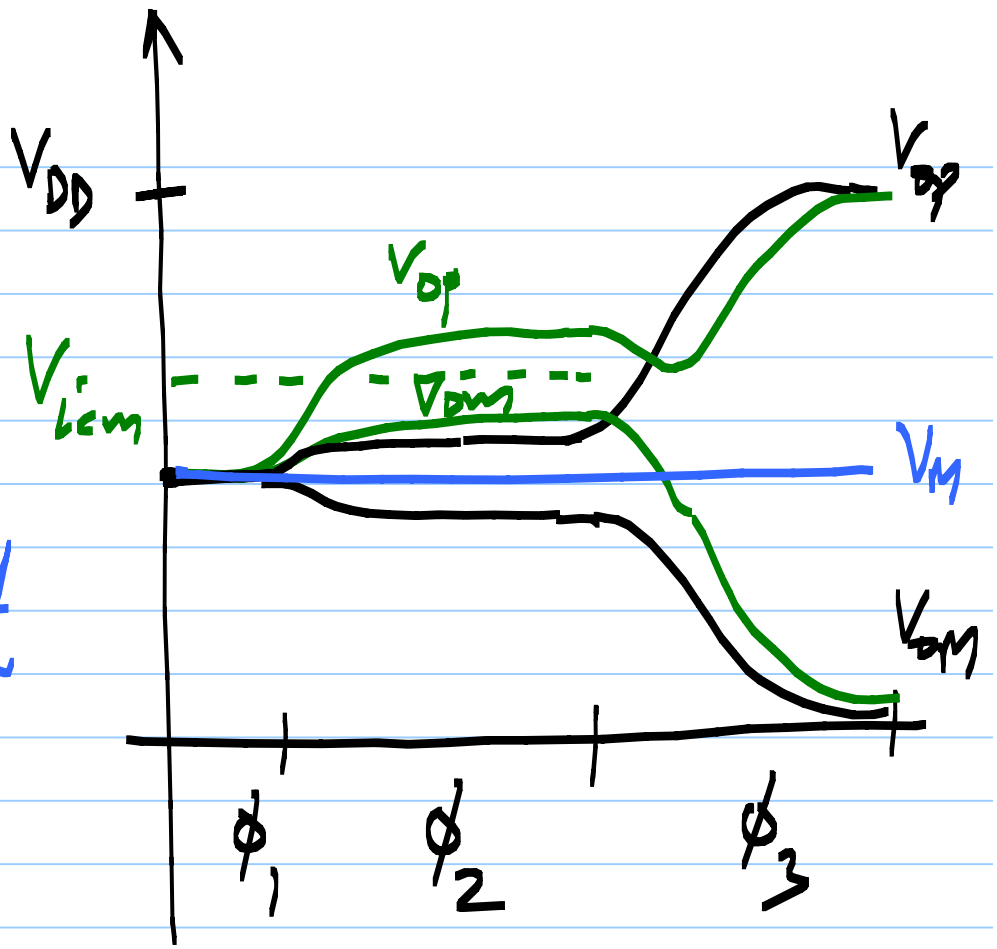


✓

Cross coupled latch enabled in ϕ_3

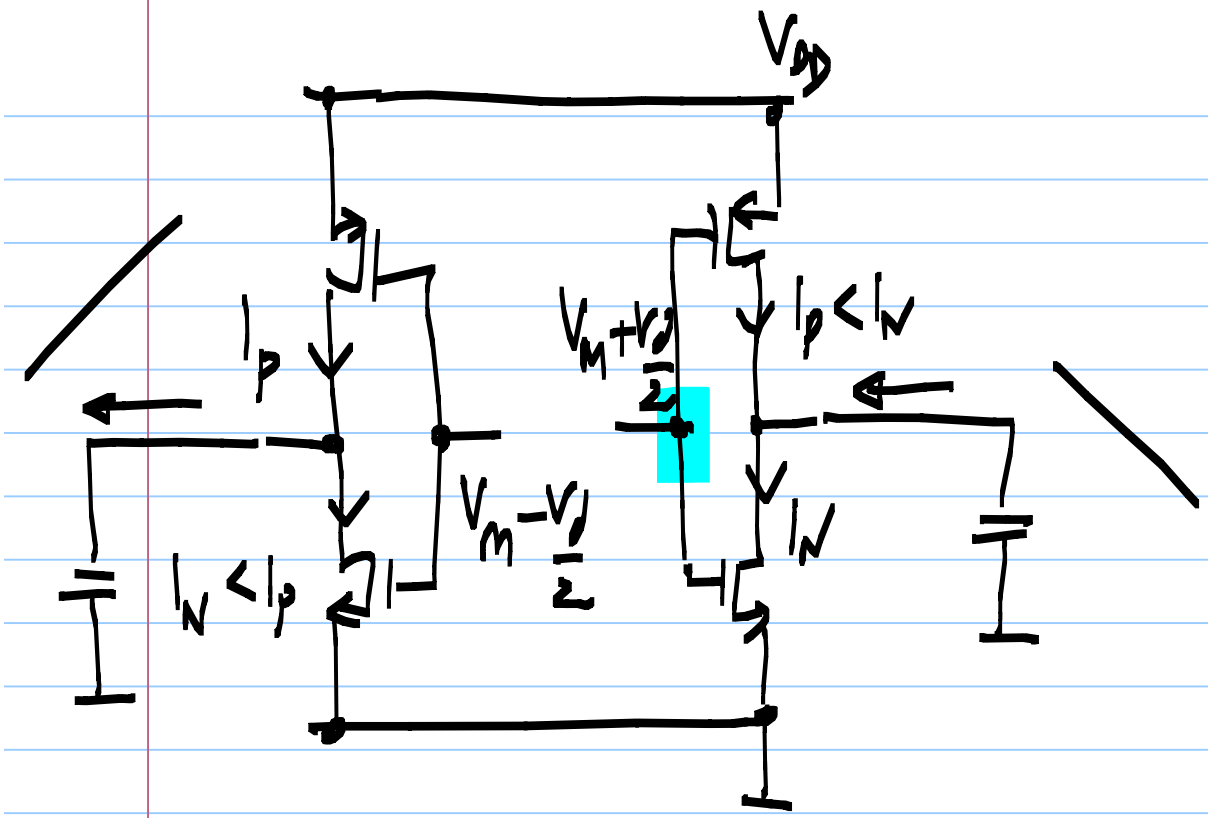
ϕ_2: Sample the inputs



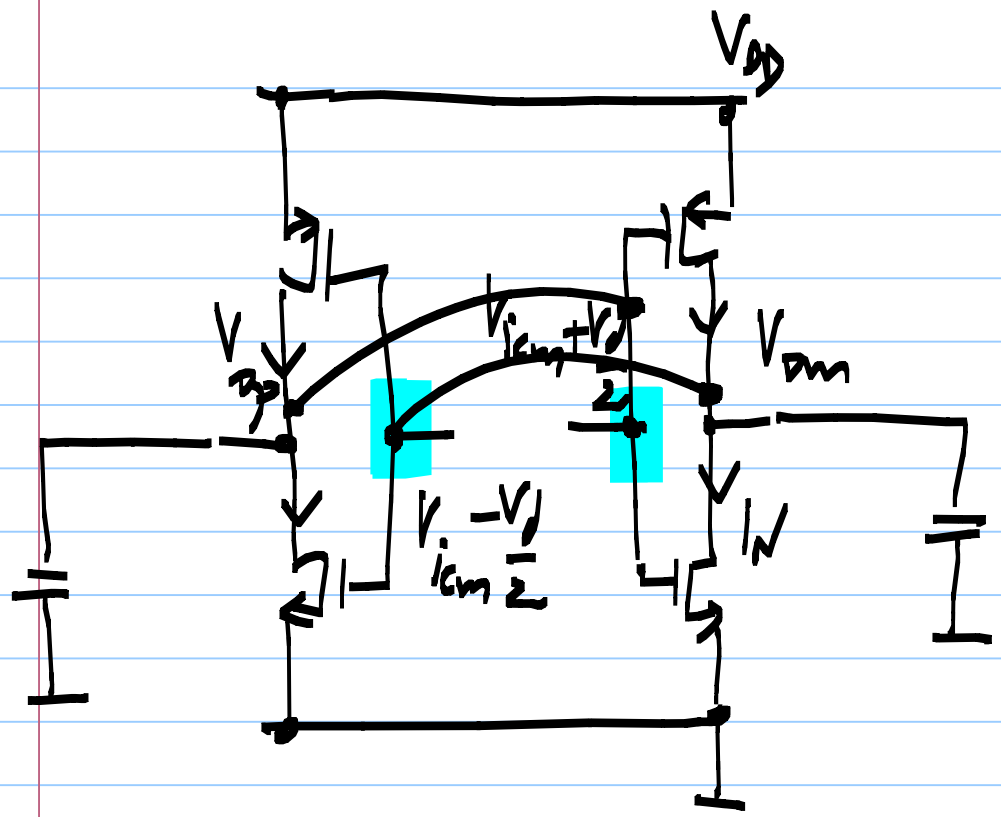


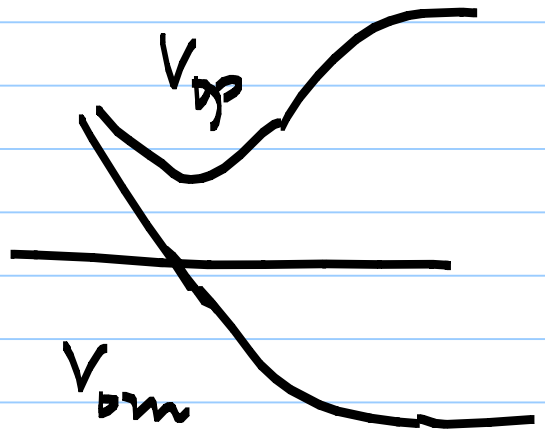
Common mode swing if

$V_{icm} \neq V_M$

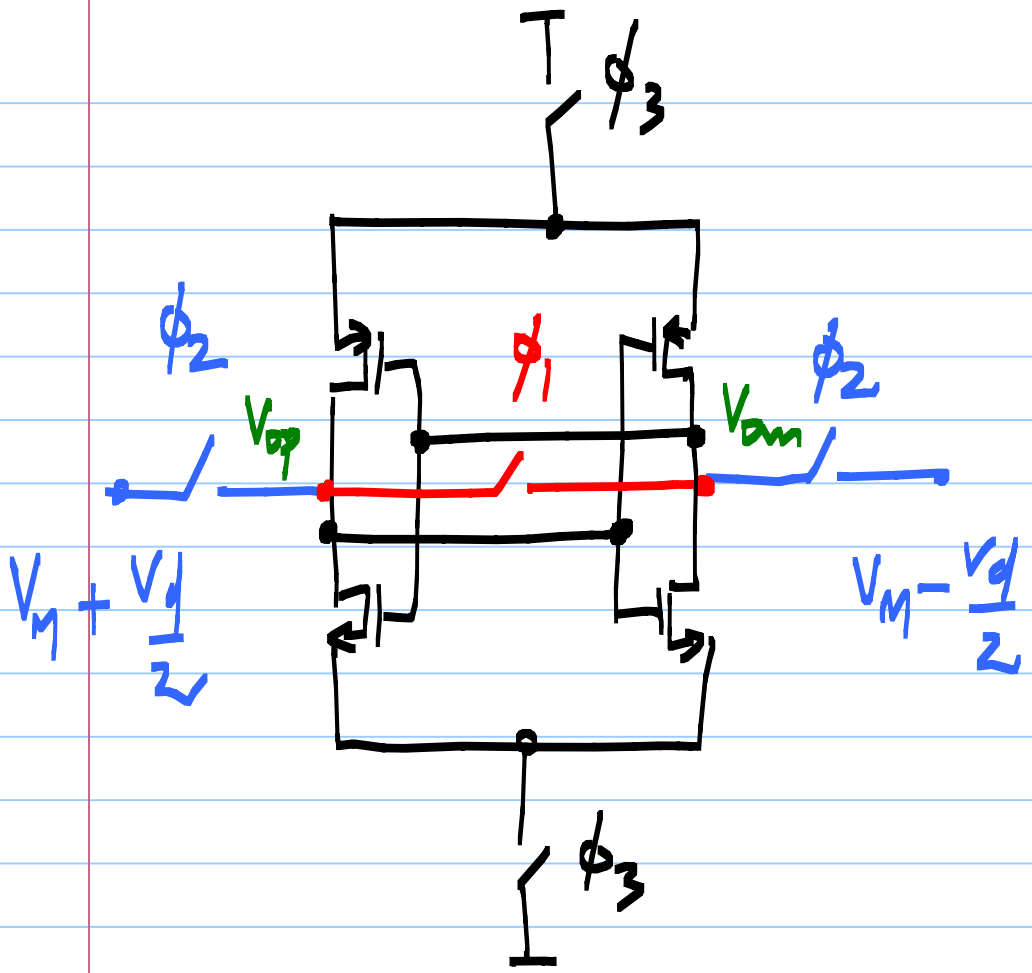

V_{DD}
I_p
$V_M + \frac{V_d}{2}$
$I_p < I_N$
$V_M - \frac{V_d}{2}$
I_N
$I_N < I_p$

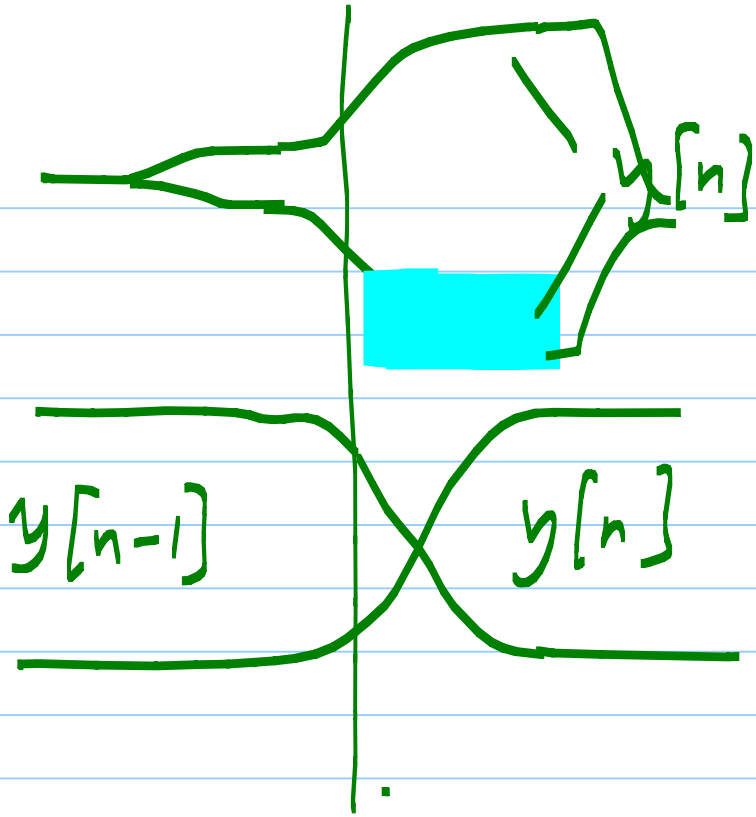
$|V_N| > |V_p|$ for both inverters

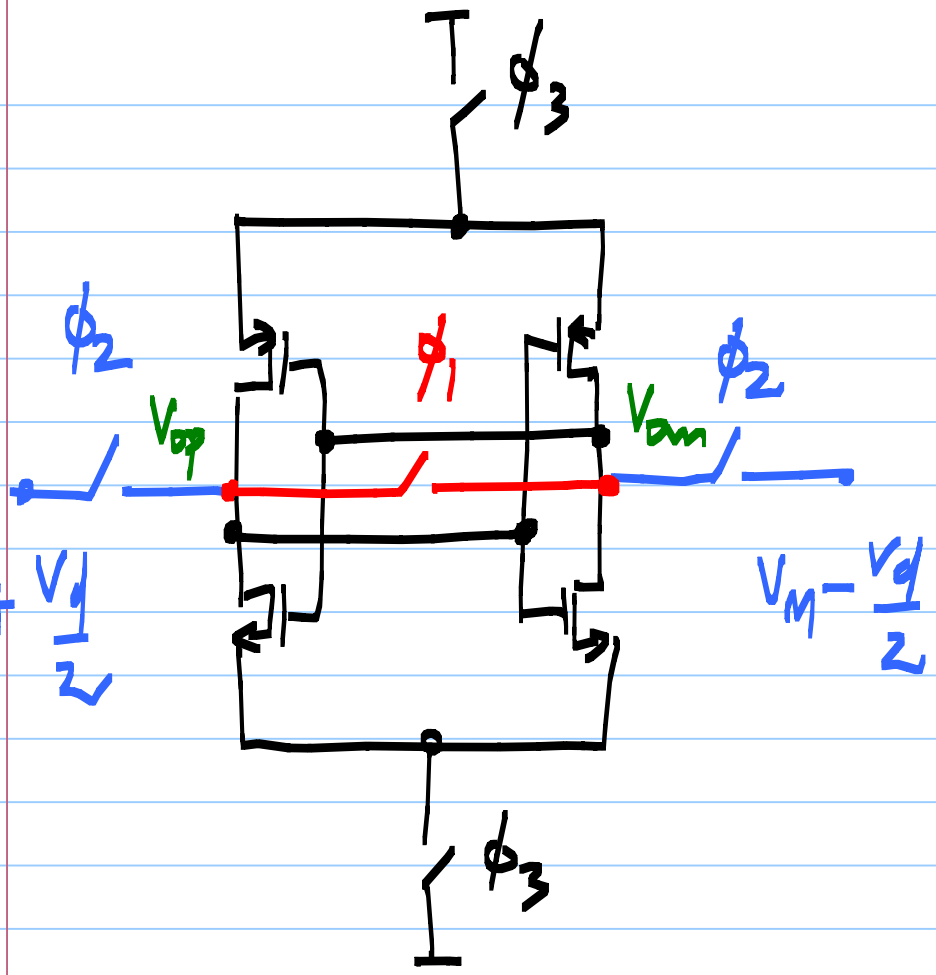


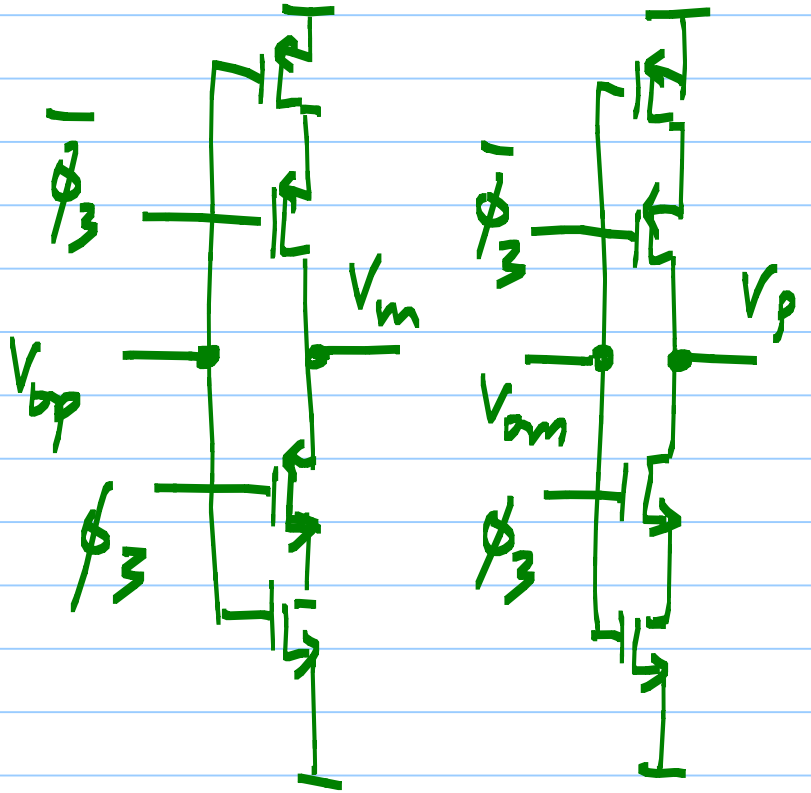


$V_{icm} > V_M$

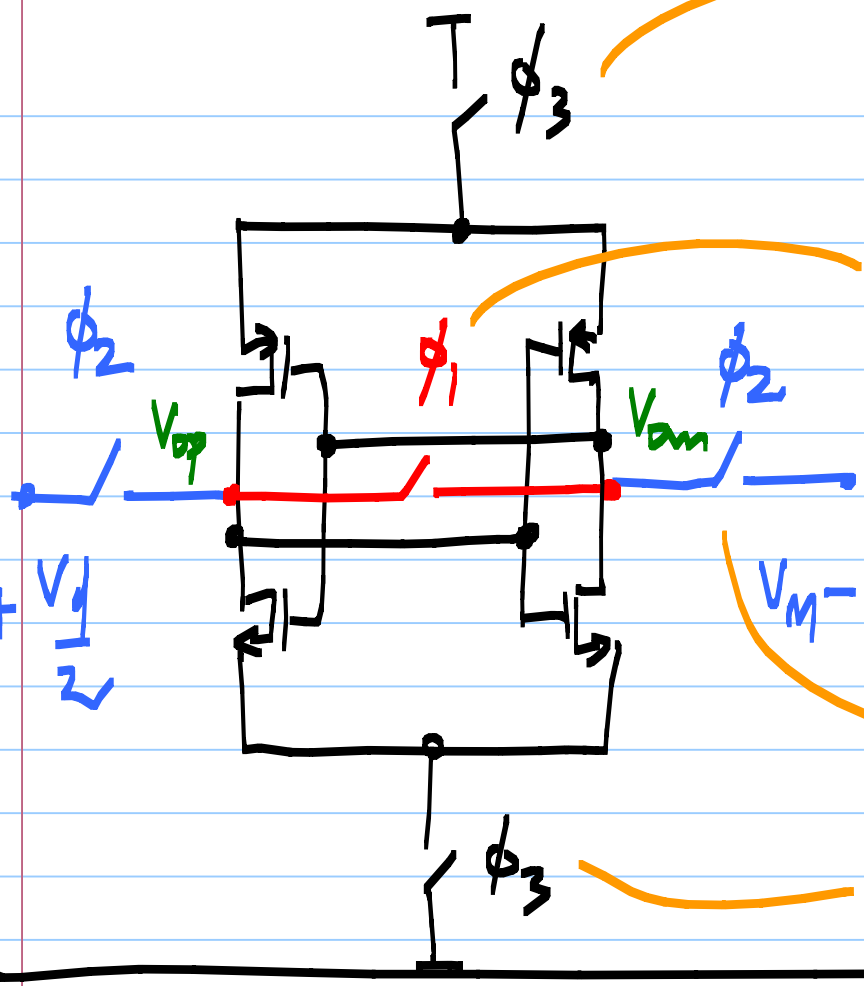

T
ϕ_3
ϕ_2
ϕ_1
ϕ_2
V_{op}
V_{on}
$V_M + \frac{V_d}{2}$
$V_M - \frac{V_d}{2}$
ϕ_3


y[n]
y[n-1]
y[n]





C^2MOS buffer



pMOS ($\bar{\phi}_3$)

nMOS (ϕ_1) + pMOS ($\bar{\phi}_1$)

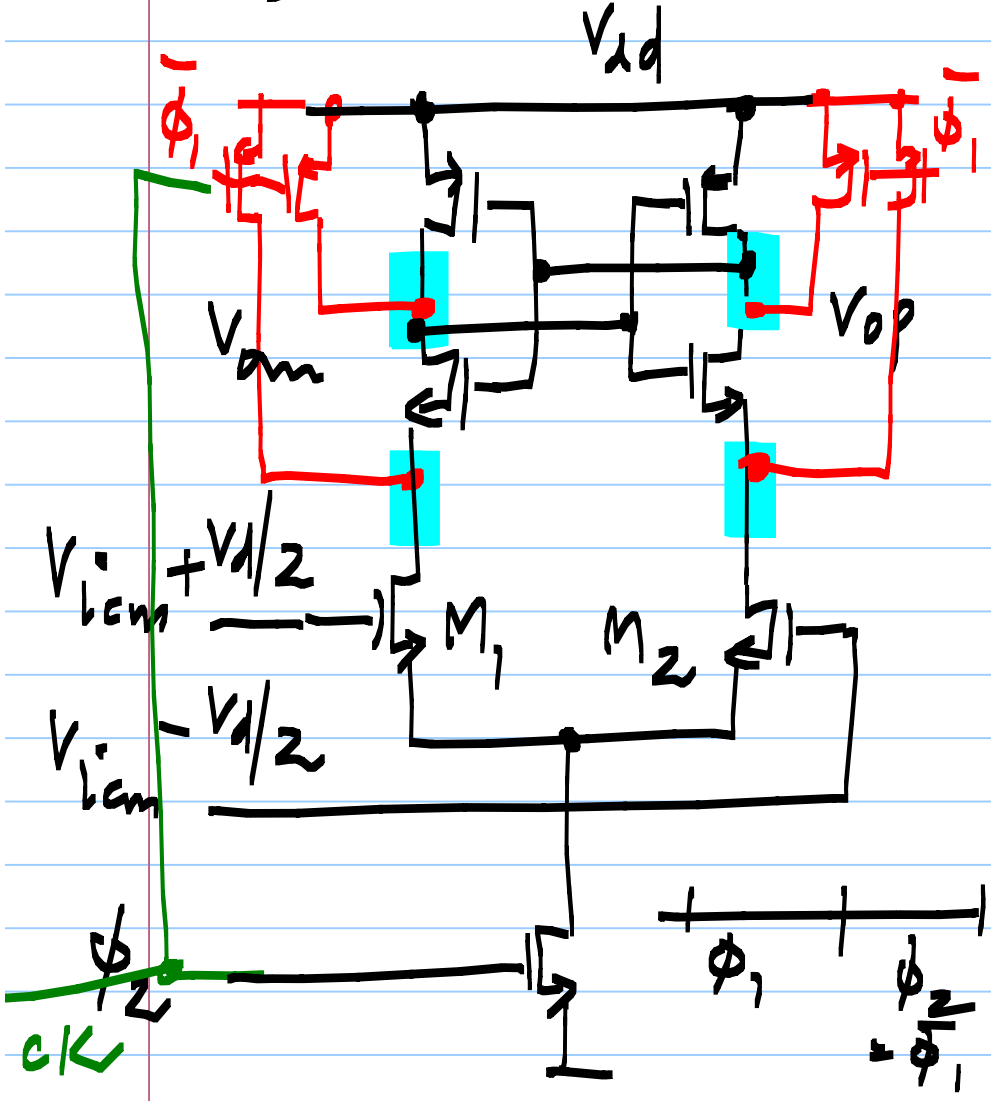
Use only one if possible

nMOS (ϕ_2) + pMOS ($\bar{\phi}_2$)

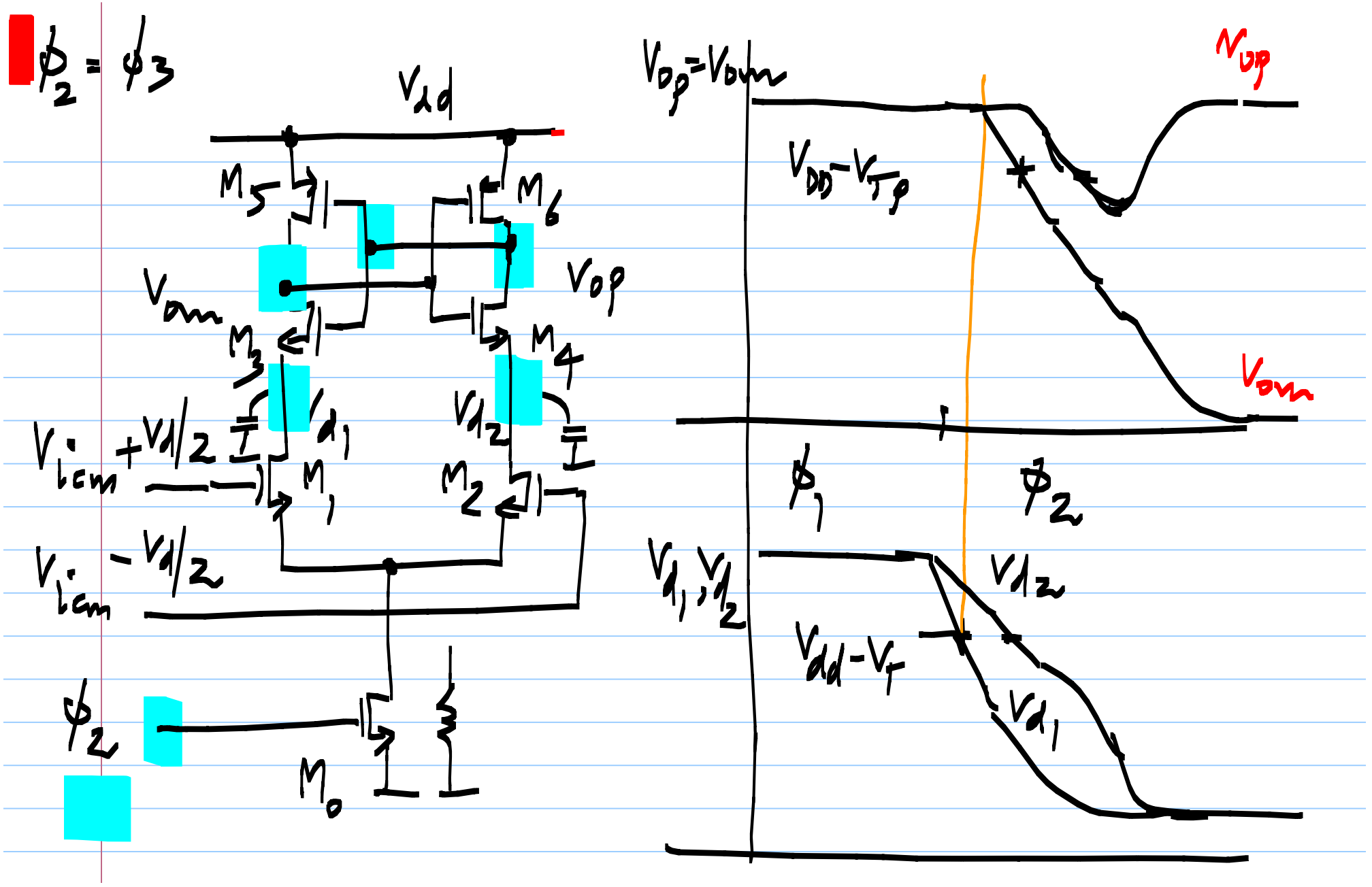
nMOS (ϕ_3)

Too many clock phases — too messy

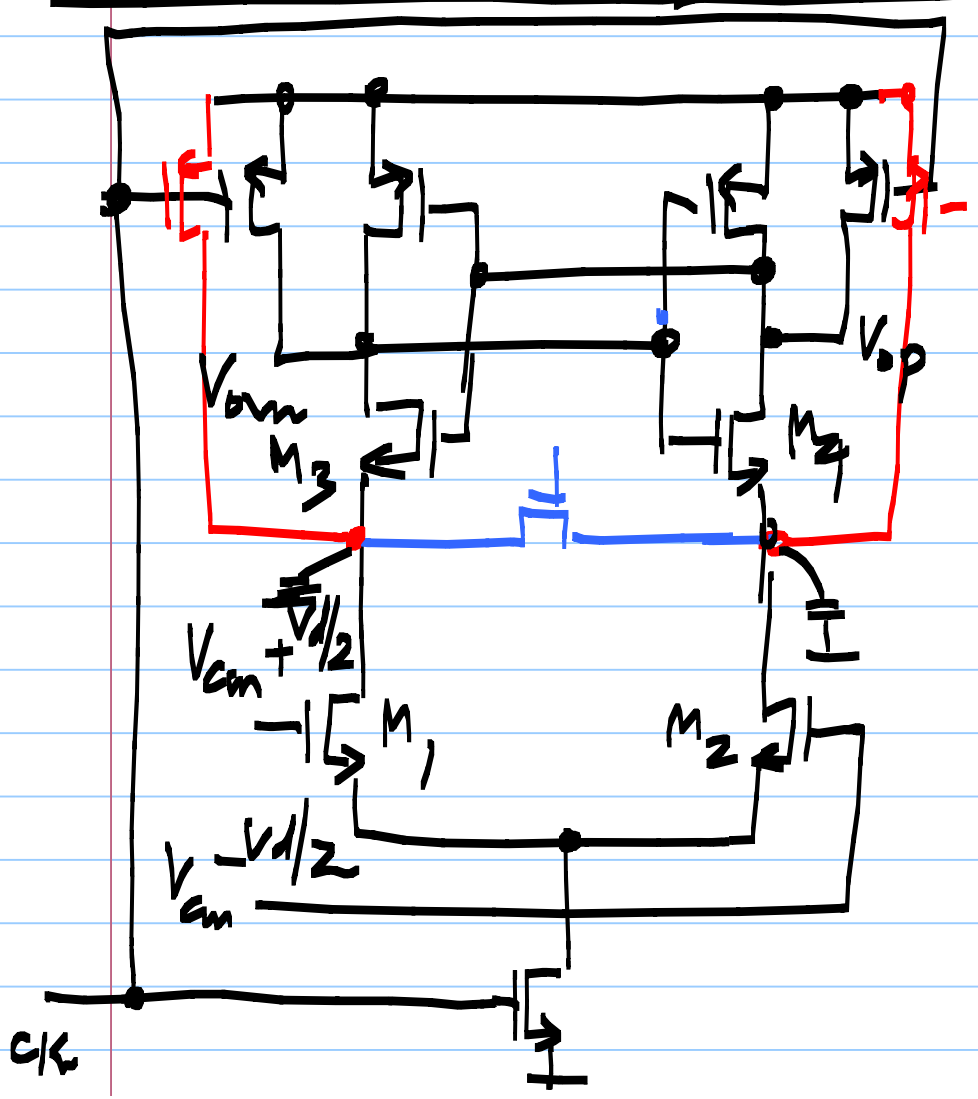
Strong Arm latch:

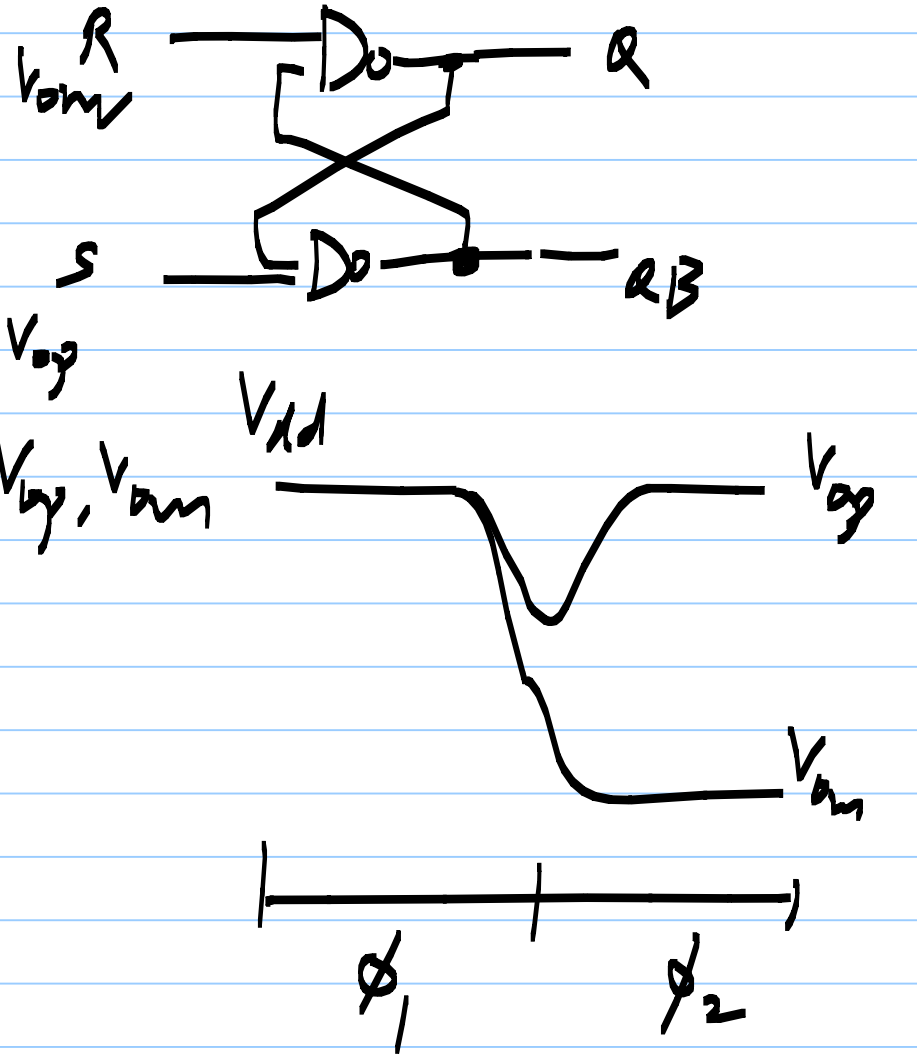


* Reset V_{op}, V_{om} to V_{DD}
* Input applied as currents to the cross-coupled inverter through a diff. pair
* $\phi_1 = 1$: $V_{op} = V_{om} = V_{dd}$ ($\phi_2 = 0$)
* optionally reset the drains of M_1 & M_2 to V_{DD}


$\phi_2 = \phi_3$
V_{dd}
M_5
M_6
V_{op}
V_{om}
M_3
M_4
$V_{icm} + V_d/2$
M_1
M_2
$V_{icm} - V_d/2$
ϕ_2
M_0
$V_{op} = V_{om}$
V_{up}
$V_{DD} - V_{Tp}$
V_{om}
ϕ_1
ϕ_2
V_{d1}, V_{d2}
V_{d2}
$V_{dd} - V_T$
V_{d1}

Strongarm latch + RS Nand latch + single clock phase ck





At the end of ϕ_2, $V_{d1} = V_{d2} \simeq 0$

In ϕ_1, current through the diff pair is zero.

V_{d1} & V_{d2} get pulled up by M_3 & M_4