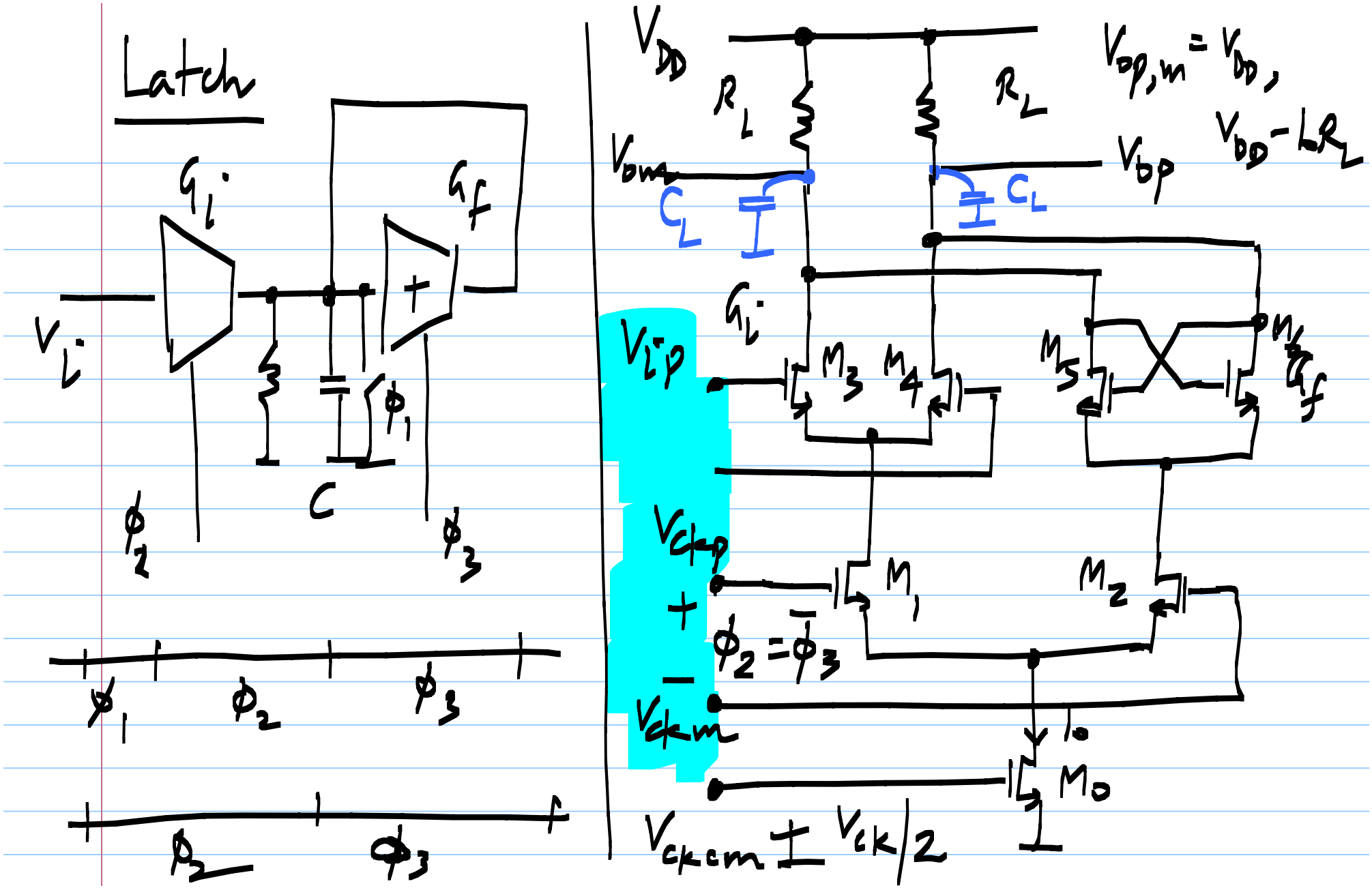
Latch
- Making decisions
- Flip-flops in CDR, Serializer/Deserializer


Latch
G_i
G_f
V_i
ϕ_1
ϕ_2
C
ϕ_3
ϕ_1
ϕ_2
ϕ_3
ϕ_2
ϕ_3
V_{DD}
R_L
R_L
$V_{op,m} = V_{DD}$,
$V_{DD} - LR_L$
V_{om}
V_{op}
C_L
C_L
G_i
V_{ip}
M_3
M_4
M_5
M_6
G_f
V_{ckp}
M_1
M_2
+
$\phi_2 = \bar{\phi}_3$
−
V_{ckm}
M_0
$V_{ckcm} \pm V_{ck}/2$

ECL - Emitter coupled logic

CML - Current mode logic

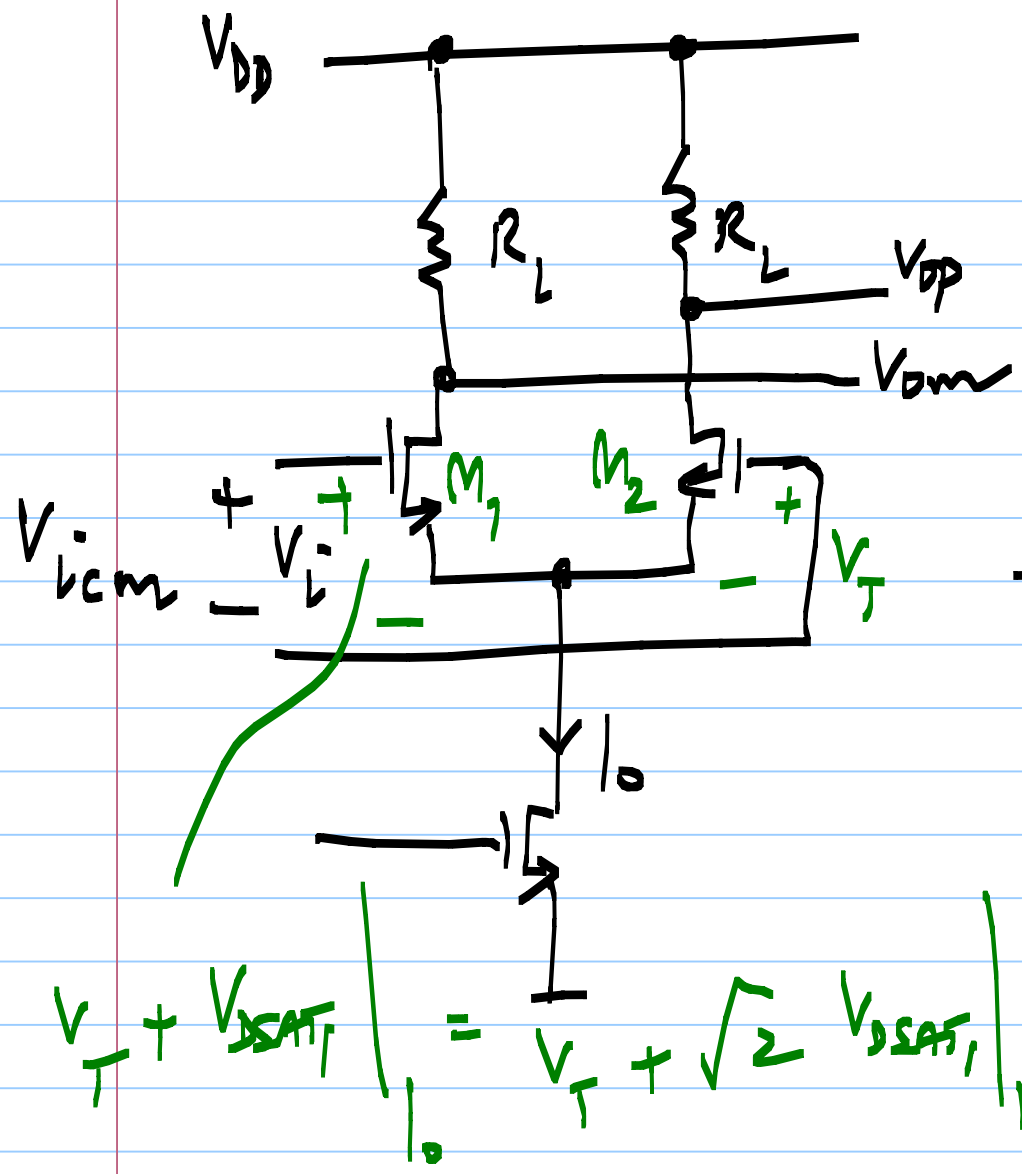
Output levels: V_{DD}, $V_{DD} - I_0 R_L$

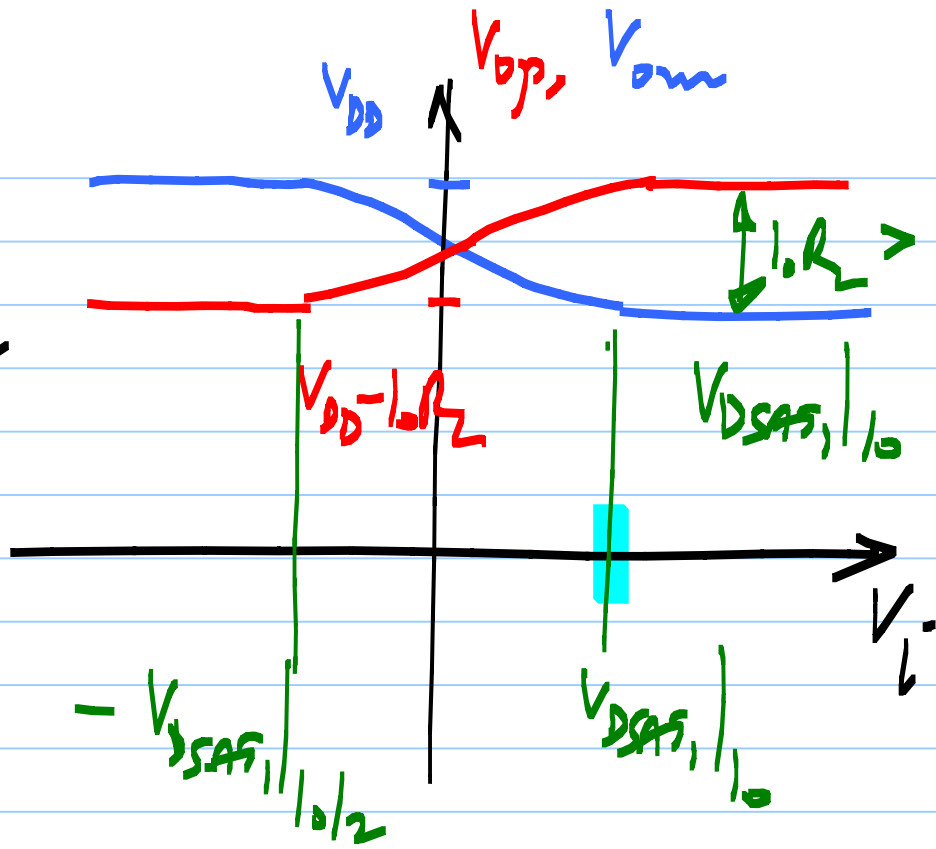
output swing $I_0 R_L$ must be > switching voltage $V_{DSAT_1}|_{I_-}$

$V_{i,cm}$: such that the transistors remain in saturation region

Cascade:

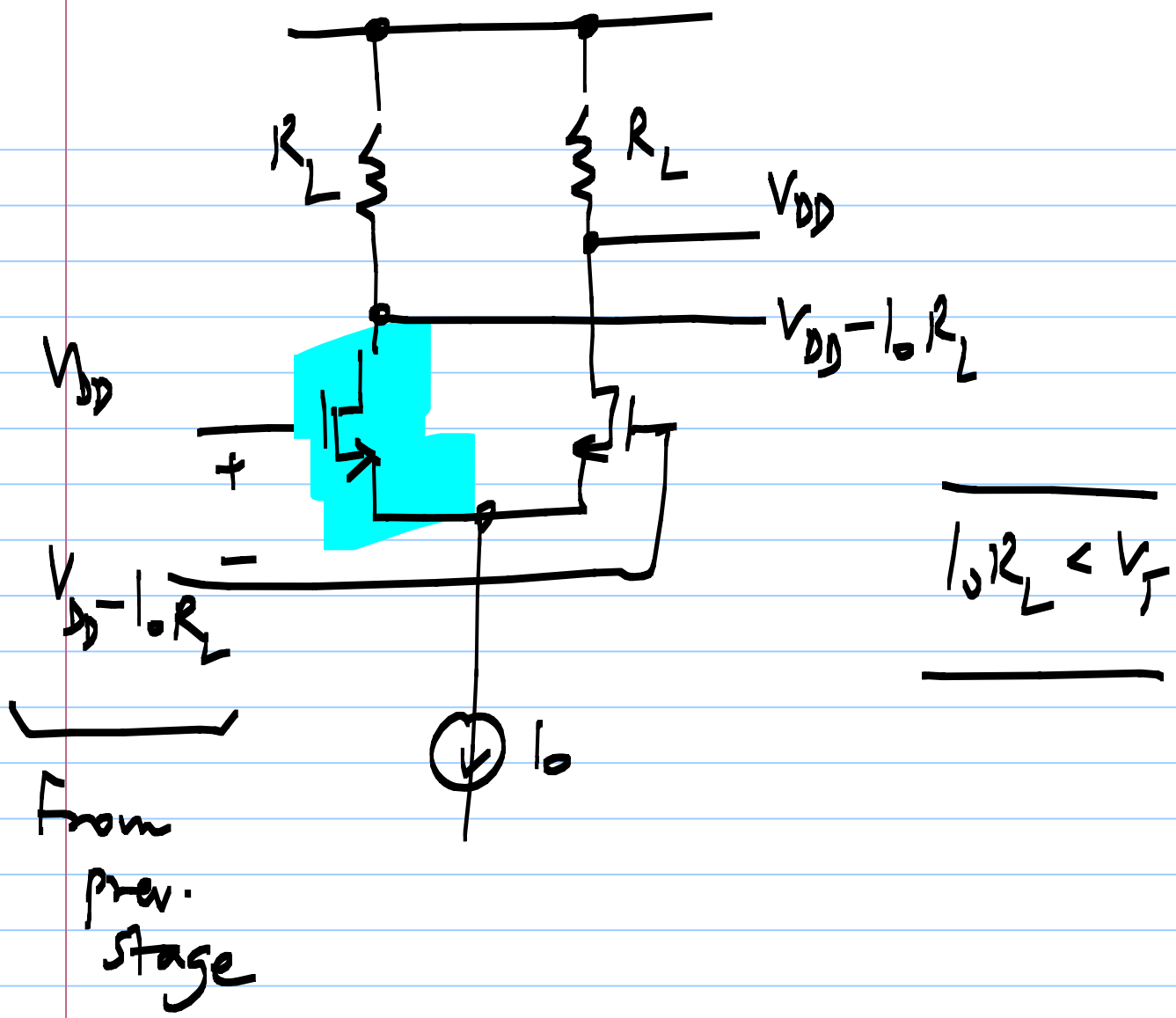
$$\left.\begin{aligned} V_{o,cm} &= V_{i,cm} \\ V_{DD} - I_0 R_L/2 &= V_{i,cm} \end{aligned}\right] \Rightarrow I_0 R_L < V_T$$





$$V_T + V_{DSAT_1}\Big|_{I_0} = V_T + \sqrt{2}\, V_{DSAT_1}\Big|_{I_0/2}$$

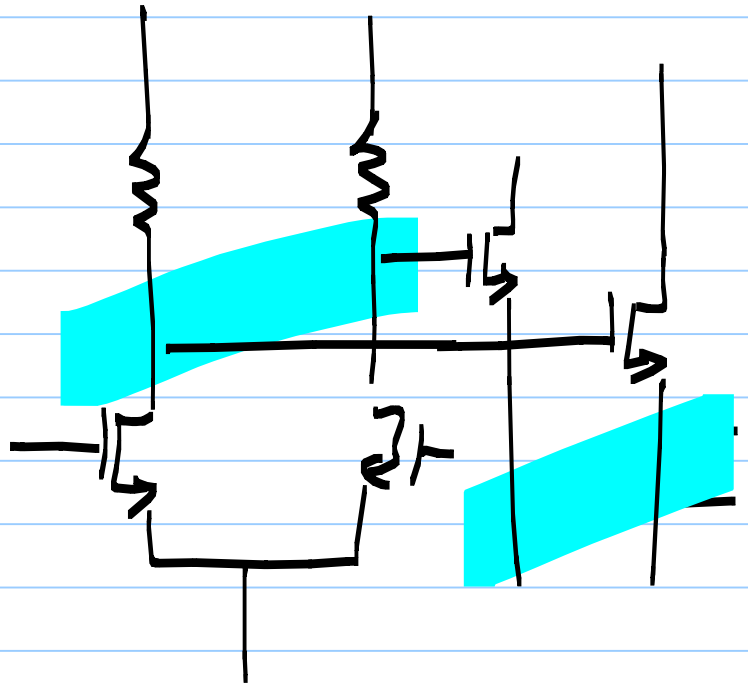
$$V_{icm} \pm V_i/2$$

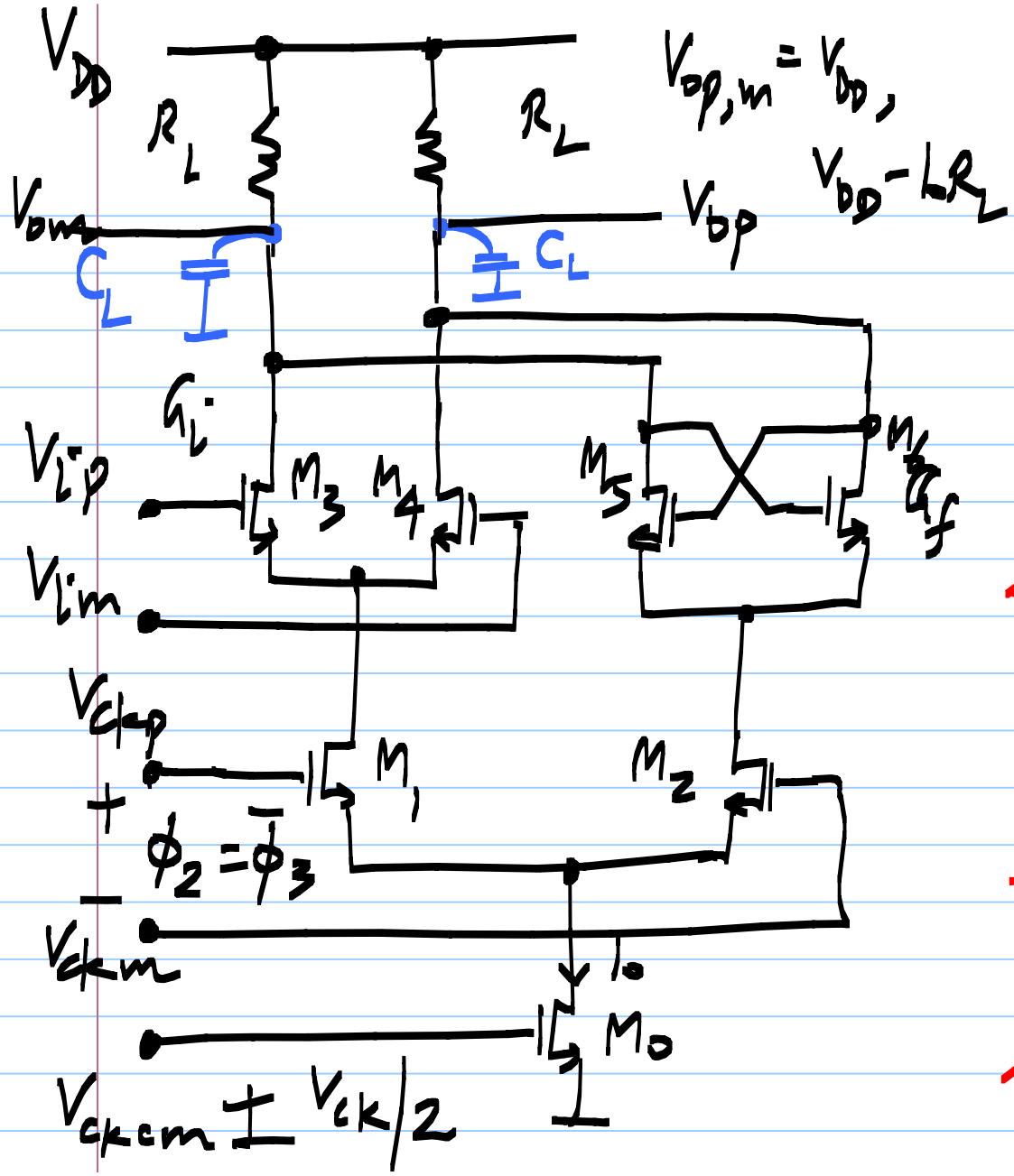


$I_o R_L < V_T$

Common mode voltage of V_{cap}, V_{ckm} must be lower than V_{icm}.

Tail current source has to be accommodated





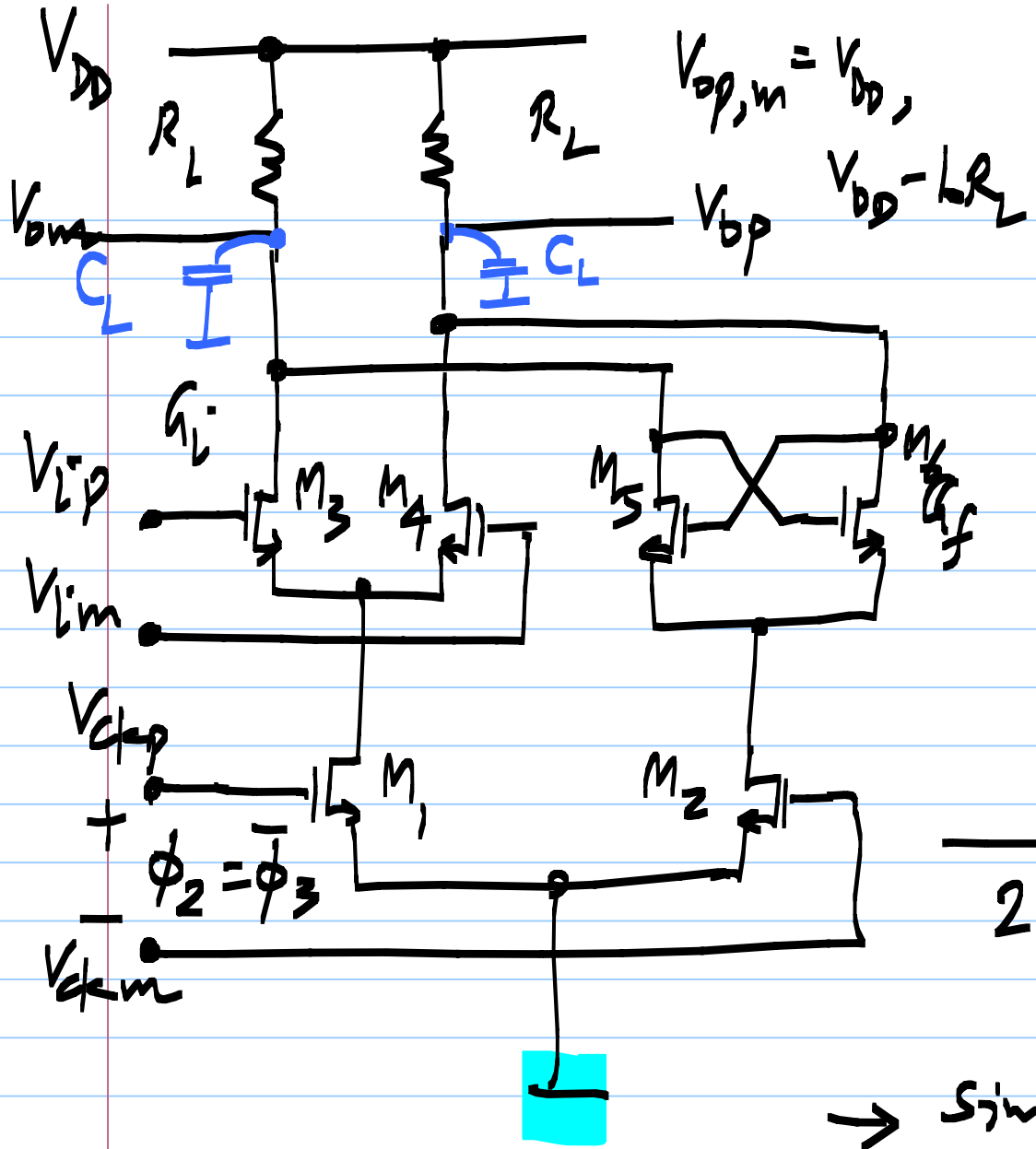
load

input signal diff pair

clock diff pair

Tail source

SiGe BJT



Simplifications

1. Eliminate the tail source

⇒ Current depends on V_{ckp}, V_{ckm} levels

Easier to fit into a lower supply voltage

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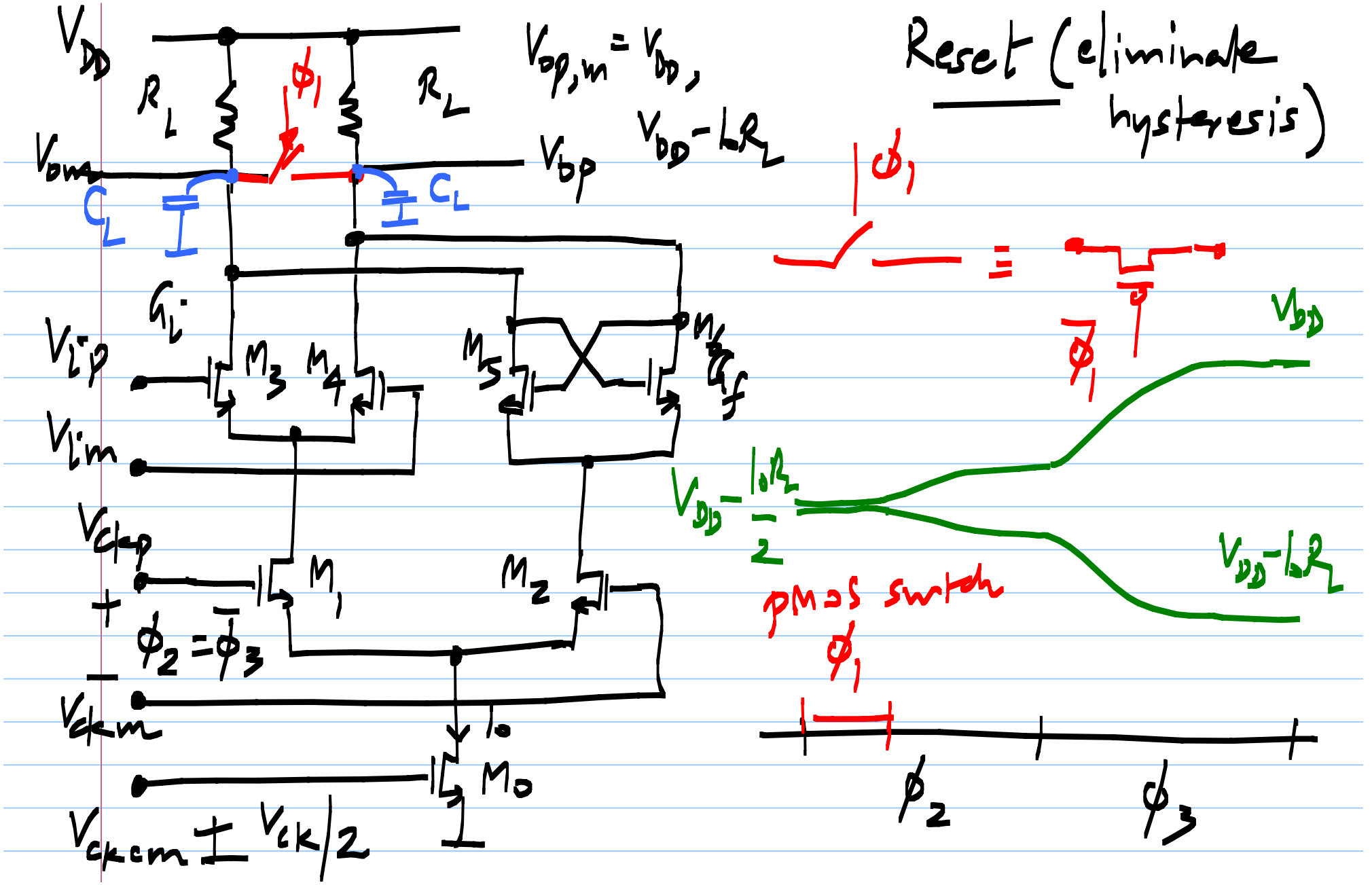
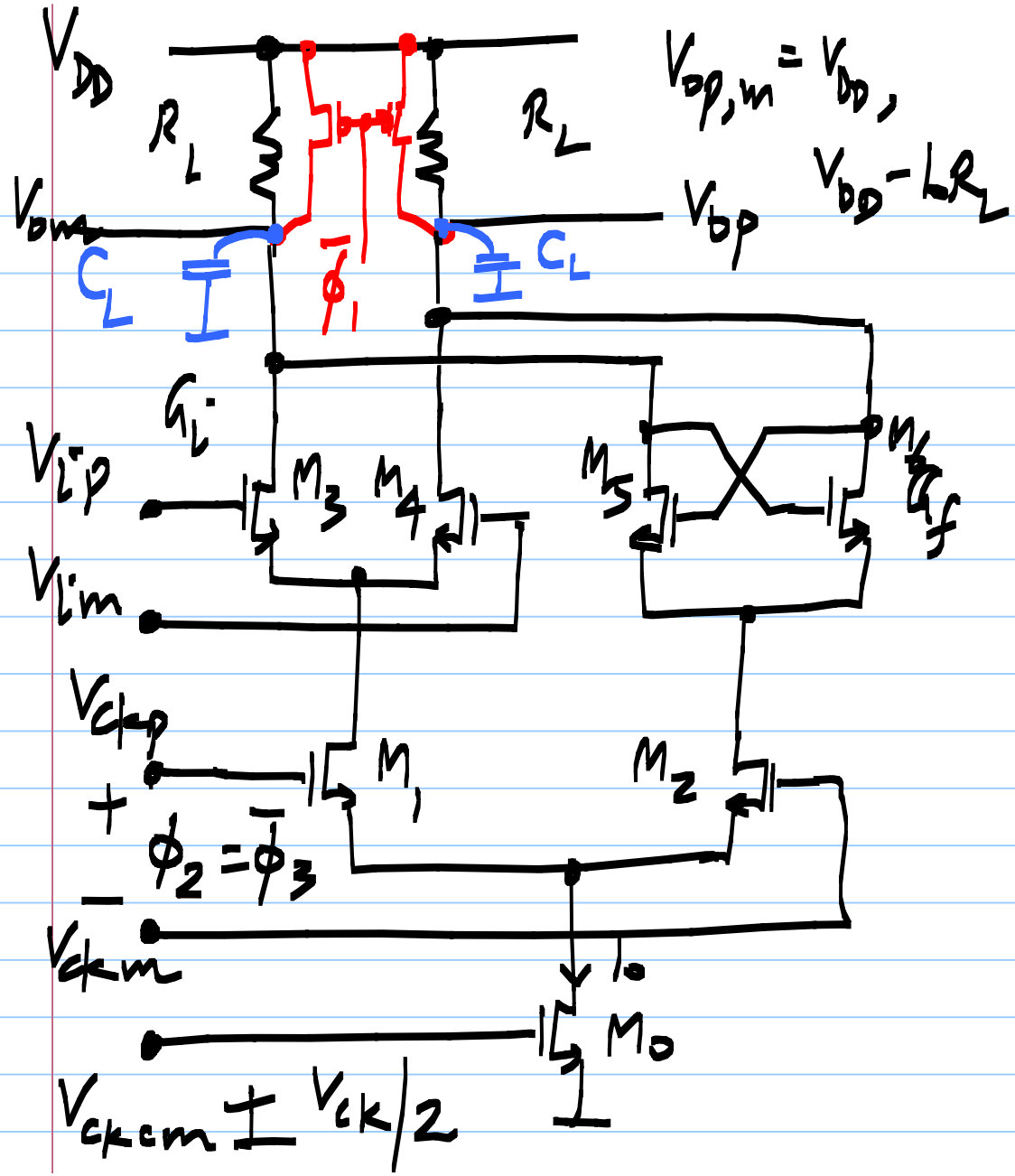
2. Use full swing V_{ckp}, V_{ckm}

→ simplified generation of V_{ckp}, V_{ckm}


V_{DD}
R_L
ϕ_1
R_L
$V_{op,m} = V_{DD}$,
$V_{DD} - I_0 R_L$
V_{om}
V_{op}
C_L
C_L
G_i
V_{ip}
M_3
M_4
M_5
M_6
V_{im}
V_{ckp}
M_1
M_2
$\phi_2 = \bar{\phi}_3$
V_{ckm}
I_0
M_0
$V_{ckcm} \pm V_{ck}/2$
Reset (eliminate hysteresis)
ϕ_1
V_{DD}
ϕ_1
$V_{DD} - \frac{I_0 R_L}{2}$
$V_{DD} - I_0 R_L$
pMOS switch
ϕ_1
ϕ_2
ϕ_3

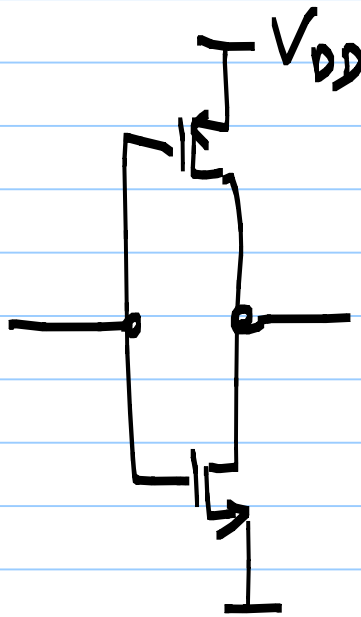


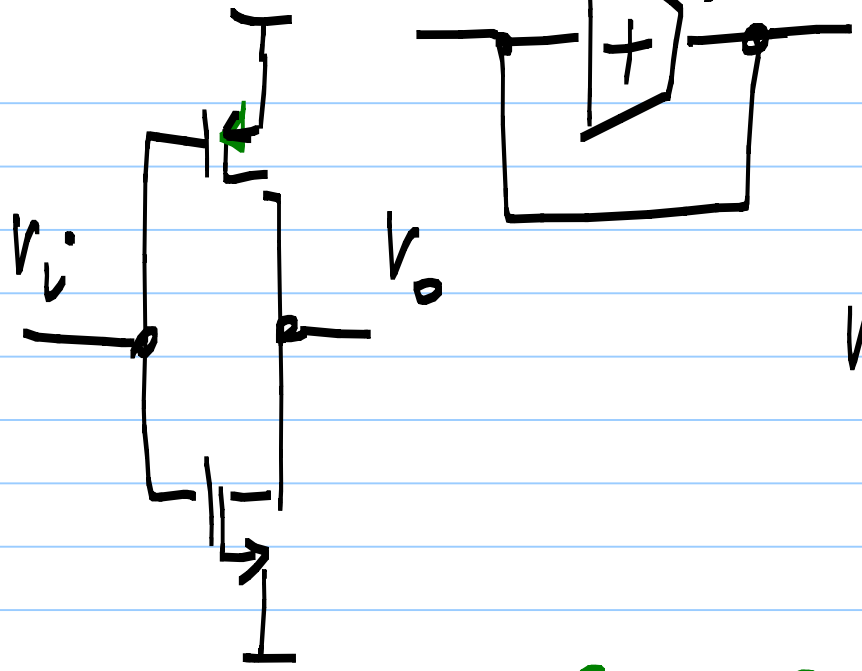
Reset both sides to V_{DD}

CML latch:

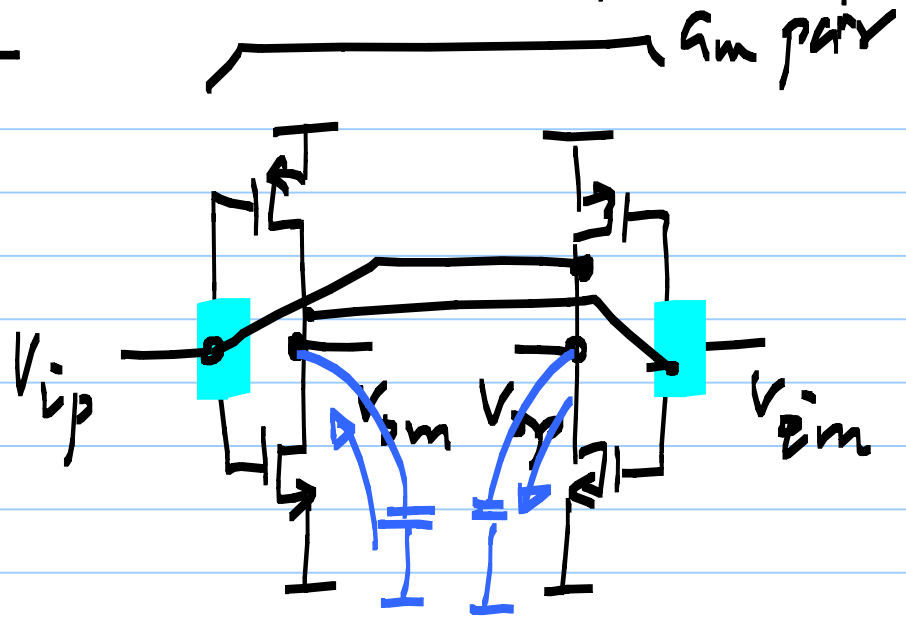
* Voltage swing limited
* Fastest latch in a given process
* Static power consumption
  (high power consumption)

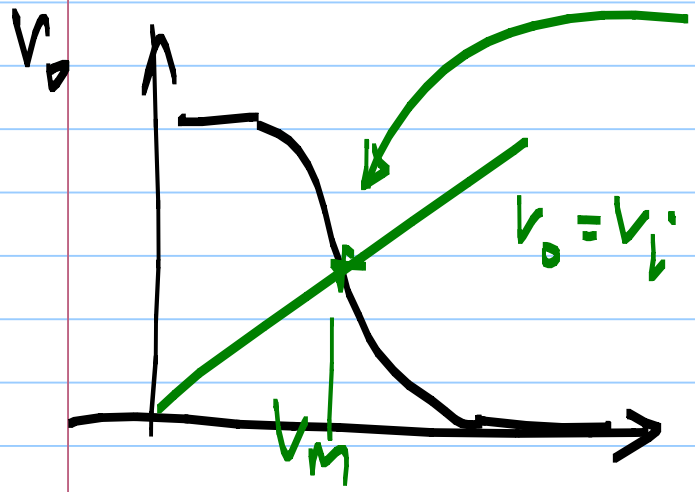
CMOS gates: no static current





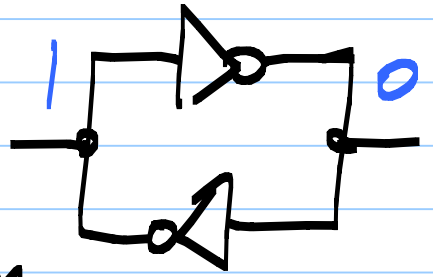
Pseudo differential

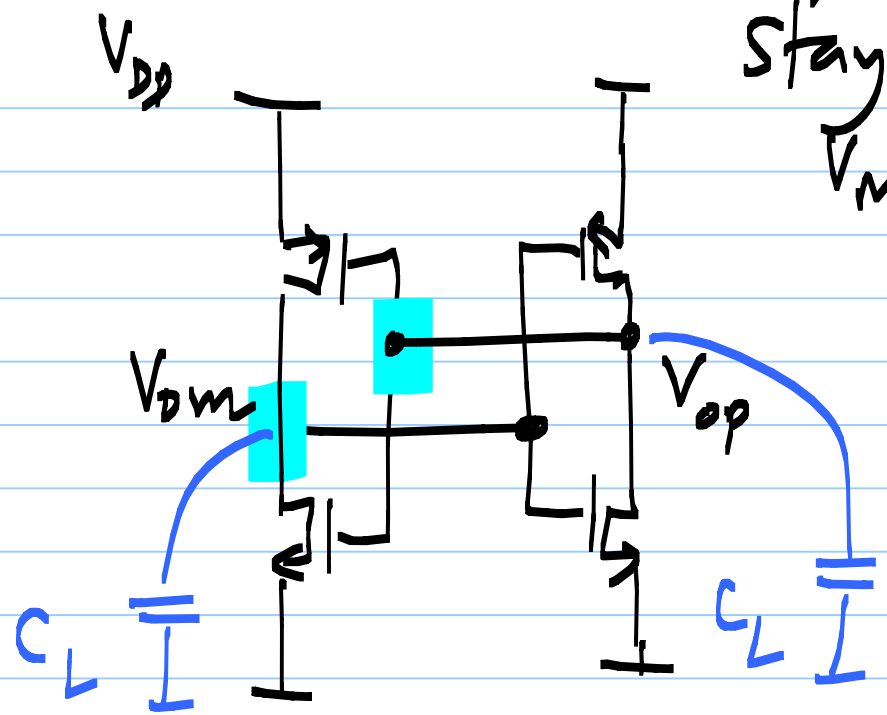




$G_m = g_{mp} + g_{mn}$

Both in saturation





Cross-coupled inverter pair

V_{op}, V_{om} perfect matching

Stay at V_M $\left[V_{op} = V_{om} = V_M \right.$ (self bias voltage)

$V_{op}, V_{om} = V_M \pm \Delta V$

→ Regenerate