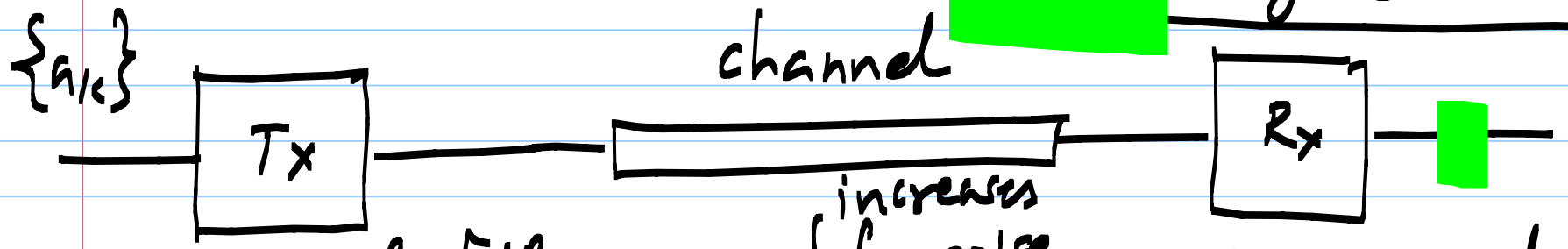
Linear equalization

$(H_{Tx} \cdot H_{Rx})$ — both for signal and xtalk



increases hf noise added before the CTLE

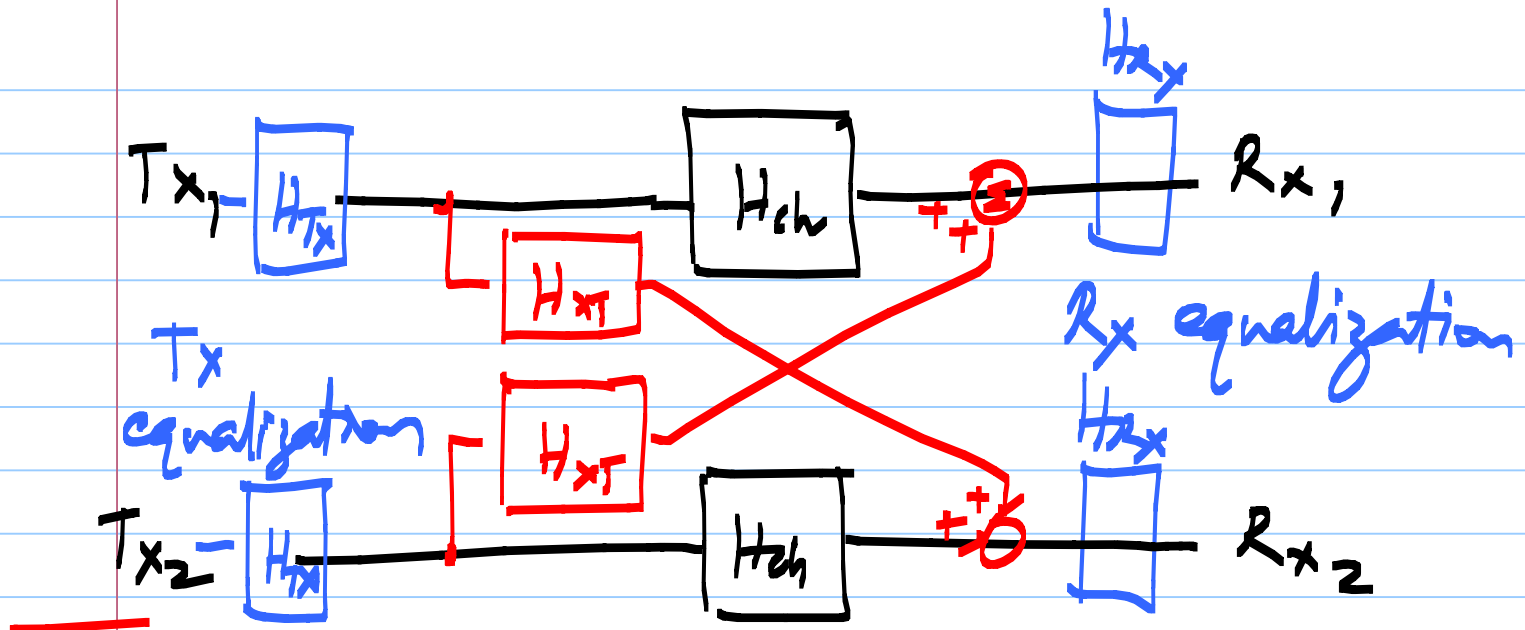
Semi-digital FIR

* Accurate weights
* Can realize high order, but gain has to be reduced to fit Tx voltage limits
* Pre- and post-cursor taps

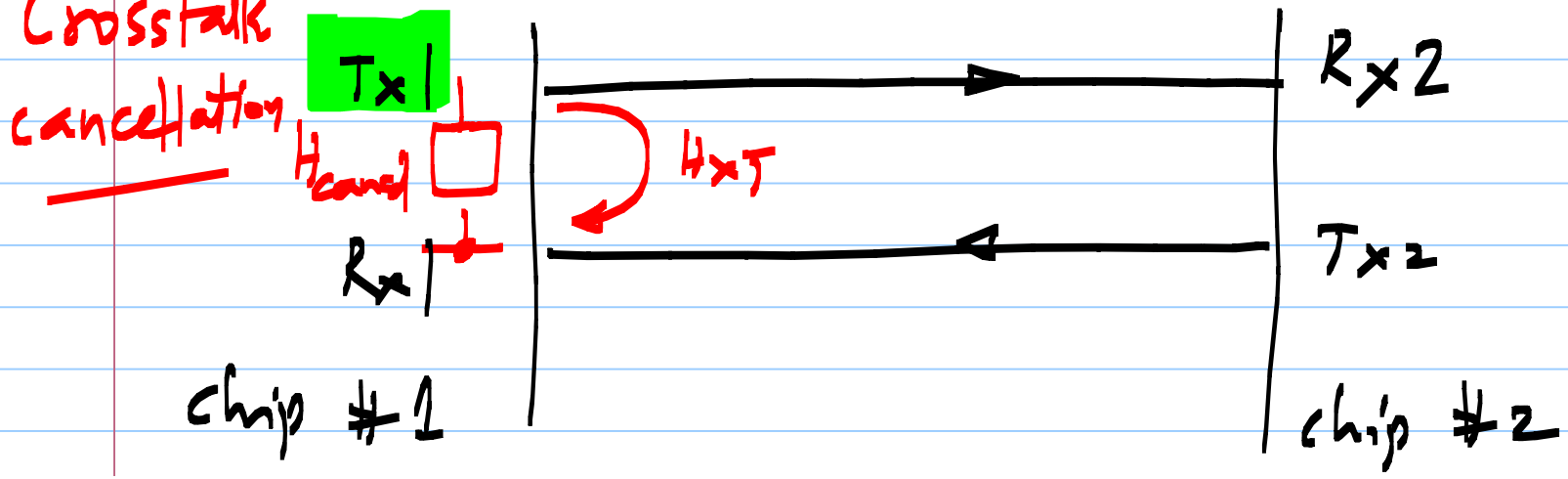
CT linear equalizer

* Simple (1 zero)
* Depends on analog comp. values
* Can have gain
* hf boost
* Ind. of clock

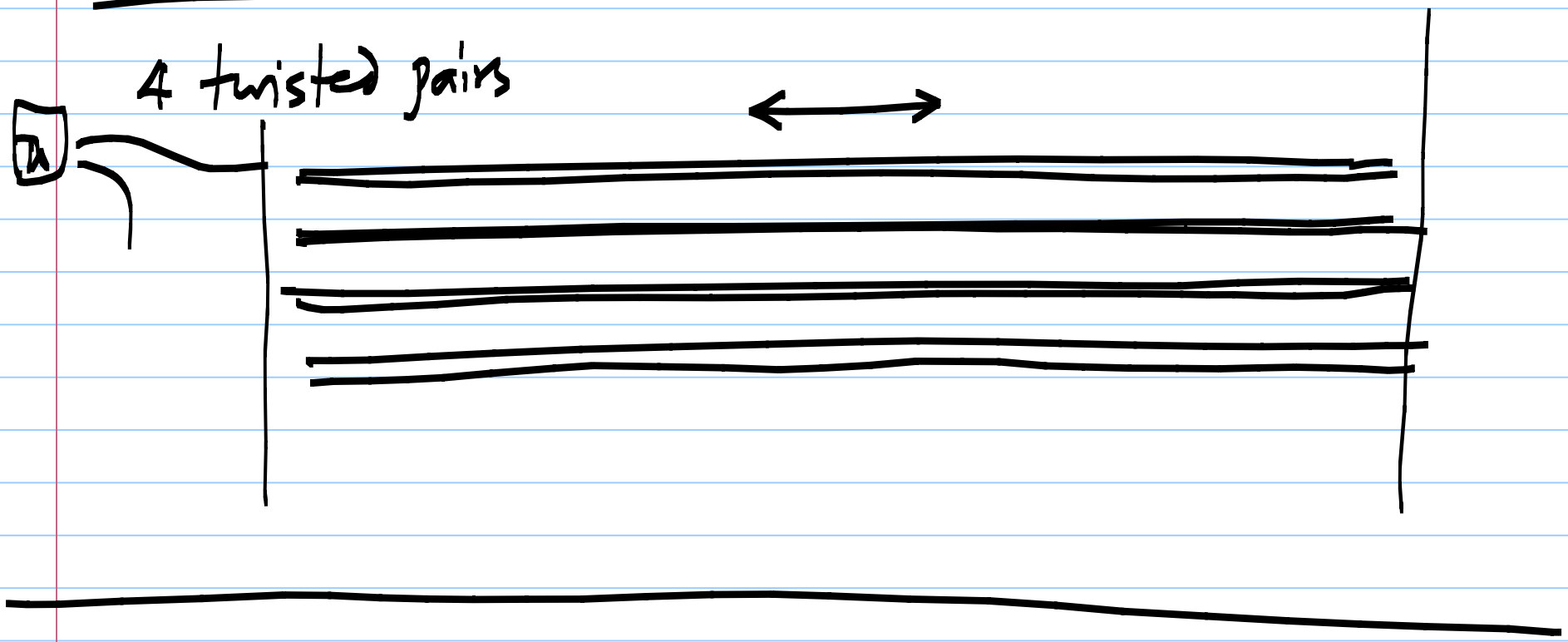
They increase crosstalk relative to the signal

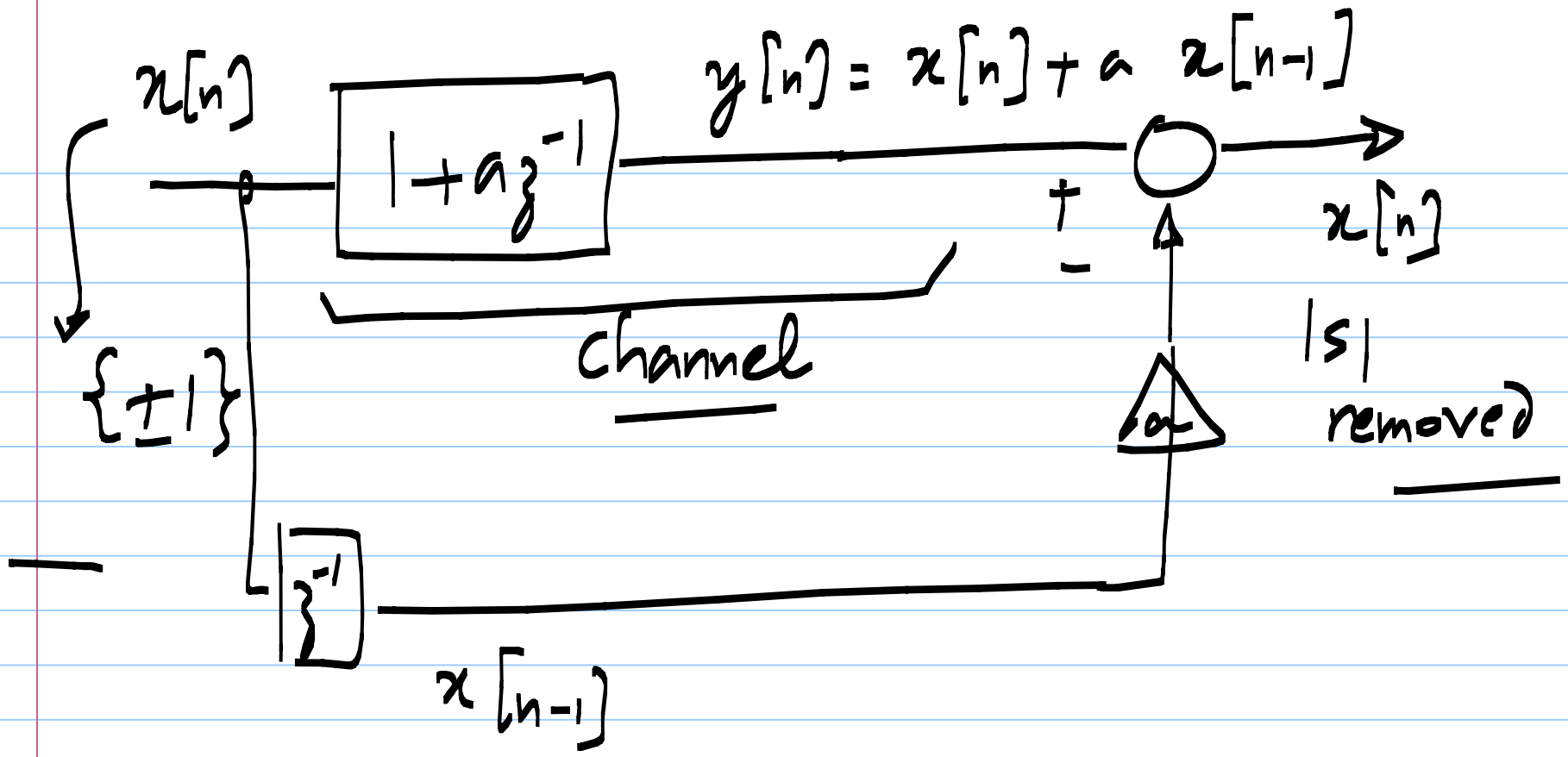


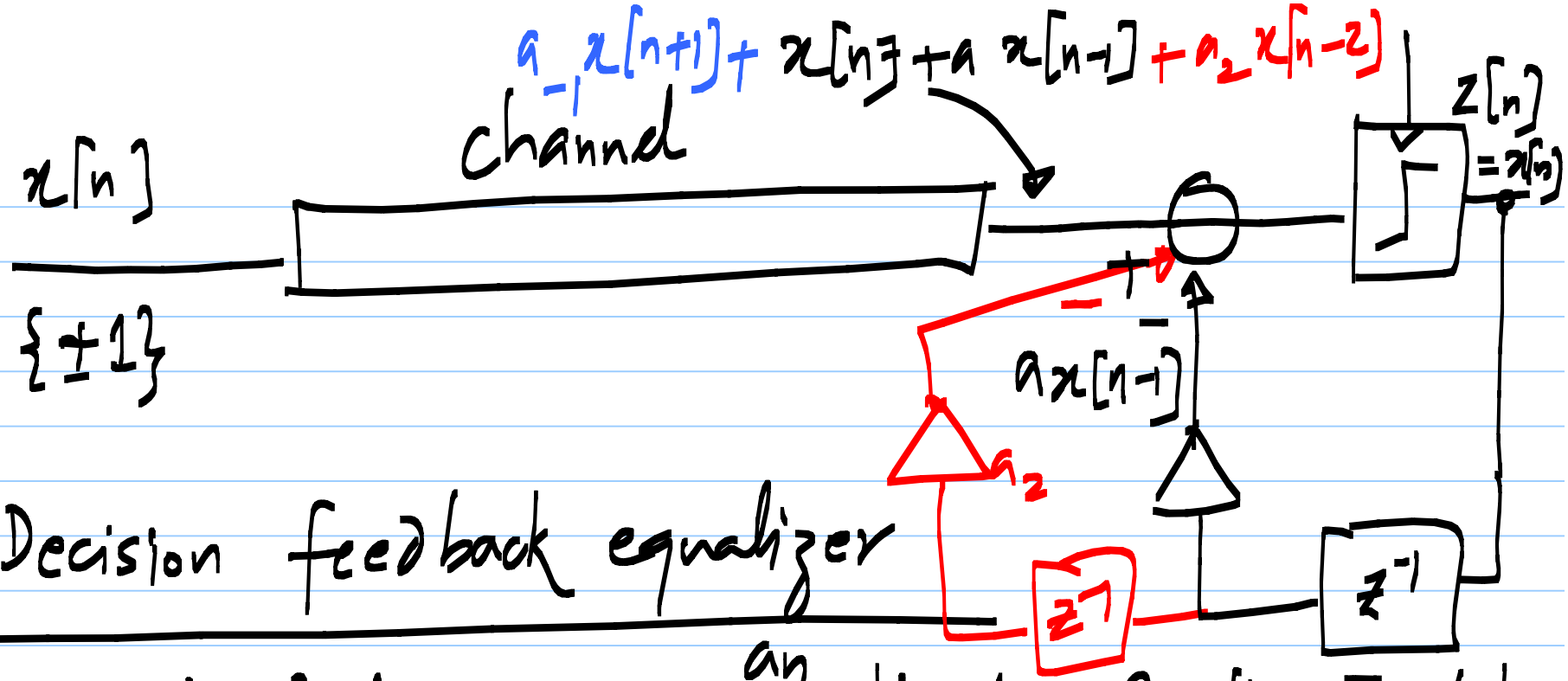
Crosstalk cancellation



Ethernet




x[n]
$1+az^{-1}$
$y[n] = x[n] + a\ x[n-1]$
+
−
x[n]
Channel
{±1}
|s|
removed
a
z^{-1}
x[n-1]

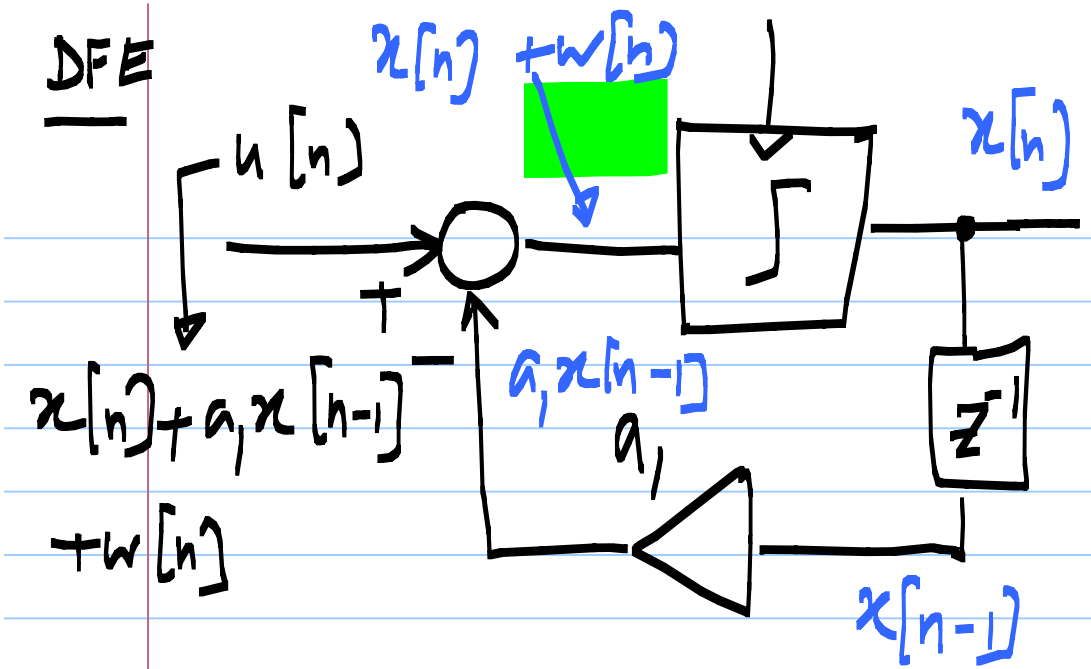


Decision feedback equalizer

Use the Rx decisions as an estimate $\hat{}$ of the Tx bits and feedback from that

Can only cancel post-cursor ISI

DFE



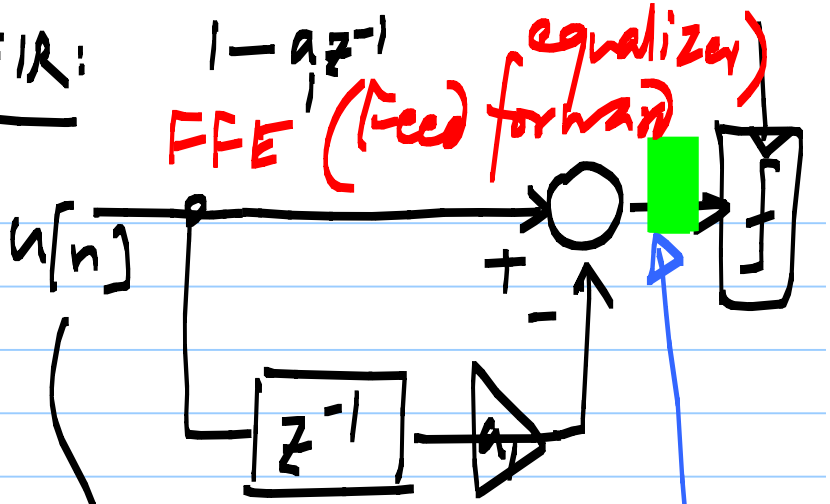
x[n]: Tx bits

w[n]: crosstalk

Crosstalk/Noise not boosted at Comparator input

Xtalk/noise boosted at Comparator input

FIR: $1 - a_1 z^{-1}$ FFE (feed forward equalizer)



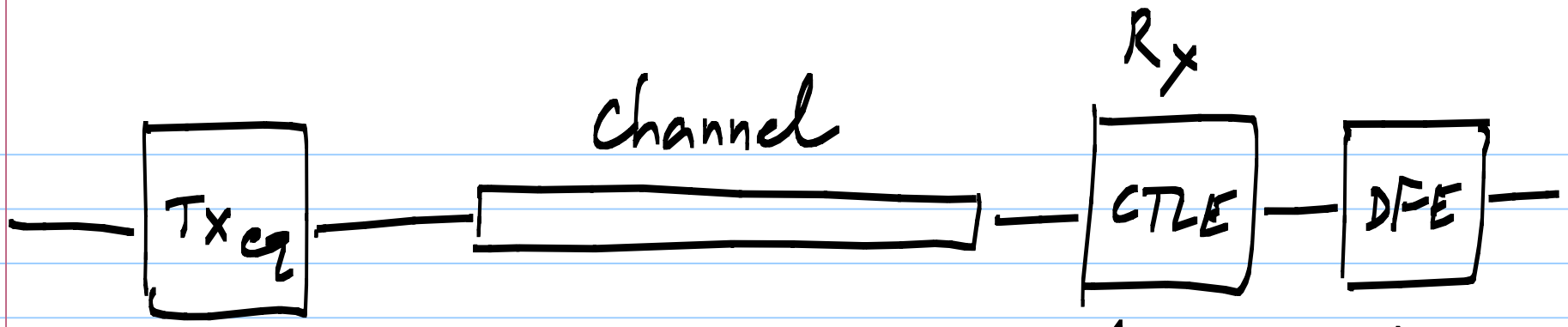
x[n] + a1 x[n-1] + w[n]

w[n] − a1 w[n-1]

W(z) (1 − a1 z^-1)

Decision feedback equalizer

* Feedback from Rx decisions
* Potential for error propagation —
  Not an issue @ small BER
* No amplification of noise / crosstalk



Semi digital

Reduces steady-state amplitude

Pre-cursor ISI

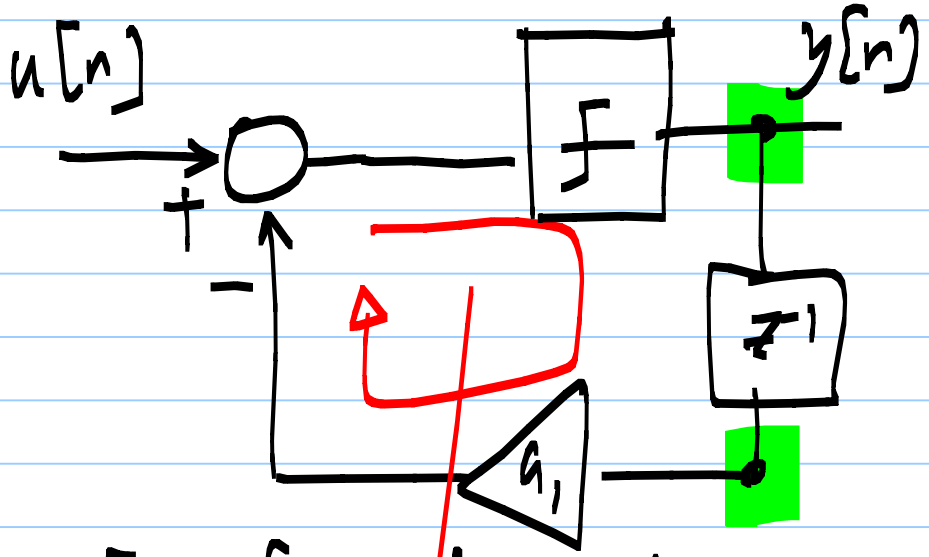
Independent of CDR

Eye opening

Needs CDR

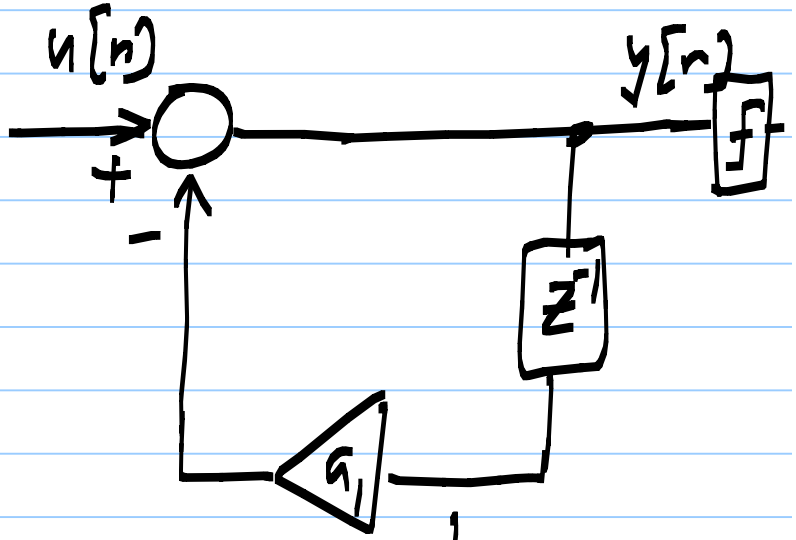
Effective, only for post-cursor ISI

DFE



DFE for channel TF

$1 + a_1 z^{-1}$



Filter.

$$\frac{1}{1 + a z^{-1}}$$

Implementation : Very challenging