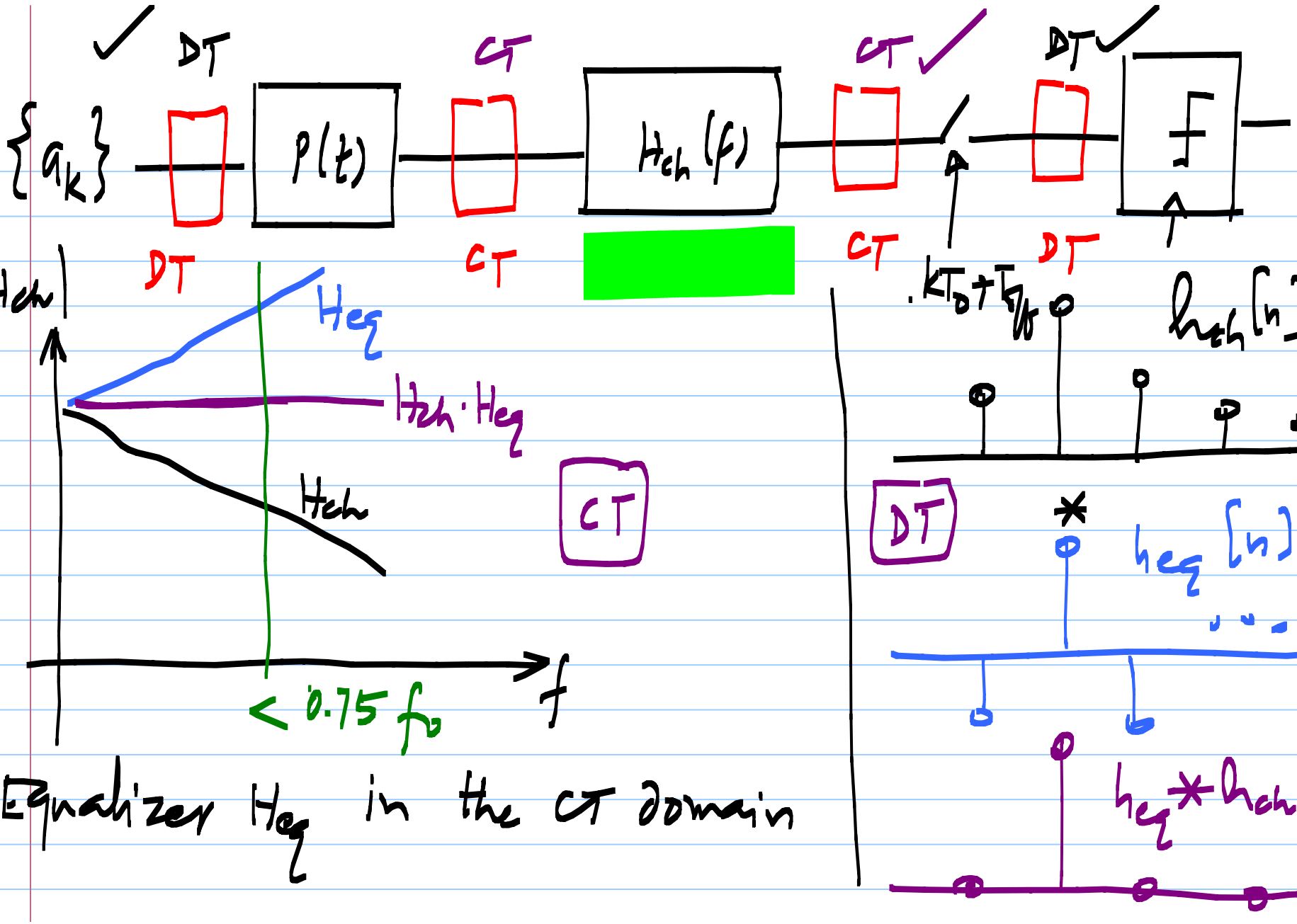
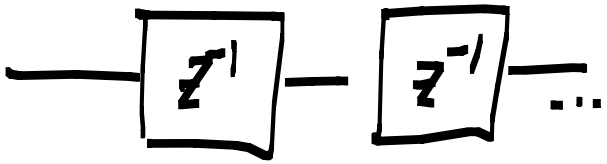


Equalizer H_{eq} in the CT domain

Rx equalization:



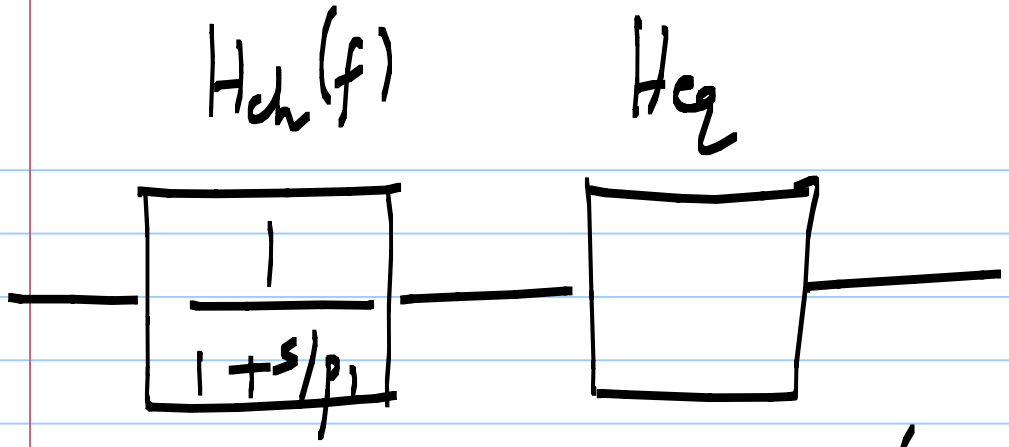
DT domain after sampling → clock recovery has to be functional

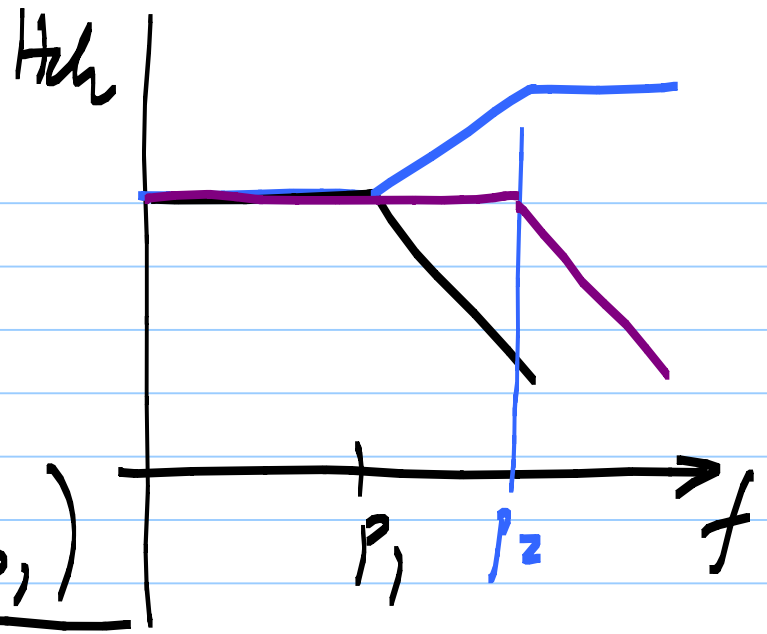
- Transfer fn. can be implemented more precisely
- Need analog delays [Can be realized after the ADC]

CT domain : Does not require the clock

Analog inaccuracy in the equalizer TF.

Low order equalization





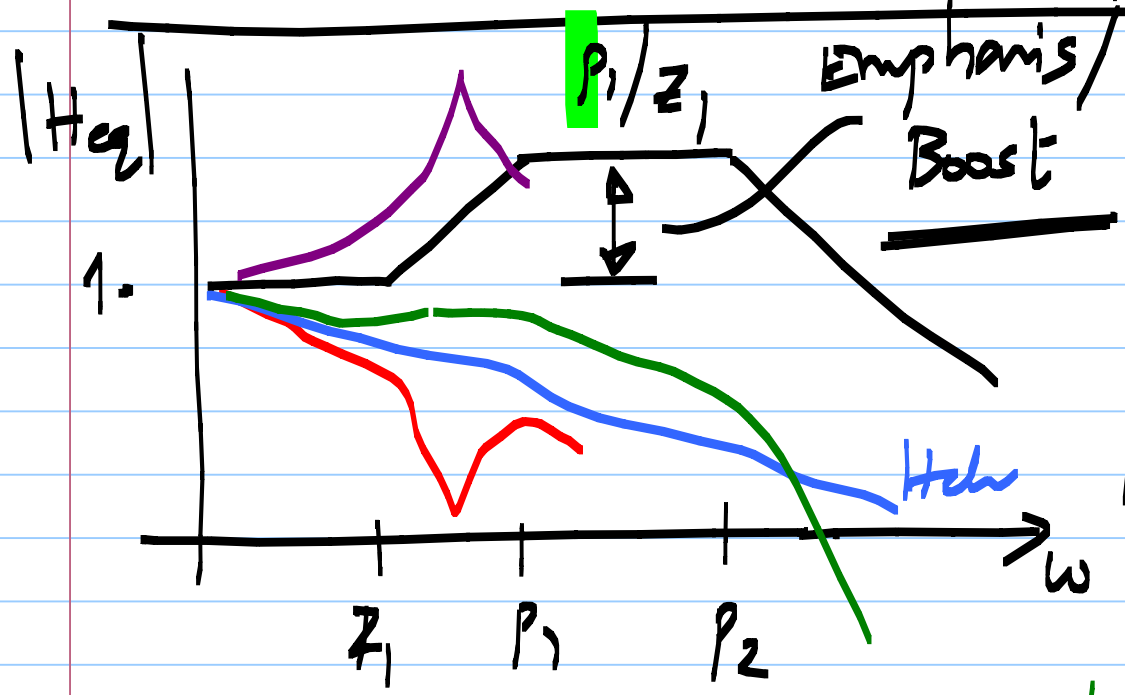
Single-pole low pass

$$H_{eq} = \frac{(1+s/p_1)}{(1+s/p_2)(1+s/p_3)\cdots}$$

Ideal equalization

$$H_{eq} = H_{ch}^{-1}(f)$$

Continuous-time linear equalizer



$$\left[\frac{1+s/z_1}{(1+s/p_1)(1+s/p_2)}\right]$$

$p_2 > p_1 > z_1$

$$\left[H_{ch}^{-1}\right]$$

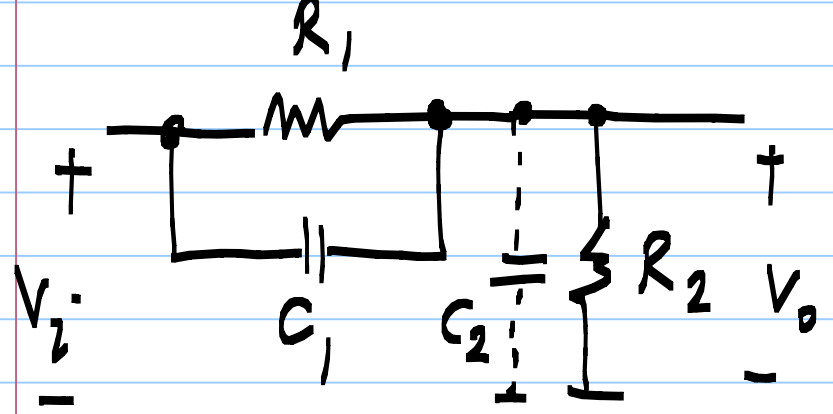
High order transfer fn. $\left(\frac{1+s/z_1}{1+s/p_1}\right)(\ldots)$

Nulls in H_{ch}

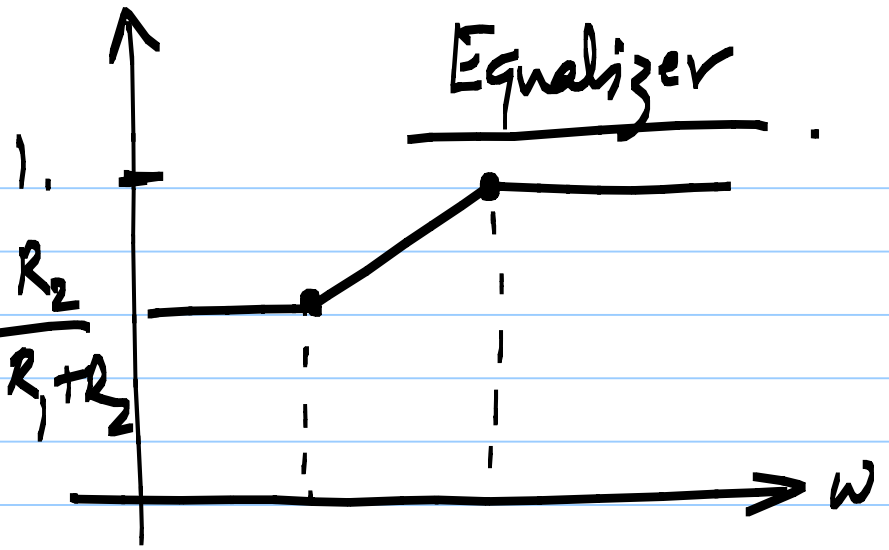
Implementation:

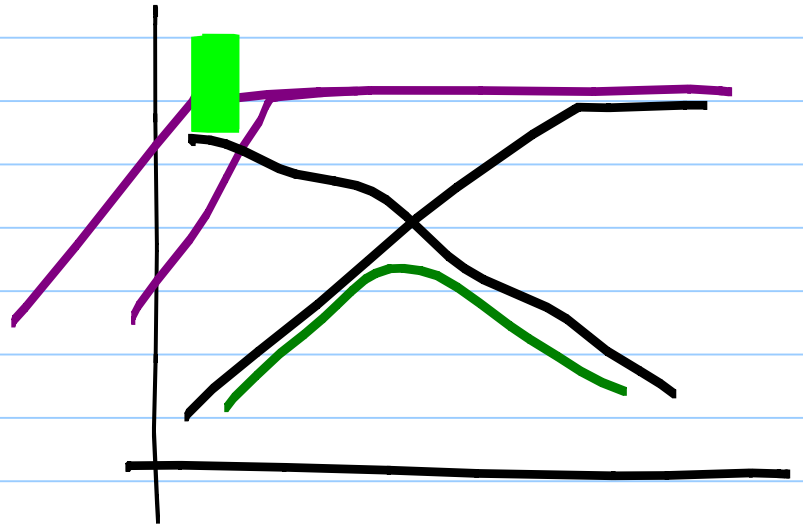
$$H_{eq}(s) = \frac{1 + s/z_1}{1 + s/p_1}$$

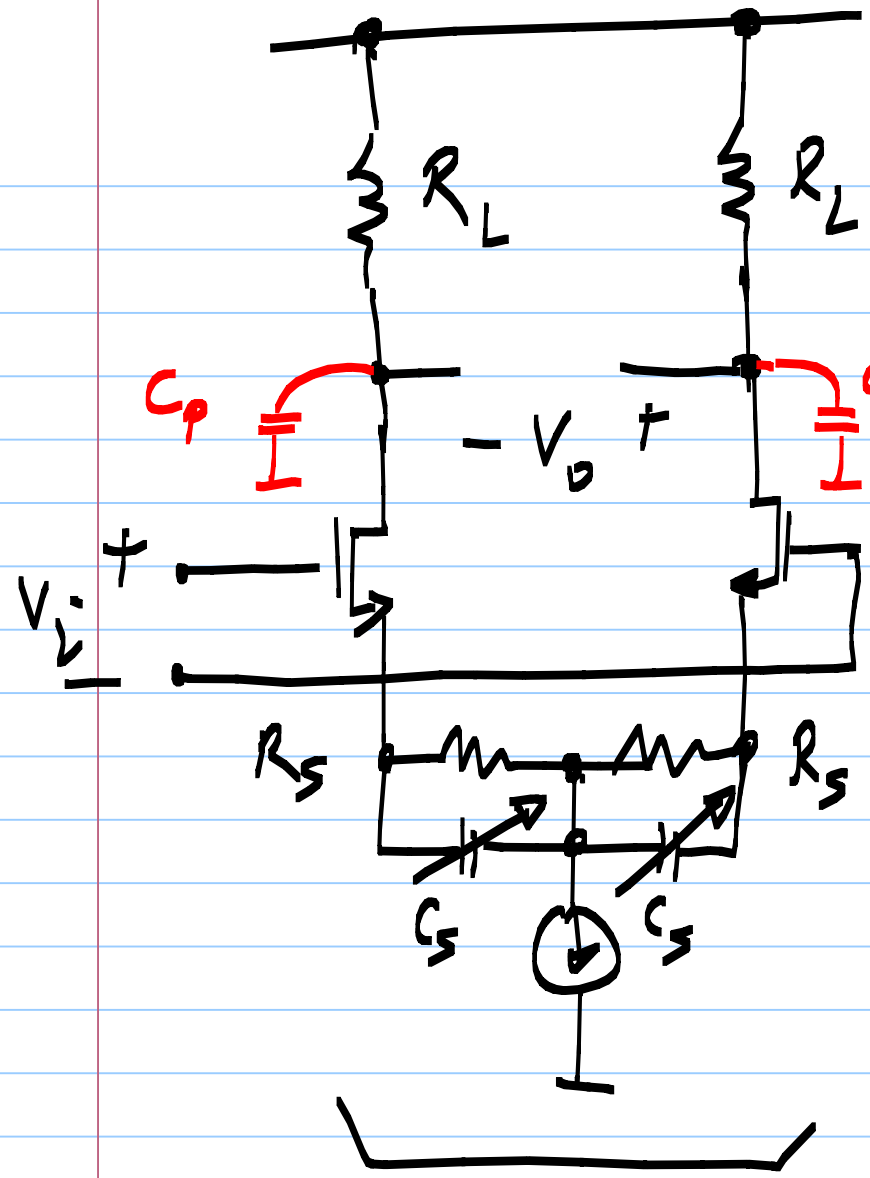
$z_1 < p_1$



Equalizer

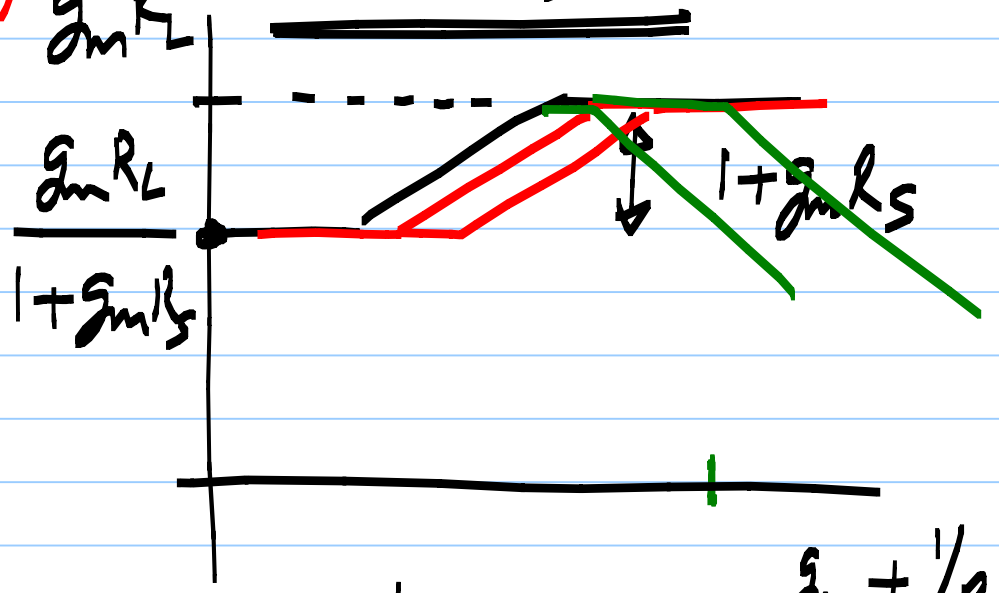




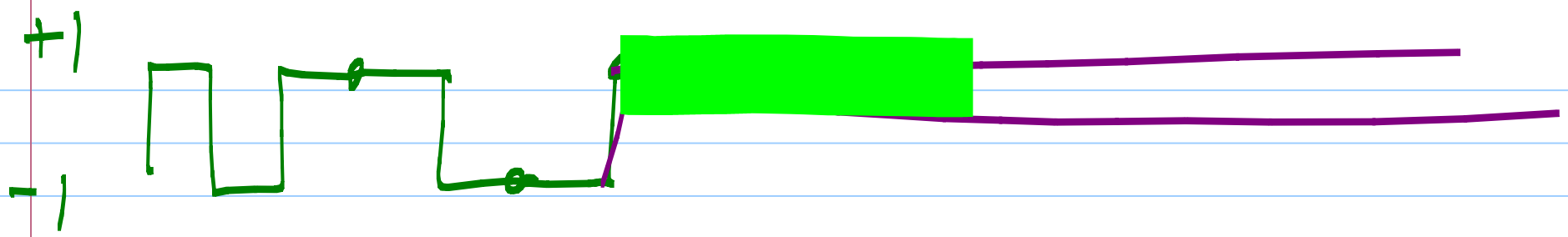


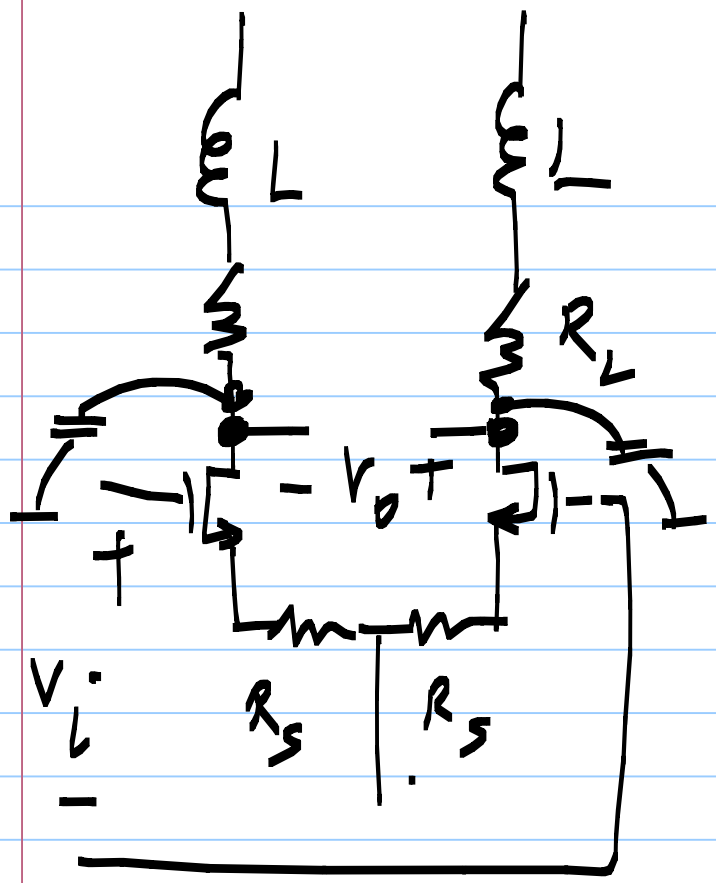
$$\frac{1+s/z_1}{1+s/p_1}\qquad\frac{1}{1+s/p_2}$$

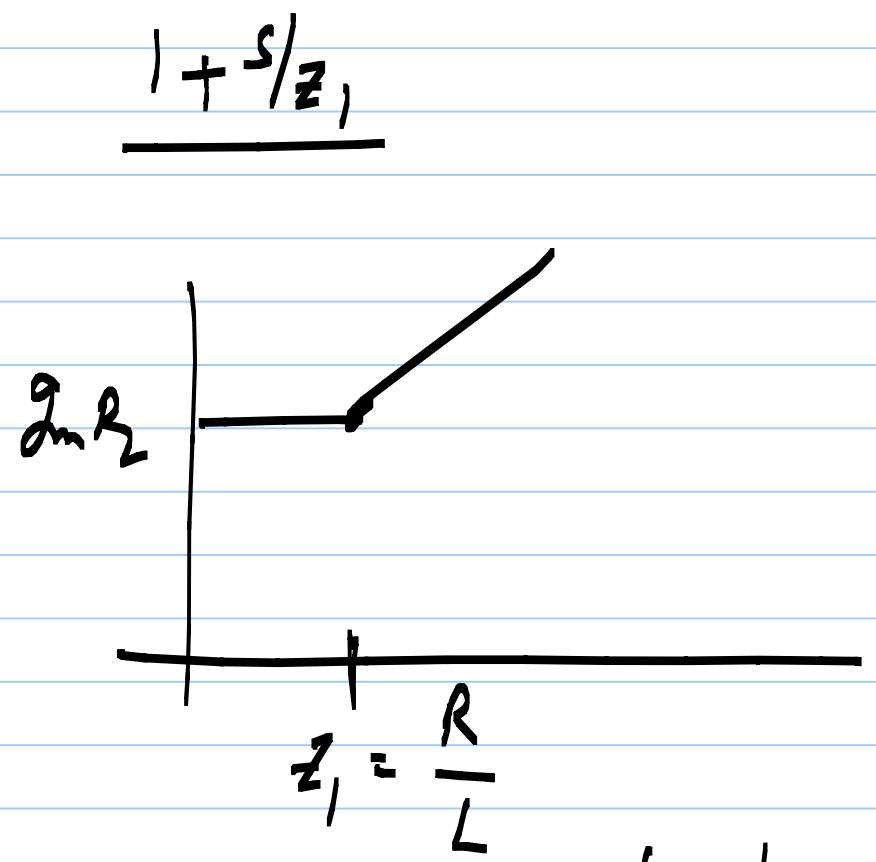
$$p_2 = 1/R_L C_\mu$$



$$z_1 = \frac{1}{R_S C_S}\ ;\ p_1 = \frac{g_m + 1/R_S}{C_S}$$


+1
-1

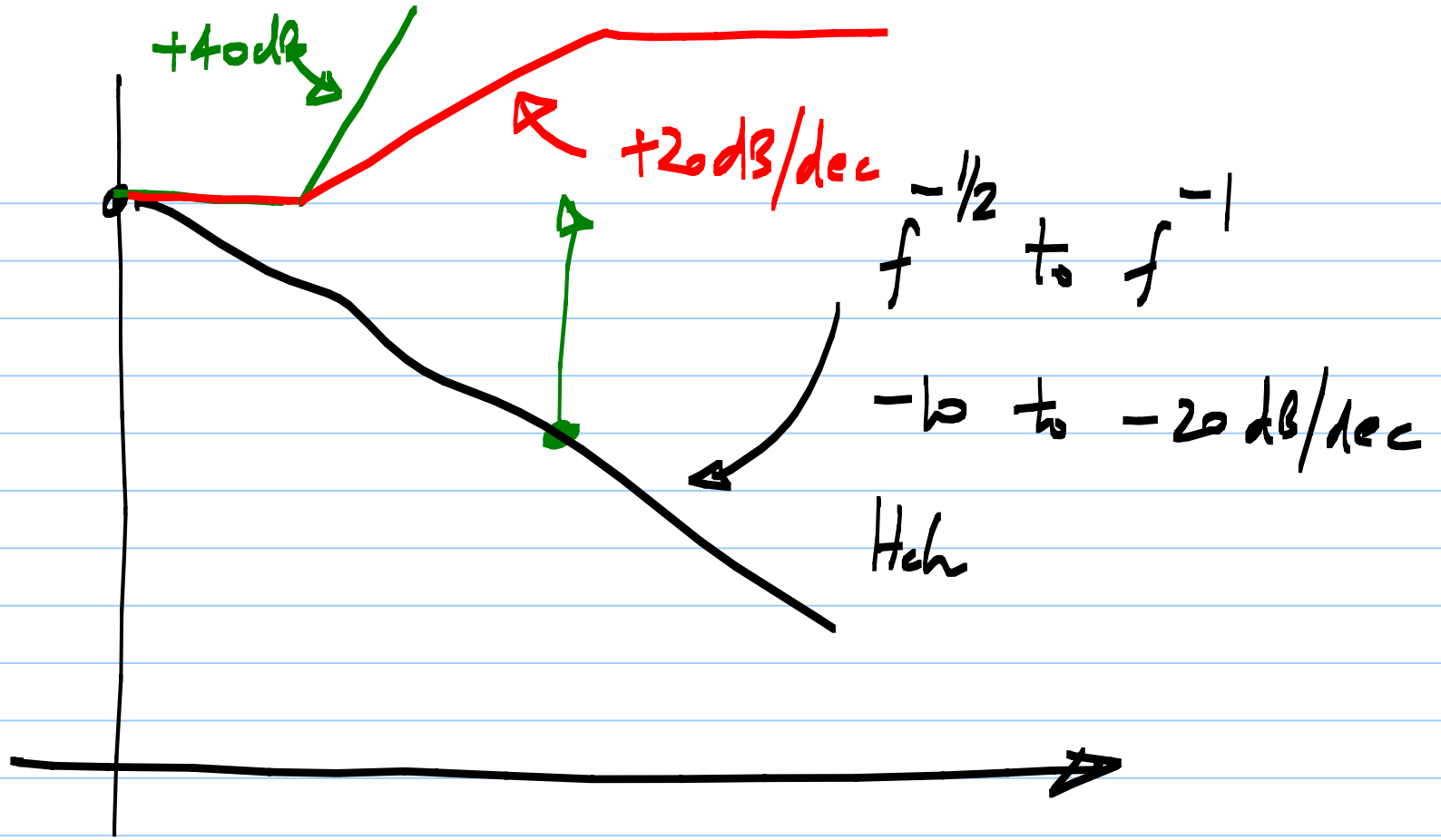




To realize a low freq. zero, L has to be large

CTLE in the R_x :

* Provides equalization independent of clock recovery
* 1 zero / pole realized to get some high frequency boost


+40dB
+20dB/dec
$f^{-1/2}$ to f^{-1}
-10 to -20 dB/dec
Hch