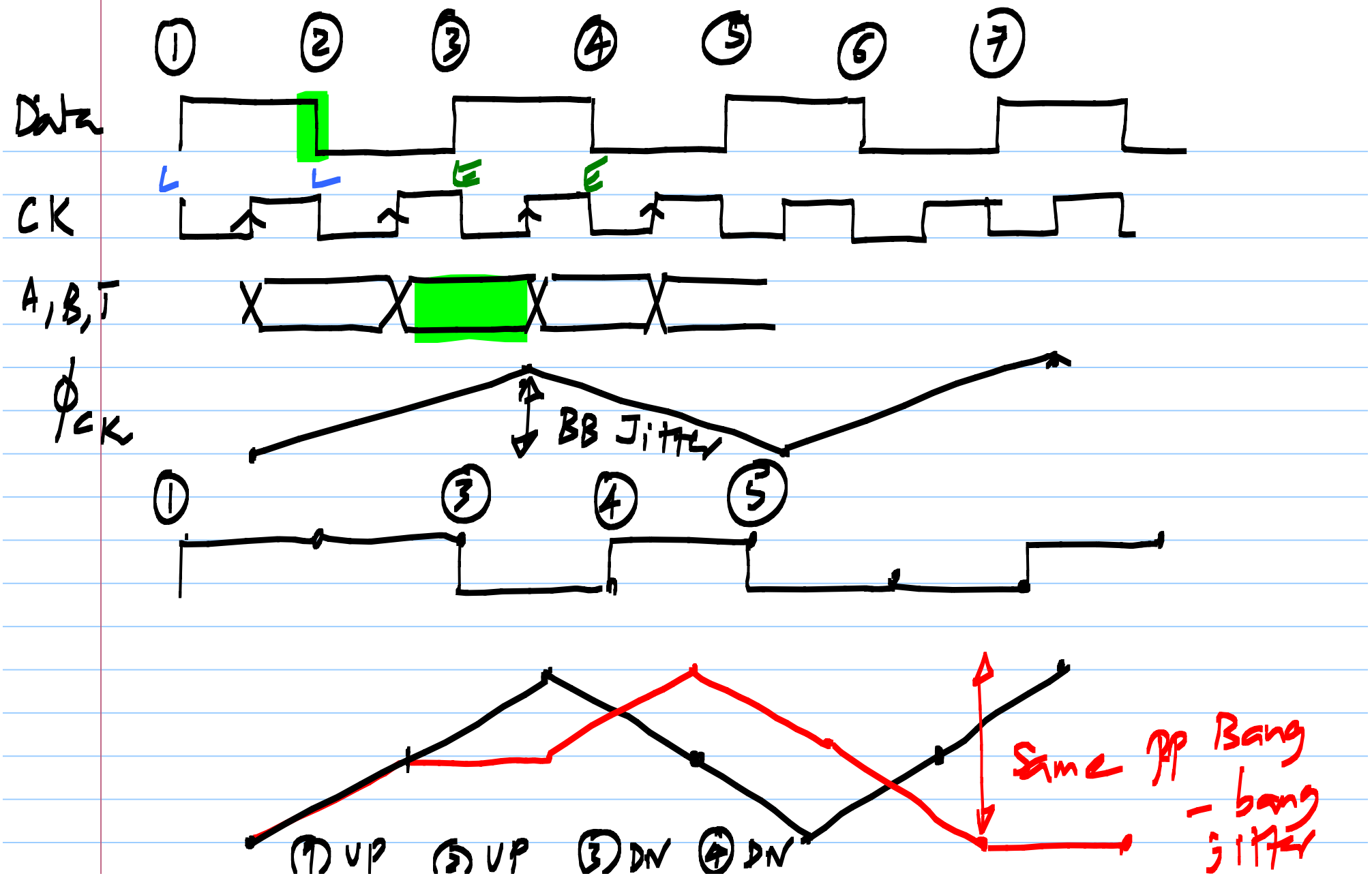
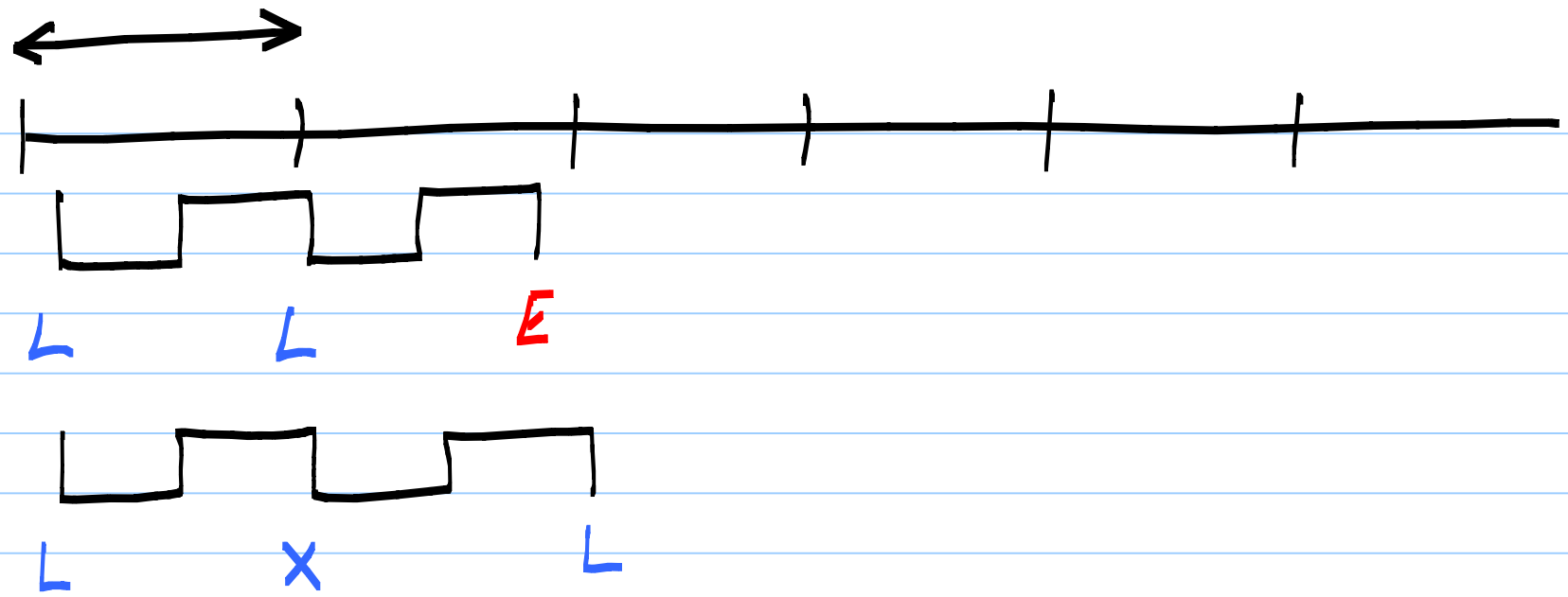
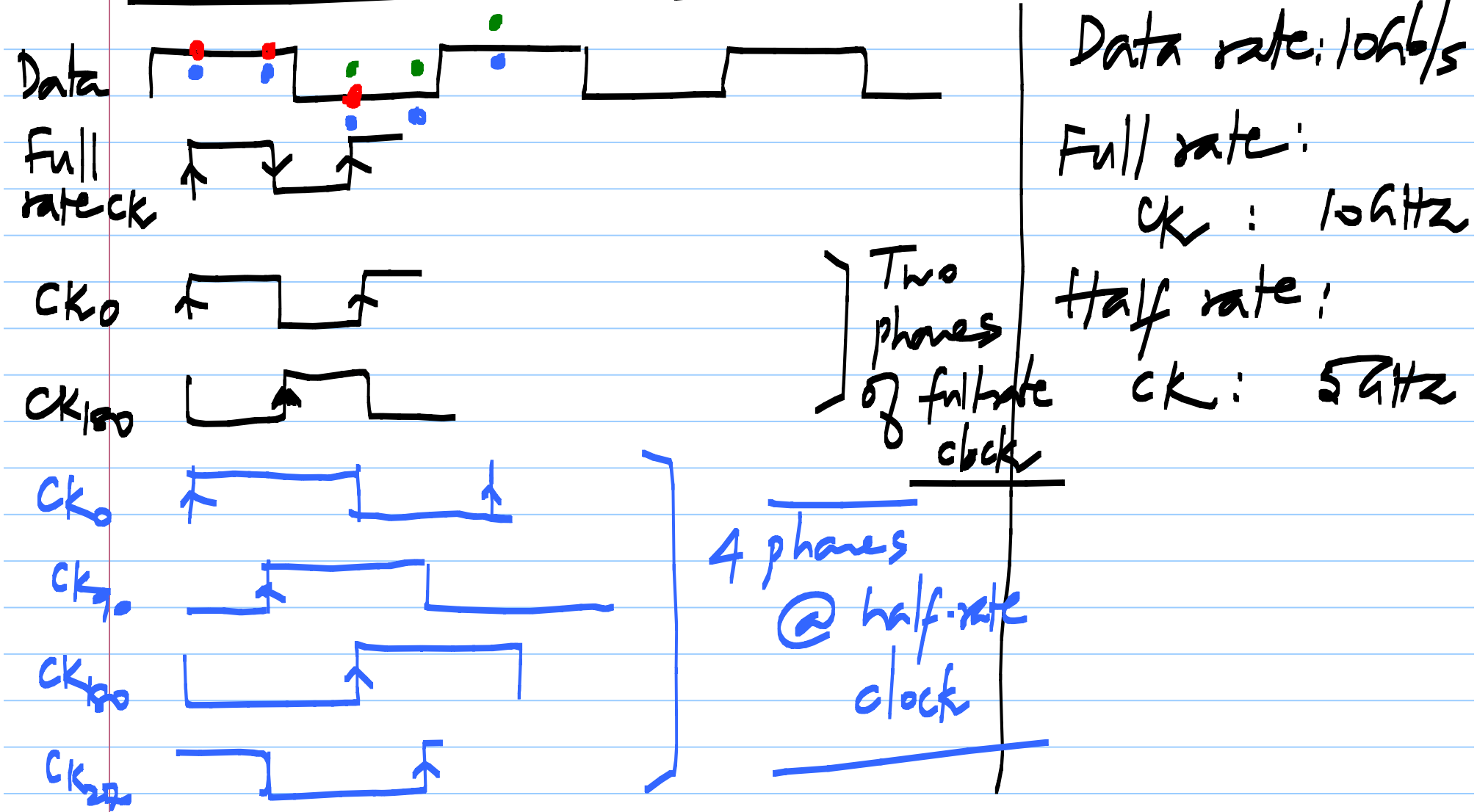

1
2
3
4
5
6
7
Data
CK
A, B, J
ϕ_{CK}
BB Jitter
1
3
4
5
1 UP
5 UP
3 DN
4 DN
Same pp Bang - bang jitter


L
L
E
L
X
L

Half-rate bang-bang phase detector



Data rate: 10Gb/s

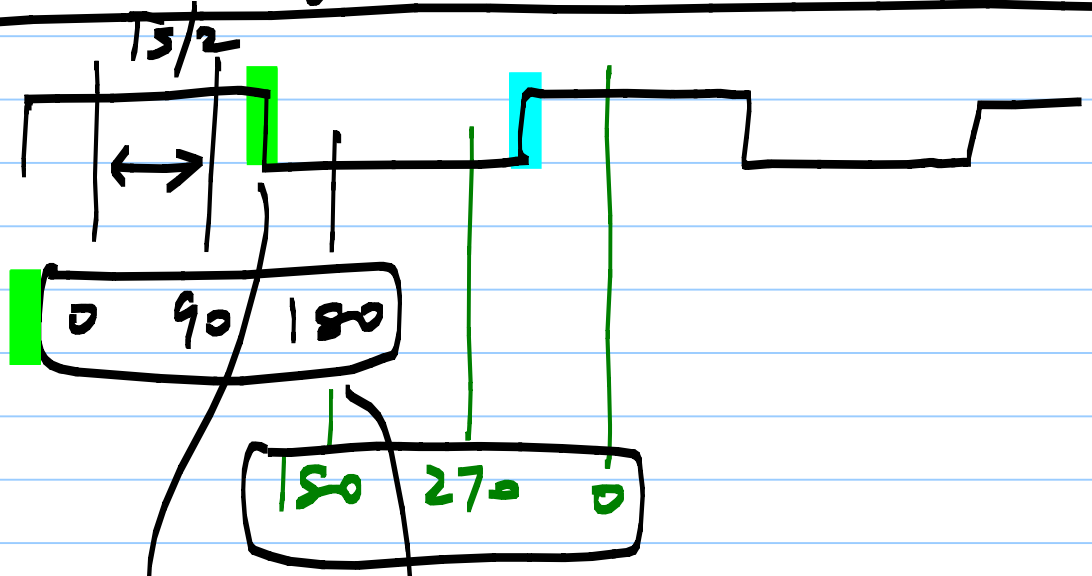
Full rate:

ck : 10GHz

Half rate:

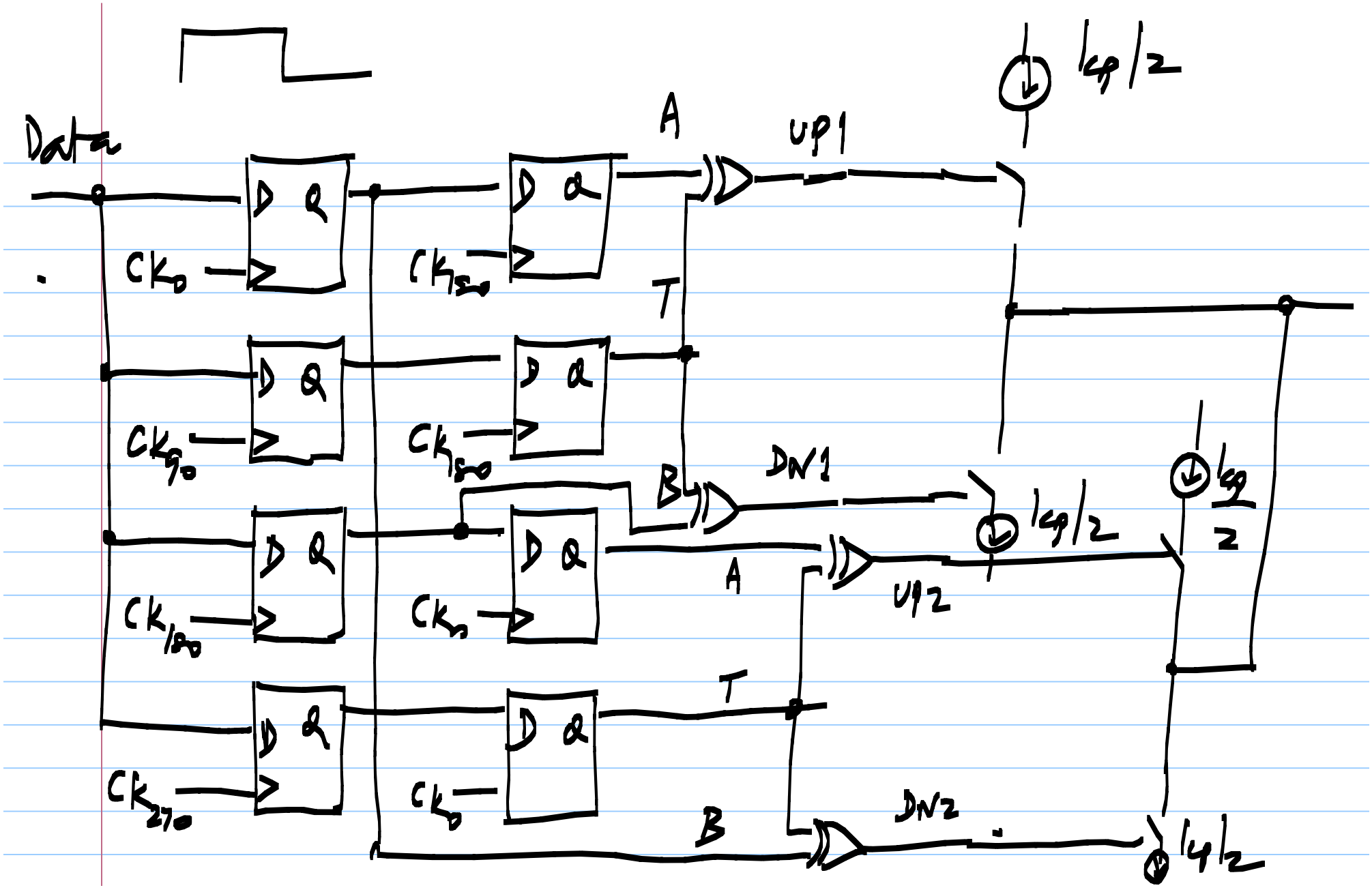
ck : 5GHz

4 phases of the half rate clock



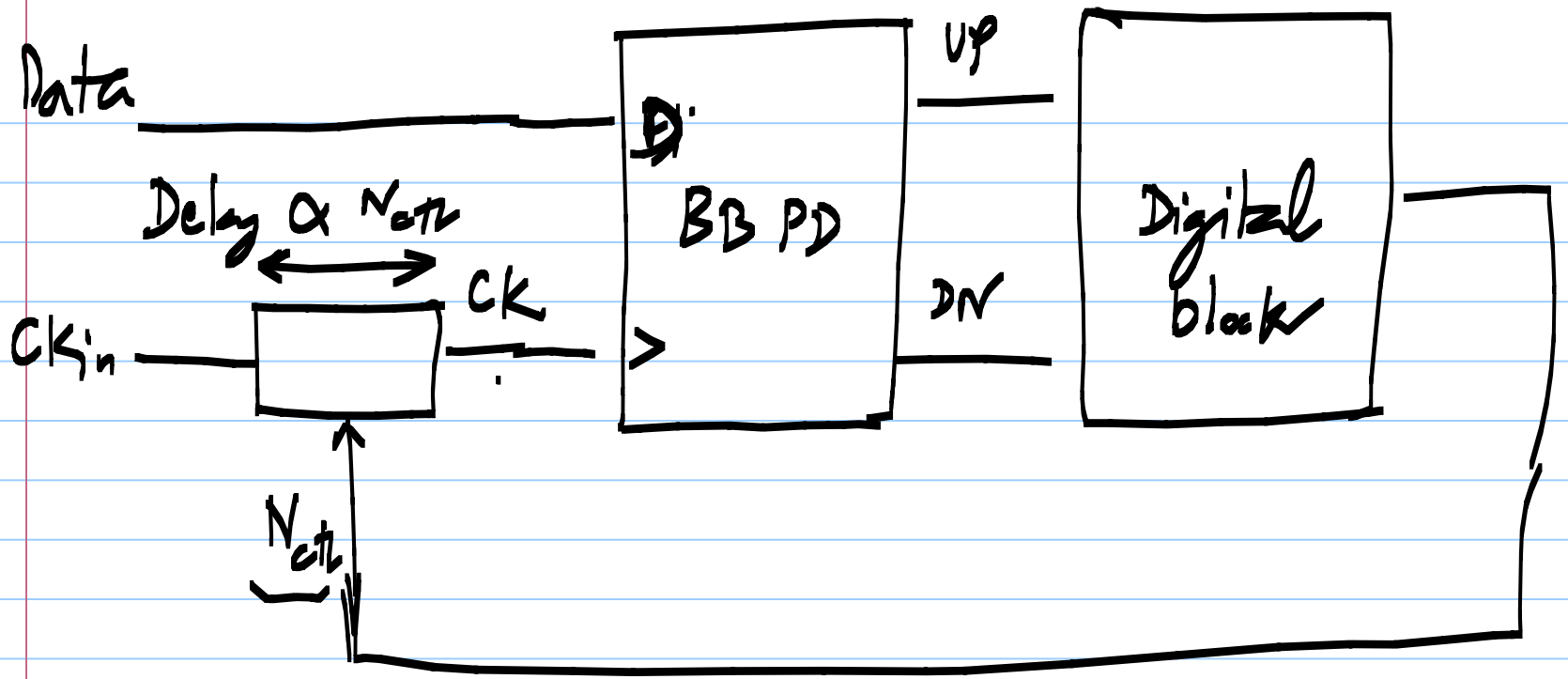
Measure output

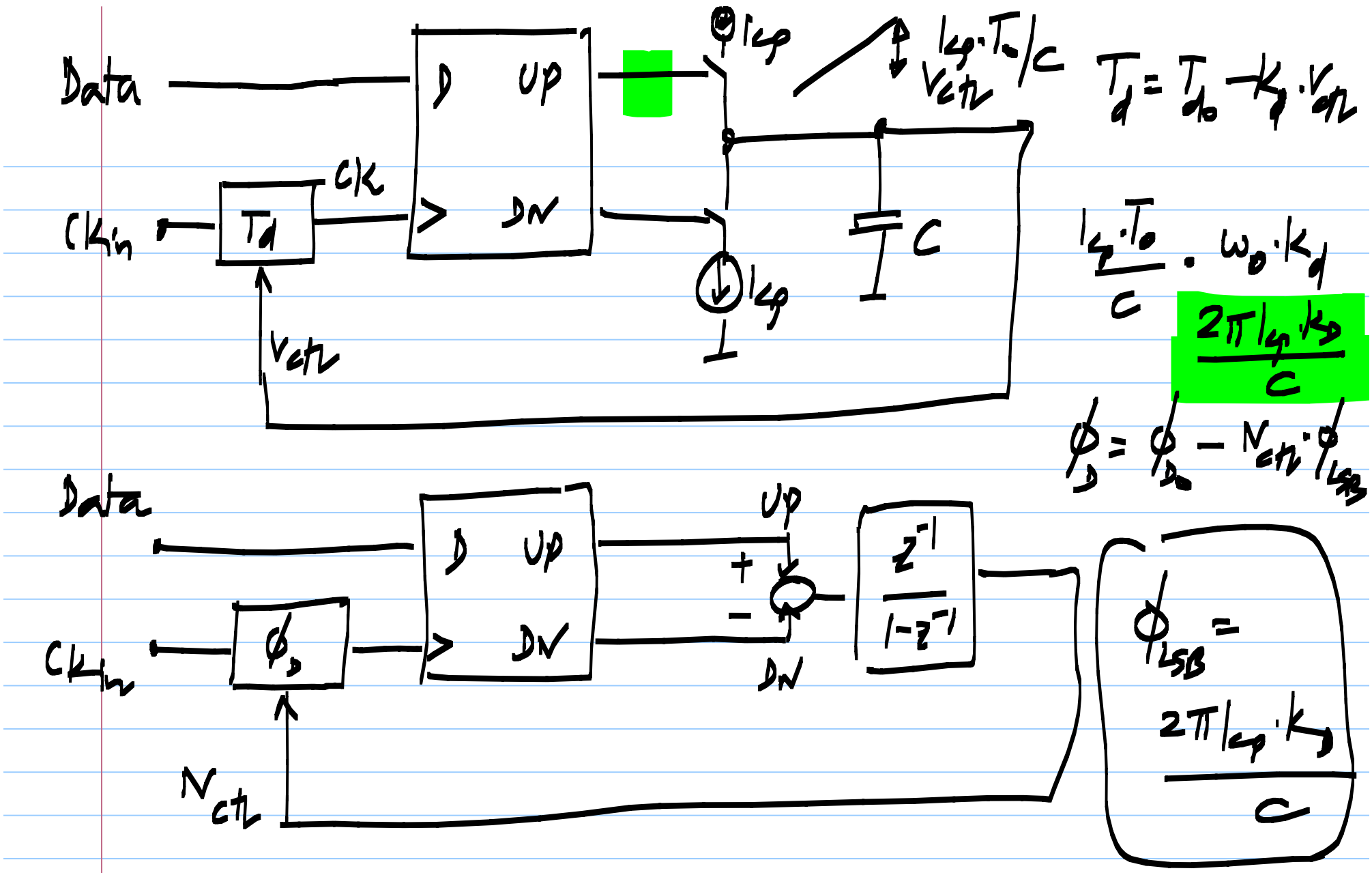
Same latency as before


Data
D Q
CK0
CK90
A
up1
Icp/2
T
CK90
CK180
CK270
B
DN1
A
up2
Icp/2
Icp
2
T
B
DN2
Icp/2

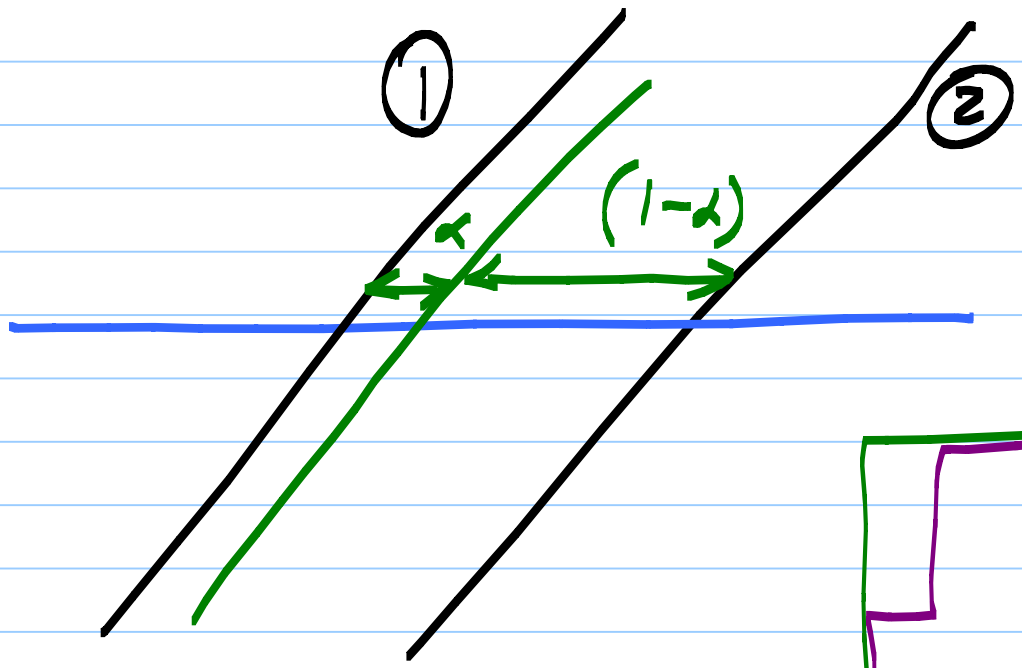
Half rate:

* Distribute clock at a lower frequency
  [But twice the number of phases]
* Waveforms have Longer time to settle
* Longer regeneration time in flip-flops
* Setup, hold time constraints the same (Input data at the original ^ rate)
* ~ 2x the number of components.


Data
D
BB PD
UP
DN
Digital block
Delay α N_{ctrl}
CK
CKin
>
N_{ctrl}


Data
D
UP
DN
CK
CKin
Td
Vctl
Icp
C
Icp
Icp·Td/C
Vctl
Td = Td0 − Kd·Vctl
Icp·Td0/C · ω0·Kd
2π Icp·Kd / C
Data
D
UP
DN
CKin
Φd
Nctl
UP
DN
+
−
z⁻¹ / 1−z⁻¹
ΦLSB =
2π Icp·Kd / C

$$\frac{100\mu A \; 100pF/V}{12F} = 10^{-2} \; 0I$$



$$\alpha \cdot ① + (1-\alpha) \cdot ②$$